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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c54t-10-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTES:

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3.1 **Clocking Scheme/Instruction** Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2 and Example 3-1.

3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).



FIGURE 3-2: **CLOCK/INSTRUCTION CYCLE**

EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



is "flushed" from the pipeline, while the new instruction is being fetched and then executed.

5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the MCLR/VPP pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is <u>RESET</u>. The DRT timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where MCLR is not tied to VDD is shown in Figure 5-3. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset TDRT msec after MCLR goes high.

In Figure 5-4, the on-chip Power-On Reset feature is being used (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the MCLR/VPP pin, and when the MCLR/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

Note: When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the <u>Embedded Control Handbook</u>.

The POR circuit does not produce an internal RESET when VDD declines.

FIGURE 5-2:

EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 k Ω will limit any current flowing into \overline{MCLR} from external capacitor C in the event of \overline{MCLR} pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

6.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers and General Purpose Registers.

The Special Function Registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Purpose Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

For the PIC16C54, PIC16CR54, PIC16C56 and PIC16CR56, the register file is composed of 7 Special Function Registers and 25 General Purpose Registers (Figure 6-4).

For the PIC16C55, the register file is composed of 8 Special Function Registers and 24 General Purpose Registers.

For the PIC16C57 and PIC16CR57, the register file is composed of 8 Special Function Registers, 24 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-5).

For the PIC16C58 and PIC16CR58, the register file is composed of 7 Special Function Registers, 25 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-6).

6.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the File Select Register (FSR). The FSR Register is described in Section 6.7.

FIGURE 6-4:

PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56 REGISTER FILE MAP



6.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not

writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as $000u \ u1uu$ (where u = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 10.0, Instruction Set Summary.

REGISTER 6-1: STATUS REGISTER (ADDRESS: 03h)

	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x				
	PA2	PA1	PA0	TO	PD	Z	DC	С				
	bit 7							bit 0				
bit 7:	PA2: This bit unused at this time.											
	Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.											
bit 6-5:	PA<1:0> : Pr	ogram page p	preselect bits	(PIC16C56/0	CR56)(PIC16	C57/CR57)(P	IC16C58/CR5	58)				
	00 = Page 0	(000h - 1FFh) - PIC16C56	6/CR56, PIC1	6C57/CR57,	PIC16C58/C	R58					
	01 = Page 1	(200h - 3FFh) - PIC16C5	6/CR56, PIC1	6C57/CR57,	PIC16C58/C	R58					
	10 = Page 2 11 = Page 3	. (400h - 3FFh . (600h - 7FFh) - PIC16C5	7/CR57, PIC1	16C58/CR58							
	Each page is	s 512 words.	.,	, e ,								
	Using the PA	A<1:0> bits as	general purp	oose read/wri	te bits in devi	ces which do	not use them	for program				
1.1.4	page presele	ect is not reco	mmended si	nce this may	affect upward	l compatibility	with future pr	oducts.				
Dit 4:	IO: Time-ou	it dit										
	1 = After poly0 = A WDT t	ime-out occur	T instruction	I, OF SLEEP IF	Istruction							
bit 3:	PD: Power-c	down bit										
	1 = After pov	wer-up or by t	he Clrwdt ii	nstruction								
	0 = By exect	ution of the SI	LEEP instruct	ion								
bit 2:	Z: Zero bit											
	1 = The result of the result	ult of an arithm	netic or logic	operation is z	zero							
bit 1.	D = The lest	$\frac{1}{100}$ $\frac{1}$	(for ADDWE 2		tructions)							
DIC 1.			(IOI ADDWF a		silucions							
	1 = A carry f	rom the 4th lo	w order bit o	f the result of	ccurred							
	0 = A carry f	rom the 4th lo	w order bit o	f the result di	d not occur							
	SUBWF	from the Ath	low order bit	of the regult	did not occur							
	1 = A borrow 0 = A borrow	v from the 4th	low order bit	of the result	occurred							
bit 0:	C: Carry/bor	row bit (for AD	DWF, SUBWF	and RRF, RLI	F instructions))						
	ADDWF		SUBW	/F		RRF or RLF						
	1 = A carry c	bccurred	1 = A	borrow did no	ot occur red	Loaded with	LSb or MSb,	respectively				
	v = A carry c		0 = A I									
Lenendi												

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

9.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT Reset or Wake-up Reset generates a device RESET.

The $\overline{\text{TO}}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset (Section 6.3).

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 9.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

9.2.1 WDT PERIOD

An 8-bit counter is available as a prescaler for the Timer0 module (Section 8.2), or as a postscaler for the Watchdog Timer (WDT), respectively. For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not

both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio (Section 6.4).

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see Device Characterization).

Under worst case conditions (VDD = Min., Temperature = Max., WDT prescaler = 1:128), it may take several seconds before a WDT time-out occurs.

9.2.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction RESETS the WDT and the prescaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.



TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	<u>Value</u> on MCLR and WDT Reset
N/A	OPTION	—	—	Tosc	Tose	PSA	PS2	PS1	PS0	11 1111	11 1111

Legend: u = unchanged, - = unimplemented, read as '0'. Shaded cells not used by Watchdog Timer.

13.6 Timing Diagrams and Specifications



FIGURE 13-2: EXTERNAL CLOCK TIMING - PIC16CR54A

TABLE 13-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A

AC Chara	cteristics	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \ \ for \ commercial \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \ \ for \ industrial \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \ \ for \ extended \end{array}$								
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions			
	Fosc	External CLKIN Frequency ⁽¹⁾	DC		4.0	MHz	XT OSC mode			
			DC	—	4.0	MHz	HS osc mode (04)			
			DC	—	10	MHz	HS osc mode (10)			
			DC	—	20	MHz	HS osc mode (20)			
			DC	—	200	kHz	LP osc mode			
		Oscillator Frequency ⁽¹⁾	DC		4.0	MHz	RC osc mode			
			0.1	—	4.0	MHz	XT OSC mode			
			4.0	—	4.0	MHz	HS osc mode (04)			
			4.0	—	10	MHz	HS osc mode (10)			
			4.0	—	20	MHz	HS osc mode (20)			
			5.0		200	kHz	LP osc mode			

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 14-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED



FIGURE 14-7: TYPICA

TYPICAL IPD vs. VDD, WATCHDOG ENABLED



FIGURE 14-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED



IPD, with WDT enabled, has two components: The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At -40° C, the latter dominates explaining the apparently anomalous behavior.





FIGURE 14-18:

TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD



15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04 PIC16LC54A-04I (Commercial, Industrial)				$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$						
PIC16C PIC16C (Comm	PIC16C54A-04, 10, 20 PIC16C54A-04I, 10I, 20I (Commercial, Industrial)			ard Ope ting Terr	$\label{eq:conditions} \begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions			
	Vdd	Supply Voltage								
D001		PIC16LC54A	3.0 2.5	_	6.25 6.25	V V	XT and RC modes LP mode			
D001A		PIC16C54A	3.0 4.5	_	6.25 5.5	V V	RC, XT and LP modes HS mode			
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode			
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset			
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	-	V/ms	See Section 5.1 for details on Power-on Reset			
	IDD	Supply Current ⁽²⁾								
D005		PIC16LC5X	_	0.5	2.5	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes			
				11	27	μΑ	Fosc = 32 kHz, VDD = 2.5V, WDT disabled, LP mode, Commercial			
			_	11	35	μΑ	Fosc = 32 kHz, VDD = 2.5V, WDT disabled, LP mode, Industrial			
D005A		PIC16C5X	—	1.8	2.4	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes			
			—	2.4	8.0	mA	FOSC = 10 MHz, VDD = 5.5V, HS mode			
			—	4.5	16	mA	FOSC = 20 MHz, VDD = 5.5V, HS mode			
				14	29	μA	HOSC = 32 kHz, VDD = 3.0V,			
			-	17	37	μΑ	Fosc = 32 kHz, VDD = 3.0V, WDT disabled, LP mode, Industrial			

Legend: Rows with standard voltage device data only are shaded for improved readability.

These parameters are characterized but not tested.

- † Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- **Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

15.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended) PIC16LC54A-04E (Extended)

PIC16I	C54A-04F		, Condi	tions (unless otherwise specified)						
(Exten	ded)	-	Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended							
PIC16C (Exten	54A-04E, ded)	10E, 20E	Standard Operating Conditions (unless otherwise specified Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended							
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions			
	Vdd	Supply Voltage								
D001		PIC16LC54A	3.0 2.5		6.25 6.25	V V	XT and RC modes LP mode			
D001A		PIC16C54A	3.5 4.5		5.5 5.5	V V	RC and XT modes HS mode			
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾		1.5*	—	V	Device in SLEEP mode			
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	-	Vss	_	V	See Section 5.1 for details on Power-on Reset			
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*		—	V/ms	See Section 5.1 for details on Power-on Reset			
	IDD	Supply Current ⁽²⁾								
D010		PIC16LC54A	-	0.5	25	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes			
			-	11	27	μA	Fosc = 32 kHz, VDD = 2.5V, LP mode, Commercial			
			—	11	35	μA	Fosc = 32 kHz, VDD = 2.5V, LP mode, Industrial			
			—	11	37	μA	Fosc = 32 kHz, VDD = 2.5V, LP mode, Extended			
D010A		PIC16C54A	—	1.8	3.3	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes			
			-	4.8	10	mA	Fosc = 10 MHz, VDD = 5.5V, HS mode			
			-	9.0	20	mA	Fosc = 20 MHz, VDD = 5.5V, HS mode			

Legend: Rows with standard voltage device data only are shaded for improved readability.

- * These parameters are characterized but not tested.
- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

15.6 Timing Diagrams and Specifications

FIGURE 15-2: EXTERNAL CLOCK TIMING - PIC16C54A



TABLE 15-1:	EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

AC Chara	acteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$									
Param No.	Symbol	Characteristic	Characteristic Min Typ† Max Units Conditions								
	Fosc	External CLKIN Fre-	DC		4.0	MHz	XT OSC mode				
		quency ⁽¹⁾	DC	—	2.0	MHz	XT osc mode (PIC16LV54A)				
			DC	—	4.0	MHz	HS osc mode (04)				
			DC	—	10	MHz	HS osc mode (10)				
			DC	—	20	MHz	HS osc mode (20)				
			DC	—	200	kHz	LP osc mode				
		Oscillator Frequency ⁽¹⁾	DC	_	4.0	MHz	RC osc mode				
			DC	—	2.0	MHz	RC osc mode (PIC16LV54A)				
			0.1	—	4.0	MHz	XT osc mode				
			0.1	—	2.0	MHz	XT osc mode (PIC16LV54A)				
			4.0	—	4.0	MHz	HS osc mode (04)				
			4.0	—	10	MHz	HS osc mode (10)				
			4.0	—	20	MHz	HS osc mode (20)				
			5.0		200	kHz	LP osc mode				

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.
 - Instruction cycle period (TcY) equals four times the input oscillator time base period.

NOTES:

17.0 ELECTRICAL CHARACTERISTICS - PIC16LC54A

Absolute Maximum Ratings^(†)

Ambient temperature under bias	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	–0.6V to (VDD + 0.6V)
Total power dissipation ⁽¹⁾	
Max. current out of Vss pin	150 mA
Max. current into Vod pin	100 mA
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, Iк (Vi < 0 or Vi > VDD)	±20 mA
Output clamp current, Iок (Vo < 0 or Vo > Voo)	±20 mA
Max. output current sunk by any I/O pin	
Max. output current sourced by any I/O pin	20 mA
Max. output current sourced by a single I/O (Port A, B or C)	50 mA
Max. output current sunk by a single I/O (Port A, B or C)	50 mA
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH} + \sum {(VD	D-VOH) X IOH} + Σ (VOL X IOL)

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



FIGURE 18-12: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 PF, 25°C)





20.0 DEVICE CHARACTERIZATION - PIC16LC54C 40MHz

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.





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21.0 PACKAGING INFORMATION

21.1 Package Marketing Information

18-Lead PDIP



28-Lead Skinny PDIP (.300")



28-Lead PDIP (.600")



18-Lead SOIC



28-Lead SOIC



20-Lead SSOP



28-Lead SSOP





Example



Example



Example



Example



Example



Example



28-Lead Plastic Dual In-line (P) - 600 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES*		MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28		
Pitch	р		.100			2.54		
Top to Seating Plane	А	.160	.175	.190	4.06	4.45	4.83	
Molded Package Thickness	A2	.140	.150	.160	3.56	3.81	4.06	
Base to Seating Plane	A1	.015			0.38			
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88	
Molded Package Width	E1	.505	.545	.560	12.83	13.84	14.22	
Overall Length	D	1.395	1.430	1.465	35.43	36.32	37.21	
Tip to Seating Plane	L	.120	.130	.135	3.05	3.30	3.43	
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38	
Upper Lead Width	B1	.030	.050	.070	0.76	1.27	1.78	
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56	
Overall Row Spacing §	eB	.620	.650	.680	15.75	16.51	17.27	
Mold Draft Angle Top	α	5	10	15	5	10	15	
Mold Draft Angle Bottom	β	5	10	15	5	10	15	

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-011 Drawing No. C04-079

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

ftp://ftp.microchip.com

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked
 Questions
- Design Tips
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