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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c54t-rci-so

3.1   Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2 and Example 3-1.
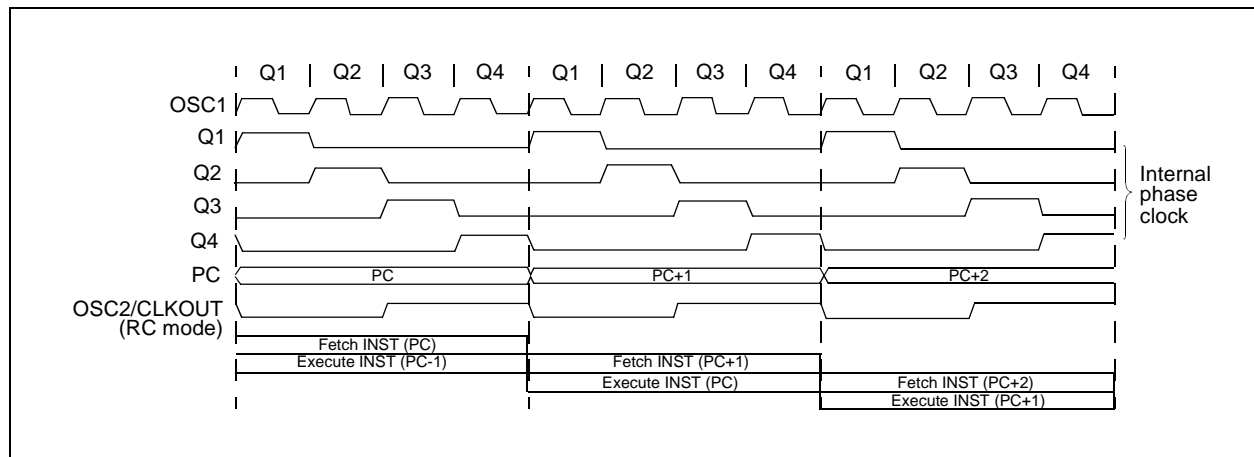
3.2   Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).
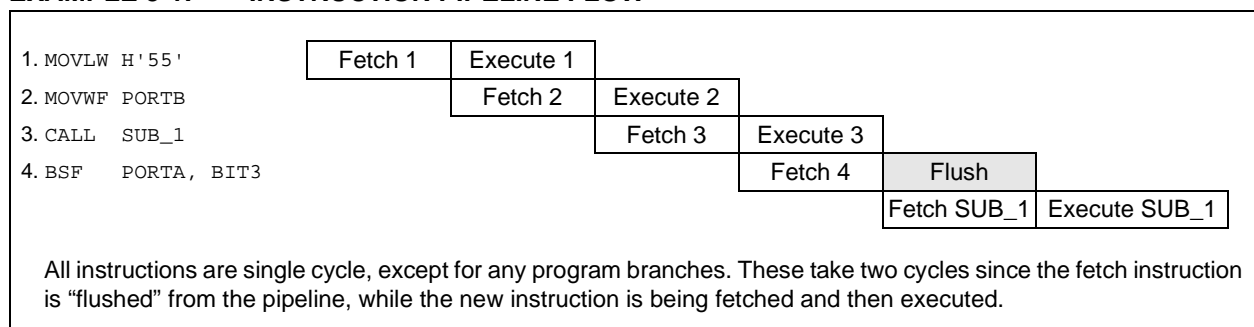
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2:   CLOCK/INSTRUCTION CYCLE

EXAMPLE 3-1:   INSTRUCTION PIPELINE FLOW

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline, while the new instruction is being fetched and then executed.

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7.6 I/O Programming Considerations

7.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 7-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 7-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                 PORT latch  PORT pins
;                 ----------  ----------
  BCF    PORTB, 7  ;01pp pppp   11pp pppp
  BCF    PORTB, 6  ;10pp pppp   11pp pppp
  MOVLW  H'3F'     ;
  TRIS   PORTB     ;10pp pppp   10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

7.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 7-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 7-2: SUCCESSIVE I/O OPERATION

This example shows a write to PORTB followed by a read from PORTB.
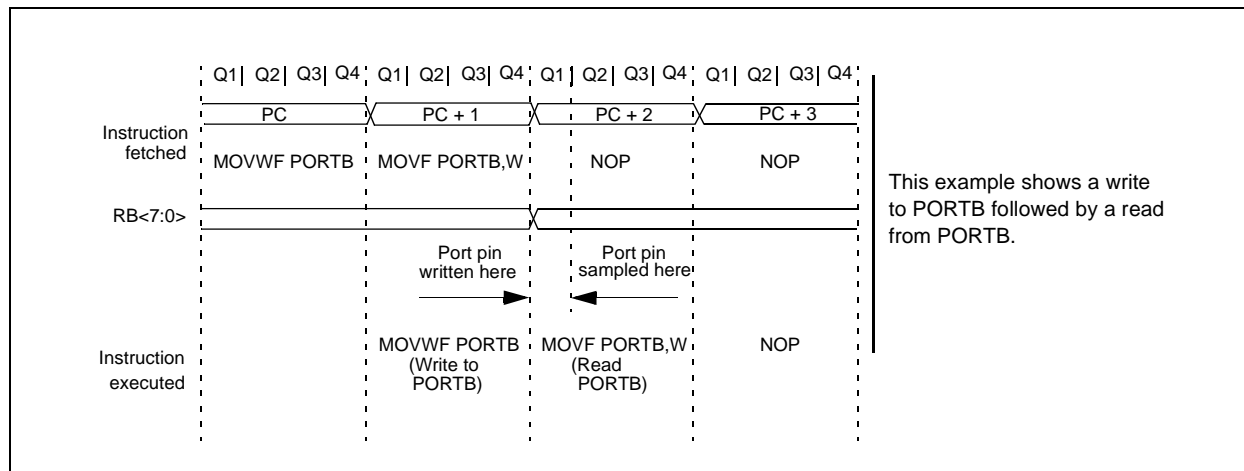
8.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.
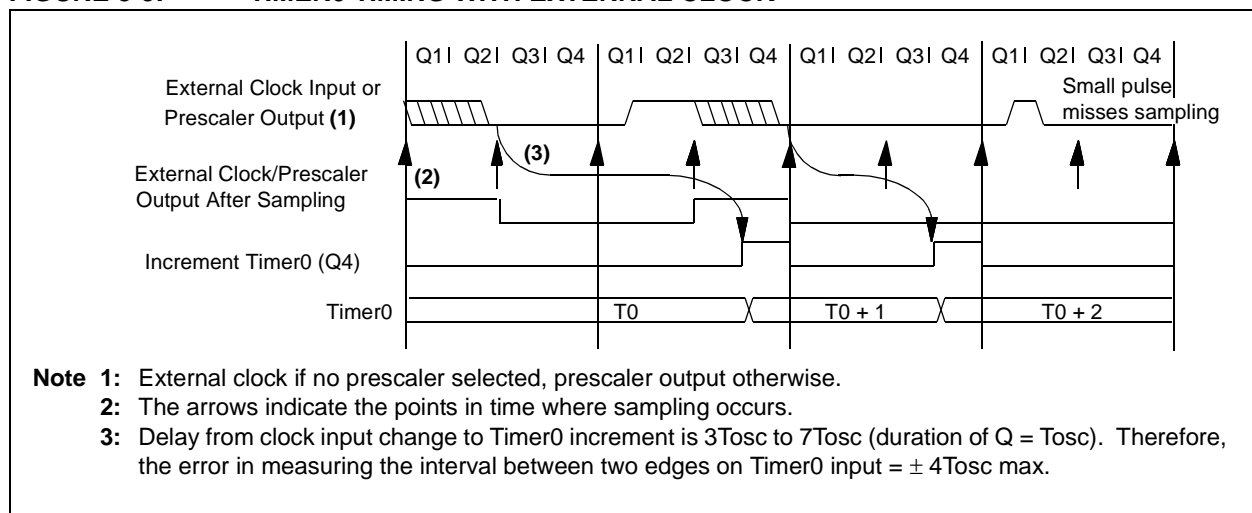
8.1.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 8-5). Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

8.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 8-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 8-5: TIMER0 TIMING WITH EXTERNAL CLOCK

Note 1: External clock if no prescaler selected, prescaler output otherwise.
2: The arrows indicate the points in time where sampling occurs.
3: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc (duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ± 4Tosc max.

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8.2   Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 9.2.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

8.2.1   SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 8-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 8-1:   CHANGING PRESCALER (TIMER0→WDT)

```
CLRWDT                  ;Clear WDT
CLRF   TMR0             ;Clear TMR0 & Prescaler
MOVLW  B'00xx1111'      ;Last 3 instructions in
                         ; this example
OPTION                  ;are required only if
                        ;desired
CLRWDT                  ;PS<2:0> are 000 or
                        ;001
MOVLW  B'00xx1xxx'      ;Set Prescaler to
OPTION                  ;desired WDT rate
```
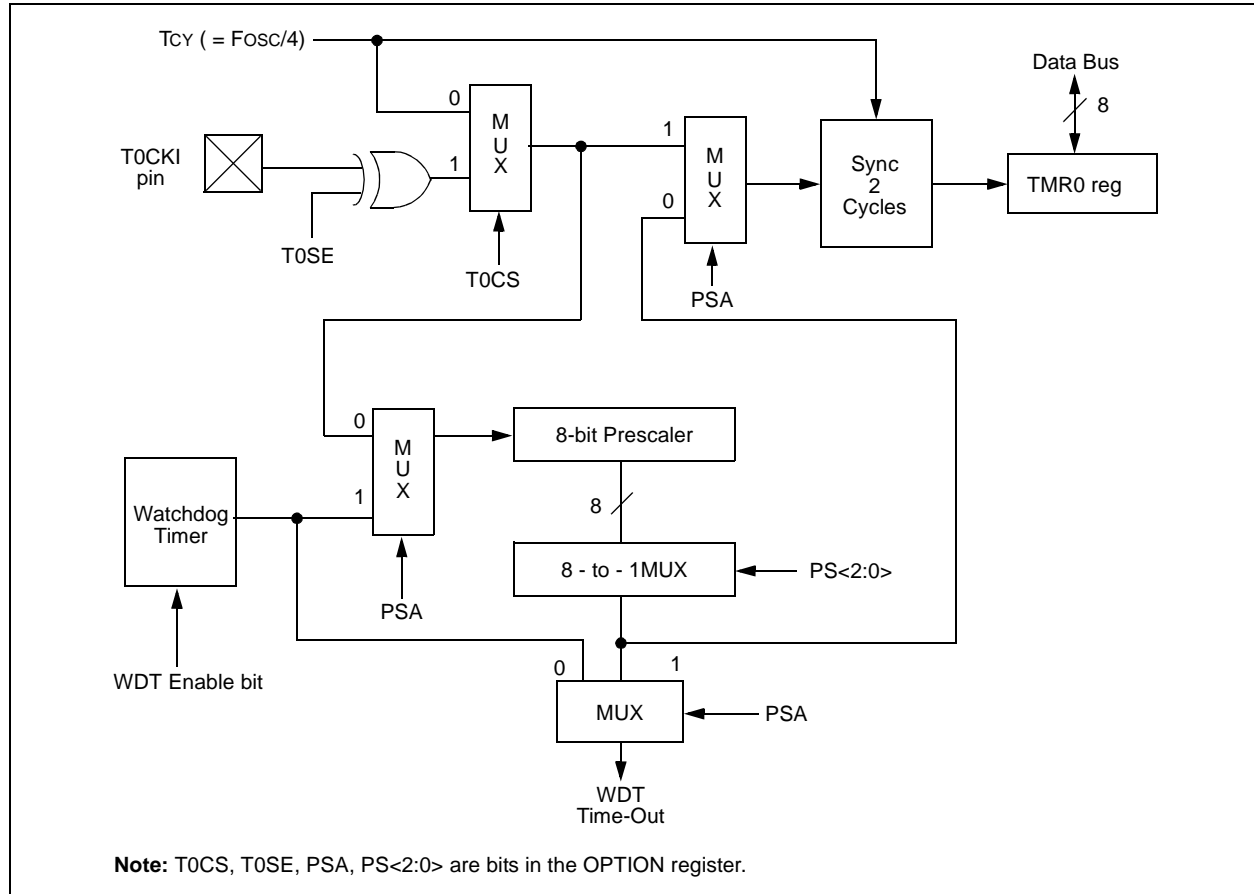
To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 8-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

EXAMPLE 8-2:   CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                  ;Clear WDT and
                        ;prescaler
MOVLW  B'xxxx0xxx'      ;Select TMR0, new
                        ;prescale value and
                        ;clock source
OPTION
```

FIGURE 8-6: **BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER**

Note: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

NOTES:

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12.3   DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)			Standard Operating Conditions (unless otherwise specified) Operating Temperature −40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
D001	VDD	**Supply Voltage** PIC16C5X-RCE PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-LPE	 3.25 3.25 4.5 4.5 2.5	 — — — — —	 6.0 6.0 5.5 5.5 6.0	 V V V V V	
D002	VDR	**RAM Data Retention Voltage**[1]	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	**Supply Current**[2] PIC16C5X-RCE[3] PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-HSE PIC16C5X-LPE	 — — — — — —	 1.8 1.8 4.8 4.8 9.0 19	 3.3 3.3 10 10 20 55	 mA mA mA mA mA μA	FOSC = 4 MHz, VDD = 5.5V FOSC = 4 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 16 MHz, VDD = 5.5V FOSC = 32 kHz, VDD = 3.25V, WDT disabled
D020	IPD	**Power-down Current**[2]	— —	5.0 0.8	22 18	μA μA	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled

*   These parameters are characterized but not tested.

†   Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

   2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

   a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

   b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

   3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial −40°C ≤ TA ≤ +85°C for industrial −40°C ≤ TA ≤ +125°C for extended					
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**	
1	Tosc	External CLKIN Period[1]	250	—	—	ns	XT osc mode	
			100	—	—	ns	10 MHz mode	
			50	—	—	ns	HS osc mode (Comm/Ind)	
			62.5	—	—	ns	HS osc mode (Ext)	
			25	—	—	μs	LP osc mode	
		Oscillator Period[1]	250	—	—	ns	RC osc mode	
			250	—	10,000	ns	XT osc mode	
			100	—	250	ns	10 MHz mode	
			50	—	250	ns	HS osc mode (Comm/Ind)	
			62.5	—	250	ns	HS osc mode (Ext)	
			25	—	—	μs	LP osc mode	
2	Tcy	Instruction Cycle Time[2]	—	4/Fosc	—	—		
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator	
			20*	—	—	ns	HS oscillator	
			2.0*	—	—	μs	LP oscillator	
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator	
			—	—	25*	ns	HS oscillator	
			—	—	50*	ns	LP oscillator	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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13.4 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	VIL	**Input Low Voltage** I/O ports $\overline{\text{MCLR}}$ (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss	— — — — —	0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V V	Pin at hi-impedance RC mode only[3] XT, HS and LP modes
D040	VIH	**Input High Voltage** I/O ports I/O ports I/O ports $\overline{\text{MCLR}}$ (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD	— — — — — — —	VDD VDD VDD VDD VDD VDD VDD	V V V V V V V	For all VDD[4] 4.0V < VDD ≤ 5.5V[4] VDD > 5.5V RC mode only[3] XT, HS and LP modes
D050	VHYS	**Hysteresis of Schmitt Trigger inputs**	0.15 VDD*	—	—	V	
D060	IIL	**Input Leakage Current**[1,2] I/O ports MCLR MCLR T0CKI OSC1	–1.0 –5.0 — –3.0 –3.0	0.5 — 0.5 0.5 0.5	+1.0 — +5.0 +3.0 +3.0	µA µA µA µA µA	**For VDD ≤ 5.5V:** VSS ≤ VPIN ≤ VDD, pin at hi-impedance VPIN = VSS + 0.25V VPIN = VDD VSS ≤ VPIN ≤ VDD VSS ≤ VPIN ≤ VDD, XT, HS and LP modes
D080	VOL	**Output Low Voltage** I/O ports OSC2/CLKOUT	— —	— —	0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, RC mode only
D090	VOH	**Output High Voltage**[2] I/O ports OSC2/CLKOUT	VDD – 0.7 VDD – 0.7	— —	— —	V V	IOH = –5.4 mA, VDD = 4.5V IOH = –1.0 mA, VDD = 4.5V, RC mode only

*   These parameters are characterized but not tested.

†   Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guid-ance only and is not tested.

Note 1: The leakage current on the $\overline{\text{MCLR}}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

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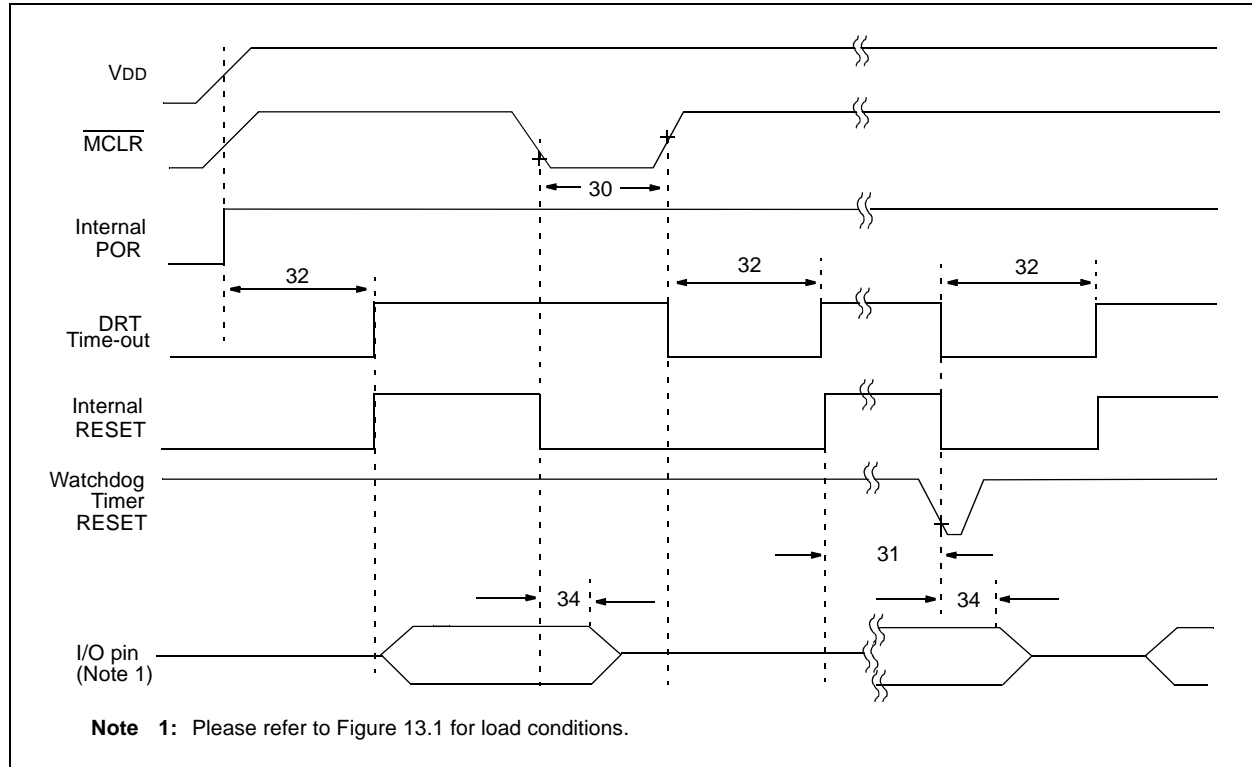**FIGURE 13-4:** **RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR54A**

Note 1: Please refer to Figure 13.1 for load conditions.

TABLE 13-3: **RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR54A**

AC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature $\quad 0°C \leq T_A \leq +70°C$ for commercial $\qquad -40°C \leq T_A \leq +85°C$ for industrial $\qquad -40°C \leq T_A \leq +125°C$ for extended					
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	1.0*	—	—	µs	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7.0*	18*	40*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	7.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	TioZ	I/O Hi-impedance from $\overline{MCLR}$ Low	—	—	1.0*	µs	

*   These parameters are characterized but not tested.

†   Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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TABLE 15-1:   EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature 0°C ≤ TA ≤ +70°C for commercial −40°C ≤ TA ≤ +85°C for industrial −20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I −40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
1	TOSC	External CLKIN Period[1]	250	—	—	ns	XT OSC mode
			500	—	—	ns	XT OSC mode (PIC16LV54A)
			250	—	—	ns	HS OSC mode (04)
			100	—	—	ns	HS OSC mode (10)
			50	—	—	ns	HS OSC mode (20)
			5.0	—	—	μs	LP OSC mode
		Oscillator Period[1]	250	—	—	ns	RC OSC mode
			500	—	—	ns	RC OSC mode (PIC16LV54A)
			250	—	10,000	ns	XT OSC mode
			500	—	—	ns	XT OSC mode (PIC16LV54A)
			250	—	250	ns	HS OSC mode (04)
			100	—	250	ns	HS OSC mode (10)
			50	—	250	ns	HS OSC mode (20)
			5.0	—	200	μs	LP OSC mode
2	Tcy	Instruction Cycle Time[2]	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

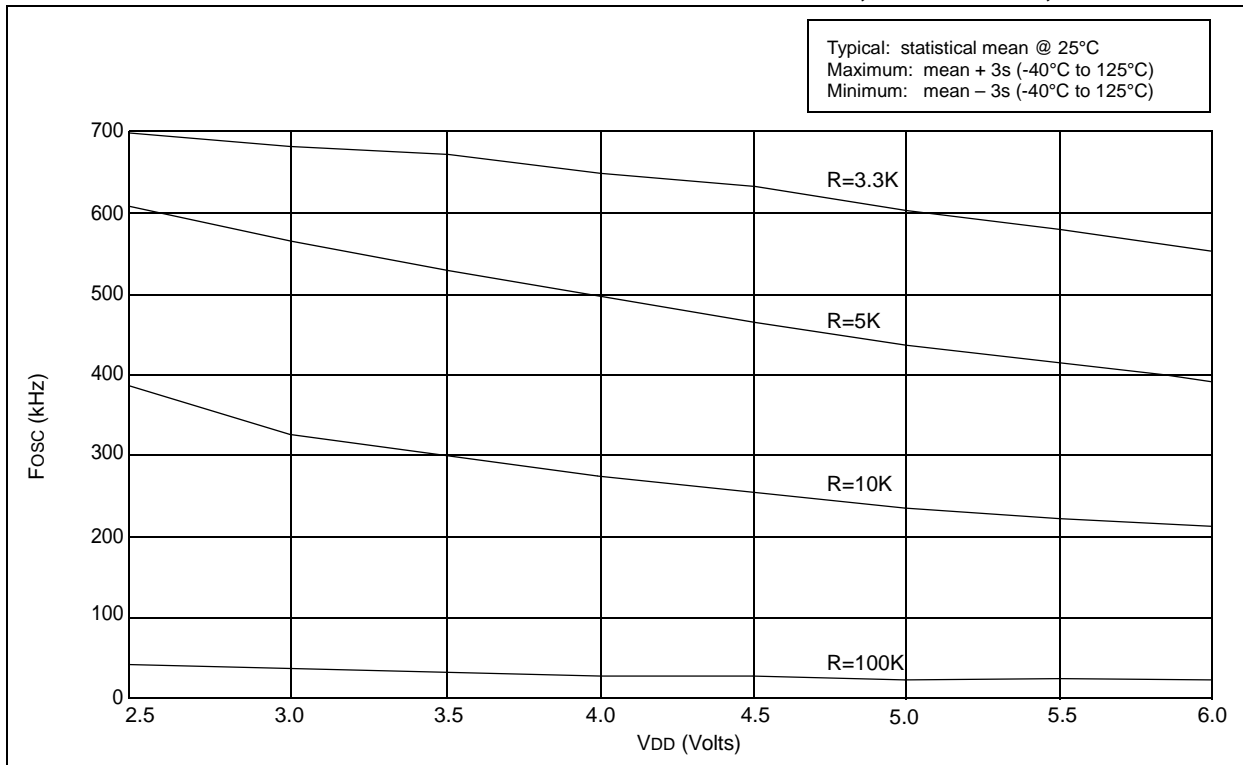*   These parameters are characterized but not tested.

†   Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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FIGURE 16-4: **TYPICAL RC OSCILLATOR FREQUENCY vs. V_{DD}, C_{EXT} = 300 pF, 25°C**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

17.0   ELECTRICAL CHARACTERISTICS - PIC16LC54A

Absolute Maximum Ratings[†]

Ambient temperature under bias..−55°C to +125°C

Storage temperature .... −65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ....0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS}...0 to +14V

Voltage on all other pins with respect to V_{SS} .... −0.6V to (V_{DD} + 0.6V)

Total power dissipation[1] ....800 mW

Max. current out of V_{SS} pin ....150 mA

Max. current into V_{DD} pin ....100 mA

Max. current into an input pin (T0CKI only) ....±500 µA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})...±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ....±20 mA

Max. output current sunk by any I/O pin ....25 mA

Max. output current sourced by any I/O pin ....20 mA

Max. output current sourced by a single I/O (Port A, B or C) ....50 mA

Max. output current sunk by a single I/O (Port A, B or C) ....50 mA

Note 1: Power dissipation is calculated as follows: Pdis = V_{DD} x {I_{DD} - $\sum I_{OH}$} + $\sum$ {(V_{DD}-V_{OH}) x I_{OH}} + $\sum$(V_{OL} x I_{OL})

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

17.4   Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 17-5:   **LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B-04, 20**

Pin

C_L

Vss

C_L = 50 pF   for all pins and OSC2 for RC mode

0 -15 pF   for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1
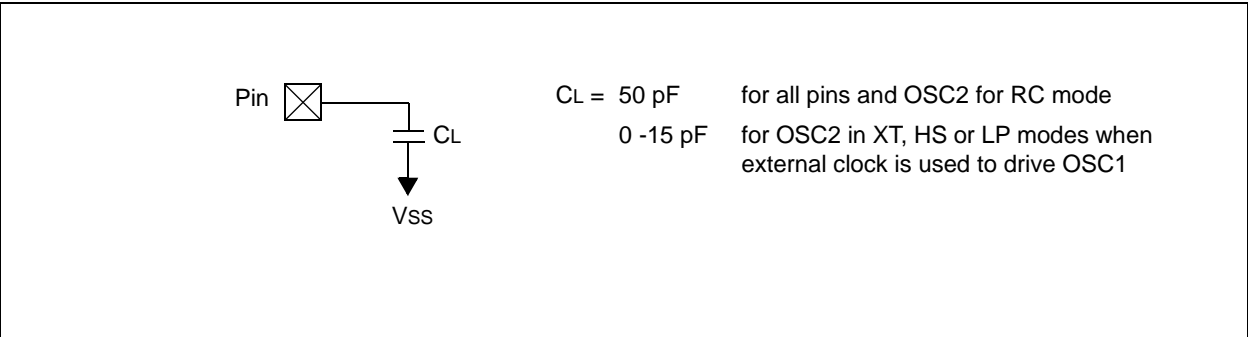
FIGURE 18-10: **VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (IN XT, HS AND LP MODES) vs. VDD**
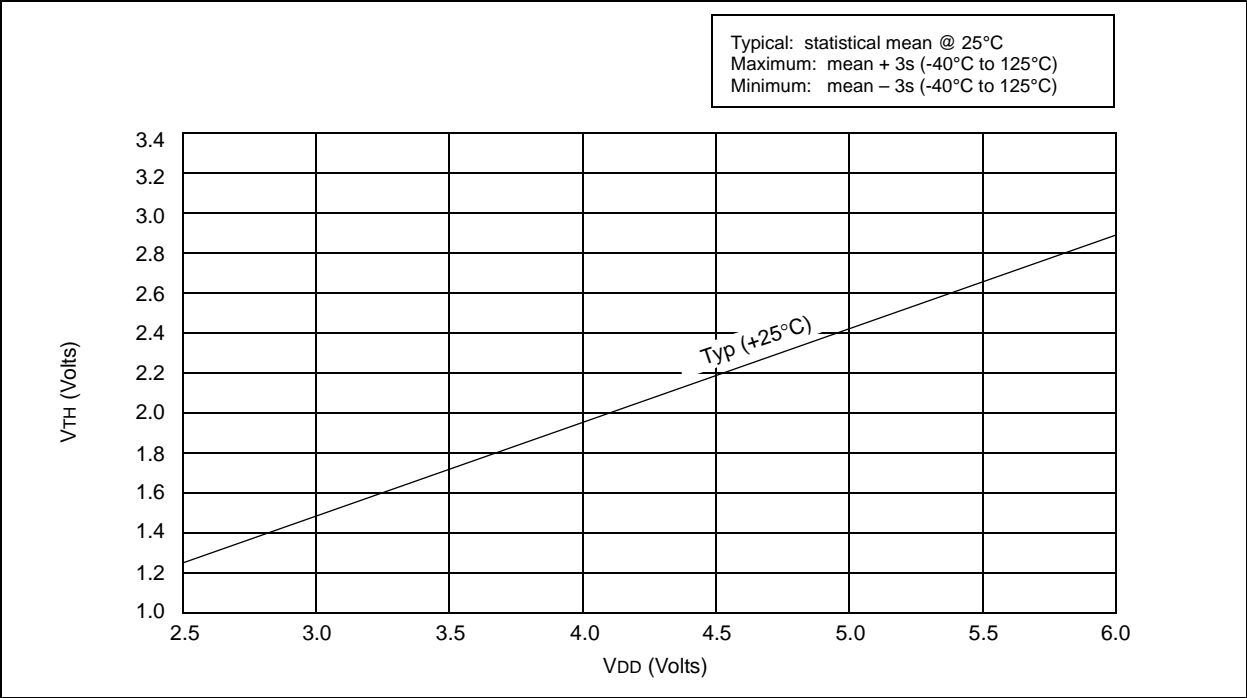
FIGURE 18-11: **TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 PF, 25°C)**

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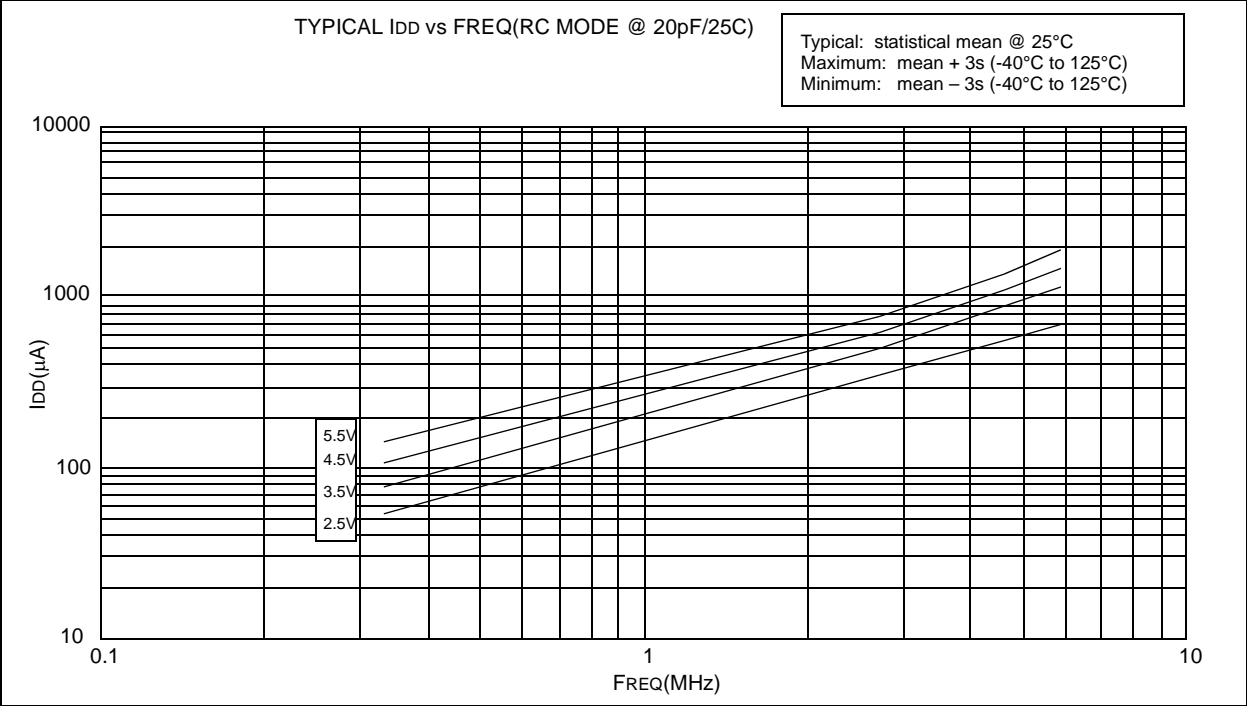
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FIGURE 19-5: **RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X-40**

Note 1: Please refer to Figure 19-2 for load conditions.
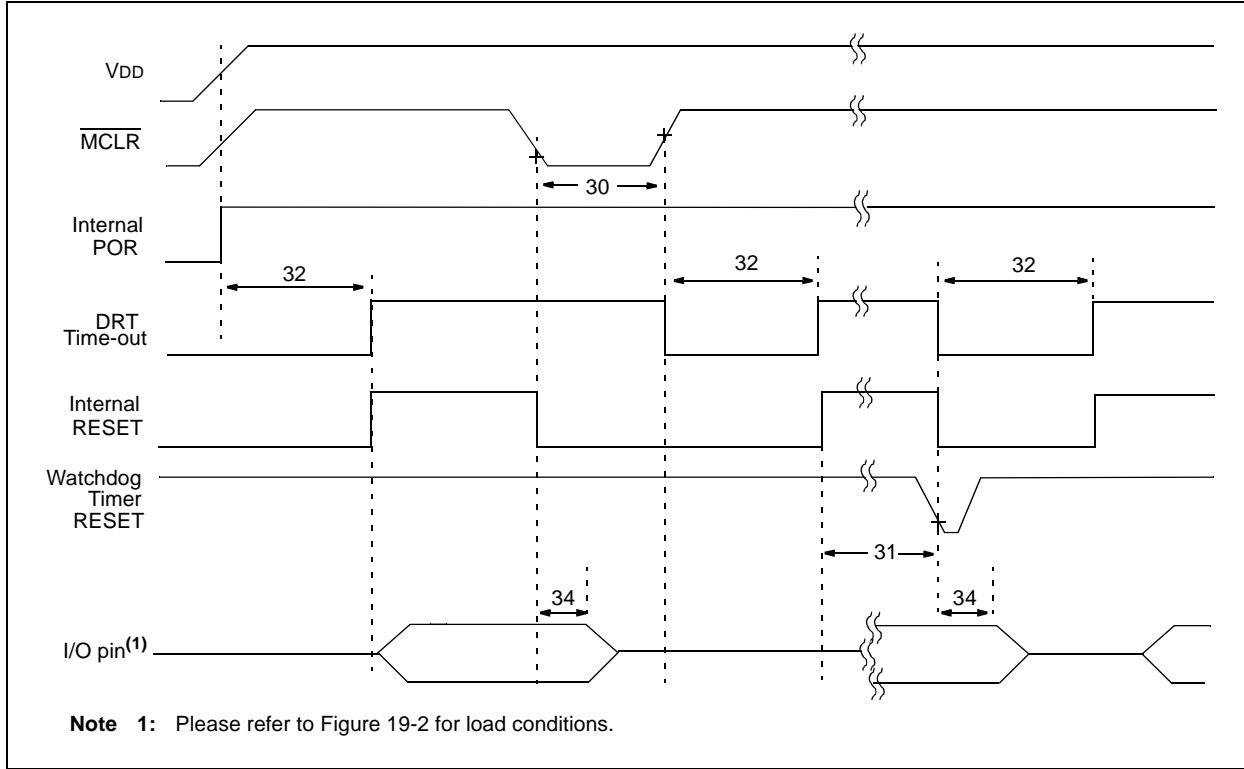
TABLE 19-3: **RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X-40**

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) Operating Voltage VDD range is described in Section 19.1.						
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	1000*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from $\overline{MCLR}$ Low	100*	300*	1000*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

1. Check any `CALL`, `GOTO` or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.

2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.

3. Eliminate any special function register page switching. Redefine data variables to reallocate them.

4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.

5. Change RESET vector to proper value for processor used.

6. Remove any use of the `ADDLW, RETURN` and `SUBLW` instructions.

7. Rewrite any code segments that use interrupts.

APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.

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NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-	XX	X	/XX	XXX
Device		Frequency Range/OSC Type	Temperature Range	Package	Pattern

Device	PIC16C54	PIC16C54T[2]
	PIC16C54A	PIC16C54AT[2]
	PIC16CR54A	PIC16CR54AT[2]
	PIC16C54C	PIC16C54CT[2]
	PIC16CR54C	PIC16CR54CT[2]
	PIC16C55	PIC16C55T[2]
	PIC16C55A	PIC16C55AT[2]
	PIC16C56	PIC16C56T[2]
	PIC16C56A	PIC16C56AT[2]
	PIC16CR56A	PIC16CR56AT[2]
	PIC16C57	PIC16C57T[2]
	PIC16C57C	PIC16C57CT[2]
	PIC16CR57C	PIC16CR57CT[2]
	PIC16C58B	PIC16C58BT[2]
	PIC16CR58B	PIC16CR58BT[2]

Frequency Range/ Oscillator Type	RC	Resistor Capacitor
	LP	Low Power Crystal
	XT	Standard Crystal/Resonator
	HS	High Speed Crystal
	02	200 KHz (LP) or 2 MHz (XT and RC)
	04	200 KHz (LP) or 4 MHz (XT and RC)
	10	10 MHz (HS only)
	20	20 MHz (HS only)
	40	40 MHz (HS only)
	b[4]	No oscillator type for JW packages[3]

*RC/LP/XT/HS are for 16C54/55/56/57 devices only
-02 is available for 16LV54A only
-04/10/20 options are available for all other devices
-40 is available for 16C54C/55A/56A/57C/58B devices only

Temperature Range	b[4]	=	0°C to +70°C
	I	=	-40°C to +85°C
	E	=	-40°C to +125°C

Package	S	=	Die in Waffle Pack
	JW	=	28-pin 600 mil/18-pin 300 mil windowed CER-DIP[3]
	P	=	28-pin 600 mil/18-pin 300 mil PDIP
	SO	=	300 mil SOIC
	SS	=	209 mil SSOP
	SP	=	28-pin 300 mil Skinny PDIP

*See Section 21 for additional package information.

Pattern	QTP, SQTP, ROM code (factory specified) or Special Requirements. Blank for OTP and Windowed devices.

Examples:

a) PIC16C55A - 04/P 301 = Commercial Temp., PDIP package, 4 MHz, standard V_{DD} limits, QTP pattern #301

b) PIC16LC54C - 04I/SO Industrial Temp., SOIC package, 200 kHz, extended V_{DD} limits

c) PIC16C57 - RC/SP = RC Oscillator, commercial temp, skinny PDIP package, 4 MHz, standard V_{DD} limits

d) PIC16C58BT -40/SS 123 = commercial temp, SSOP package in tape and reel, 4 MHz, extended V_{DD} limits, ROM pattern #123

Note 1: C = normal voltage range
LC = extended

2: T = in tape and reel - SOIC and SSOP packages only

3: JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirements of each oscillator type, including LC devices.

4: b = Blank

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Worldwide Site (www.microchip.com)