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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c54t-xt-ss

PIC16C5X

TABLE 5-3: RESET CONDITIONS FOR ALL REGISTERS

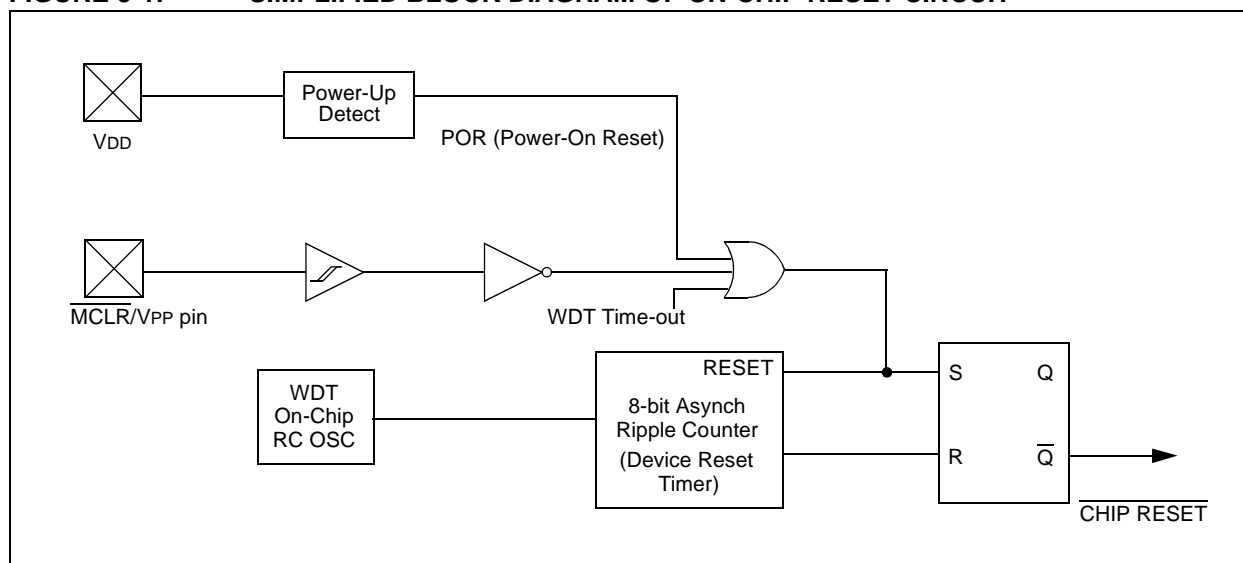
Register	Address	Power-On Reset	MCLR or WDT Reset
W	N/A	xxxx xxxx	uuuu uuuu
TRIS	N/A	1111 1111	1111 1111
OPTION	N/A	--11 1111	--11 1111
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000q quuu
FSR ⁽¹⁾	04h	1xxx xxxx	1uuu uuuu
PORTA	05h	---- xxxx	---- uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu
PORTC ⁽²⁾	07h	xxxx xxxx	uuuu uuuu
General Purpose Register Files	07-7Fh	xxxx xxxx	uuuu uuuu

Legend: x = unknown u = unchanged - = unimplemented, read as '0'
q = see tables in Table 5-1 for possible values.

Note 1: These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for MCLR and WDT Reset, the value is 111u uuuu.

2: General purpose register file on PIC16C54/CR54/C56/CR56/C58/CR58.

FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



5.2 Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides an 18 ms nominal time-out on RESET regardless of Oscillator mode used. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows VDD to rise above VDD min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after the voltage on the MCLR/VPP pin has reached a logic high (VIH) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The Device Reset time delay will vary from chip to chip due to VDD, temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the PIC16C5X from SLEEP mode automatically.

5.3 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be RESET in the event of a brown-out.

To RESET PIC16C5X devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 5-6, Figure 5-7 and Figure 5-8.

FIGURE 5-6: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1

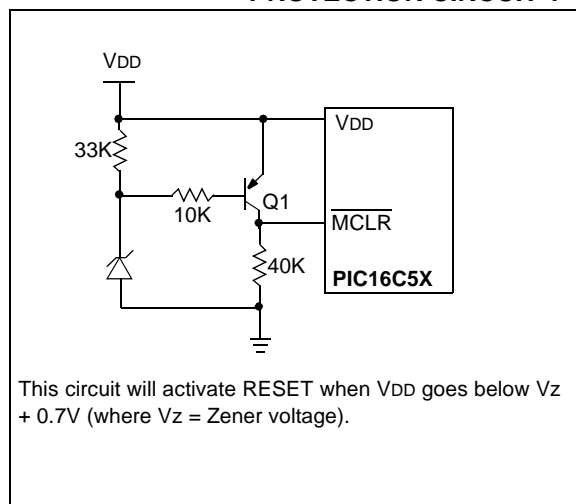


FIGURE 5-7: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2

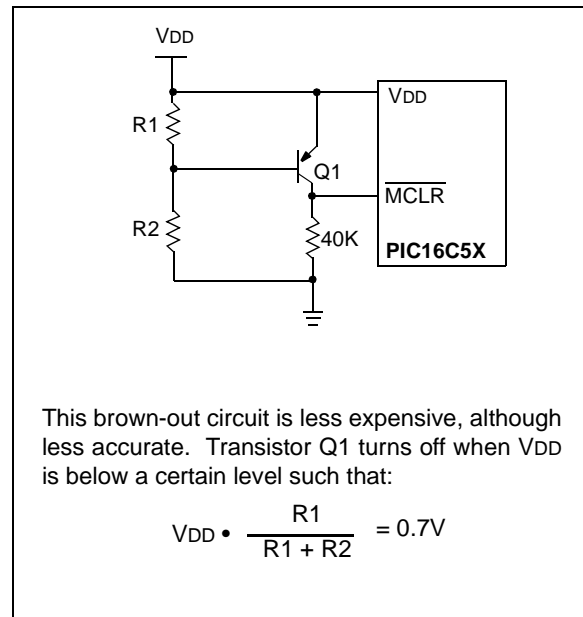
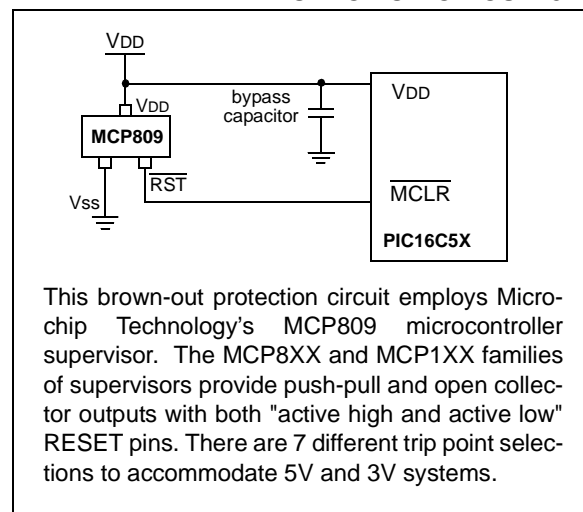


FIGURE 5-8: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



6.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the \overline{TO} and \overline{PD} bits are not

writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS Register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 10.0, Instruction Set Summary.

REGISTER 6-1: STATUS REGISTER (ADDRESS: 03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
PA2	PA1	PA0	\overline{TO}	\overline{PD}	Z	DC	C
bit 7			bit 0				

bit 7: **PA2:** This bit unused at this time.

Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

bit 6-5: **PA<1:0>:** Program page preselect bits (PIC16C56/CR56)(PIC16C57/CR57)(PIC16C58/CR58)

00 = Page 0 (000h - 1FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58

01 = Page 1 (200h - 3FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58

10 = Page 2 (400h - 5FFh) - PIC16C57/CR57, PIC16C58/CR58

11 = Page 3 (600h - 7FFh) - PIC16C57/CR57, PIC16C58/CR58

Each page is 512 words.

Using the PA<1:0> bits as general purpose read/write bits in devices which do not use them for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: **\overline{TO} :** Time-out bit

1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction

0 = A WDT time-out occurred

bit 3: **\overline{PD} :** Power-down bit

1 = After power-up or by the `CLRWDT` instruction

0 = By execution of the `SLEEP` instruction

bit 2: **Z:** Zero bit

1 = The result of an arithmetic or logic operation is zero

0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC:** Digit carry/borrow bit (for `ADDWF` and `SUBWF` instructions)

ADDWF

1 = A carry from the 4th low order bit of the result occurred

0 = A carry from the 4th low order bit of the result did not occur

SUBWF

1 = A borrow from the 4th low order bit of the result did not occur

0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C:** Carry/borrow bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

ADDWF

1 = A carry occurred

0 = A carry did not occur

SUBWF

1 = A borrow did not occur

0 = A borrow occurred

RRF or RLF

Loaded with LSb or MSb, respectively

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

1 = bit is set

0 = bit is cleared

x = bit is unknown

PIC16C5X

6.5.1 PAGING CONSIDERATIONS – PIC16C56/CR56, PIC16C57/CR57 AND PIC16C58/CR58

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS Register will not be updated. Therefore, the next `GOTO`, `CALL` or modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA<1:0>).

For example, a `NOP` at location 1FFh (page 0) increments the PC to 200h (page 1). A `GOTO xxx` at 200h will return the program to address xxh on page 0 (assuming that PA<1:0> are clear).

To prevent this, the page preselect bits must be updated under program control.

6.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the RESET vector).

The STATUS Register page preselect bits are cleared upon a RESET, which means that page 0 is preselected.

Therefore, upon a RESET, a `GOTO` instruction at the RESET vector location will automatically cause the program to jump to page 0.

6.6 Stack

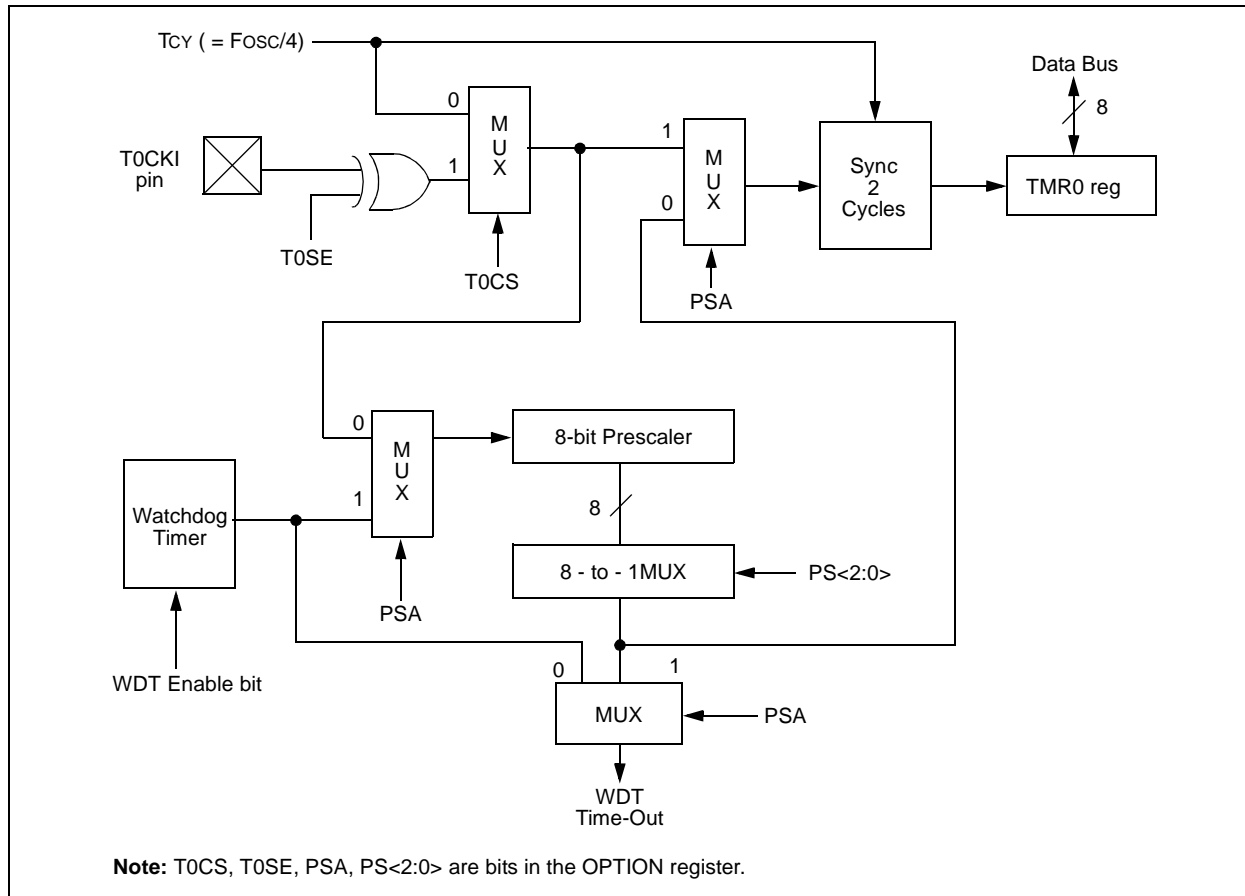
PIC16C5X devices have a 10-bit or 11-bit wide, two-level hardware push/pop stack.

A `CALL` instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential `CALL`'s are executed, only the most recent two return addresses are stored.

A `RETLW` instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential `RETLW`'s are executed, the stack will be filled with the address previously stored in level 2. Note that the W Register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the `RETLW` instruction, the PC is loaded with the Top of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC, therefore, paging is not an issue when returning from a subroutine.

FIGURE 8-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



CALL		Subroutine Call				
Syntax:	[<i>label</i>] CALL k					
Operands:	0 ≤ k ≤ 255					
Operation:	(PC) + 1 → TOS; k → PC<7:0>; (STATUS<6:5>) → PC<10:9>; 0 → PC<8>					
Status Affected:	None					
Encoding:	<table border="1"><tr><td>1001</td><td>kkkk</td><td>kkkk</td></tr></table>			1001	kkkk	kkkk
1001	kkkk	kkkk				
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two-cycle instruction.					
Words:	1					
Cycles:	2					
Example:	HERE CALL THERE					
Before Instruction						
PC = address (HERE)						
After Instruction						
PC = address (THERE)						
TOS = address (HERE + 1)						

CLRF	Clear f			
Syntax:	[<i>label</i>] CLRF f			
Operands:	$0 \leq f \leq 31$			
Operation:	00h \rightarrow (f); 1 \rightarrow Z			
Status Affected:	Z			
Encoding:	<table border="1"><tr><td>0000</td><td>011f</td><td>ffff</td></tr></table>	0000	011f	ffff
0000	011f	ffff		
Description:	The contents of register 'f' are cleared and the Z bit is set.			
Words:	1			
Cycles:	1			
Example:	CLRF FLAG_REG			
Before Instruction				
FLAG_REG	= 0x5A			
After Instruction				
FLAG_REG	= 0x00			
Z	= 1			

CLR W				
Syntax:	[<i>label</i>] CLRW			
Operands:	None			
Operation:	00h → (W); 1 → Z			
Status Affected:	Z			
Encoding:	<table border="1"><tr><td>0000</td><td>0100</td><td>0000</td></tr></table>	0000	0100	0000
0000	0100	0000		
Description:	The W register is cleared. Zero bit (Z) is set.			
Words:	1			
Cycles:	1			
Example:	CLR W			
Before Instruction				
W	= 0x5A			
After Instruction				
W	= 0x00			
Z	= 1			

CLRWD		Clear Watchdog Timer				
Syntax:	[<i>label</i>] CLRWD					
Operands:	None					
Operation:	00h → WDT; 0 → WDT prescaler (if assigned); 1 → \overline{TO} ; 1 → \overline{PD}					
Status Affected:	\overline{TO} , \overline{PD}					
Encoding:	<table border="1"><tr><td>0000</td><td>0000</td><td>0100</td></tr></table>			0000	0000	0100
0000	0000	0100				
Description:	The CLRWD instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits \overline{TO} and \overline{PD} are set.					
Words:	1					
Cycles:	1					
Example:	CLRWD					
Before Instruction						
WDT counter		=	?			
After Instruction						
WDT counter		=	0x00			
WDT prescaler		=	0			
\overline{TO}		=	1			
\overline{PD}		=	1			

13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 PIC16LCR54A-04I (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
PIC16CR54A-04, 10, 20 PIC16CR54A-04I, 10I, 20I (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
	IPD	Power-down Current⁽²⁾					
D006		PIC16LCR54A-Commercial	—	1.0	6.0	μA	V _{DD} = 2.5V, WDT disabled
			—	2.0	8.0*	μA	V _{DD} = 4.0V, WDT disabled
			—	3.0	15	μA	V _{DD} = 6.0V, WDT disabled
			—	5.0	25	μA	V _{DD} = 6.0V, WDT enabled
D006A		PIC16CR54A-Commercial	—	1.0	6.0	μA	V _{DD} = 2.5V, WDT disabled
			—	2.0	8.0*	μA	V _{DD} = 4.0V, WDT disabled
			—	3.0	15	μA	V _{DD} = 6.0V, WDT disabled
			—	5.0	25	μA	V _{DD} = 6.0V, WDT enabled
D007		PIC16LCR54A-Industrial	—	1.0	8.0	μA	V _{DD} = 2.5V, WDT disabled
			—	2.0	10*	μA	V _{DD} = 4.0V, WDT disabled
			—	3.0	20*	μA	V _{DD} = 4.0V, WDT enabled
			—	3.0	18	μA	V _{DD} = 6.0V, WDT disabled
			—	5.0	45	μA	V _{DD} = 6.0V, WDT enabled
D007A		PIC16CR54A-Industrial	—	1.0	8.0	μA	V _{DD} = 2.5V, WDT disabled
			—	2.0	10*	μA	V _{DD} = 4.0V, WDT disabled
			—	3.0	20*	μA	V _{DD} = 4.0V, WDT enabled
			—	3.0	18	μA	V _{DD} = 6.0V, WDT disabled
			—	5.0	45	μA	V _{DD} = 6.0V, WDT enabled

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all I_{DD} measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS}, T_{0CKI} = V_{DD}, MCLR = V_{DD}; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through R_{EXT}. The current through the resistor can be estimated by the formula: I_R = V_{DD}/2R_{EXT} (mA) with R_{EXT} in kΩ.

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13.2 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

PIC16CR54A-04E, 10E, 20E (Extended)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage RC, XT and LP modes HS mode	3.25 4.5	— —	6.0 5.5	V V	
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current ⁽²⁾ RC ⁽³⁾ and XT modes HS mode HS mode	— — —	1.8 4.8 9.0	3.3 10 20	mA mA mA	FOSC = 4.0 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 16 MHz, VDD = 5.5V
D020	IPD	Power-down Current ⁽²⁾	— —	5.0 0.8	22 18	μA μA	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: $I_R = VDD/2R_{EXT}$ (mA) with REXT in kΩ.

FIGURE 14-19: PORTA, B AND C I_{OH} vs. V_{OH}, V_{DD} = 3 V

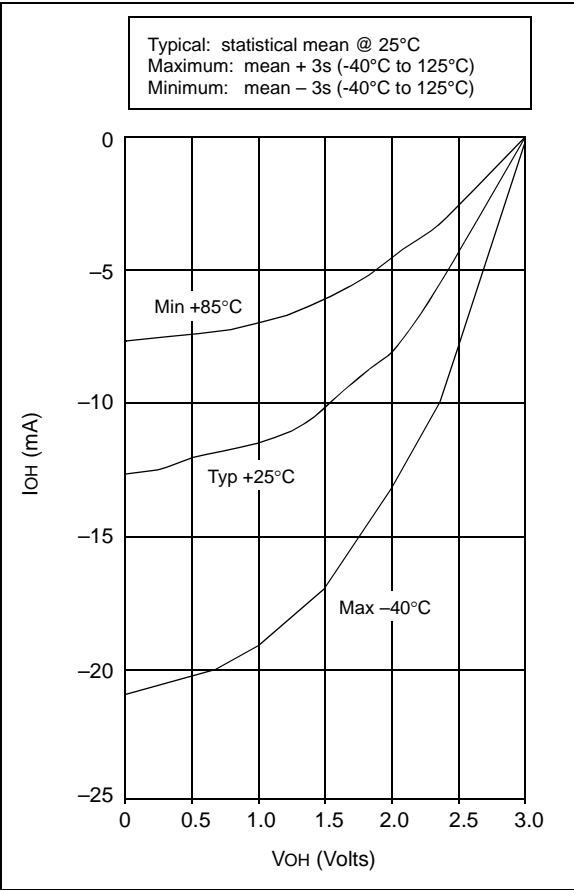
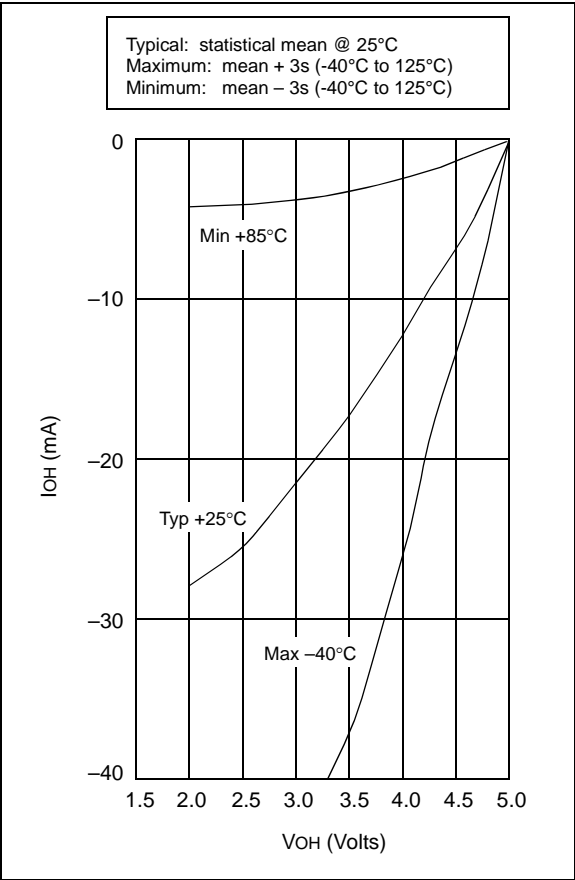


FIGURE 14-20: PORTA, B AND C I_{OH} vs. V_{OH}, V_{DD} = 5 V



15.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings^(†)

Ambient temperature under bias	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on MCLR with respect to VSS.....	0 to +14V
Voltage on all other pins with respect to VSS	–0.6V to (VDD + 0.6V)
Total power dissipation ⁽¹⁾	800 mW
Max. current out of Vss pin	150 mA
Max. current into VDD pin	100 mA
Max. current into an input pin (T0CKI only)	±500 µA
Input clamp current, I _{IK} (V _I < 0 or V _I > VDD).....	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > VDD)	±20 mA
Max. output current sunk by any I/O pin	25 mA
Max. output current sourced by any I/O pin	20 mA
Max. output current sourced by a single I/O port (PORTA or B)	50 mA
Max. output current sunk by a single I/O port (PORTA or B)	50 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

15.5 Timing Parameter Symbolology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T	T
F Frequency	Time

Lowercase letters (pp) and their meanings:

pp	
2 to	mc MCLR
ck CLKOUT	osc oscillator
cy cycle time	os OSC1
drt device reset timer	t0 T0CKI
io I/O port	wdt watchdog timer

Uppercase letters and their meanings:

S	P Period
F Fall	R Rise
H High	V Valid
I Invalid (Hi-impedance)	Z Hi-impedance
L Low	

FIGURE 15-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54A

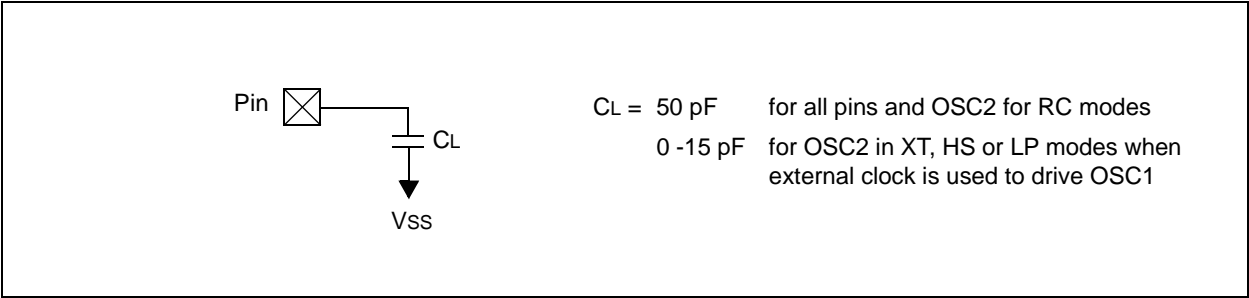


FIGURE 16-16: WDT TIMER TIME-OUT PERIOD vs. VDD⁽¹⁾

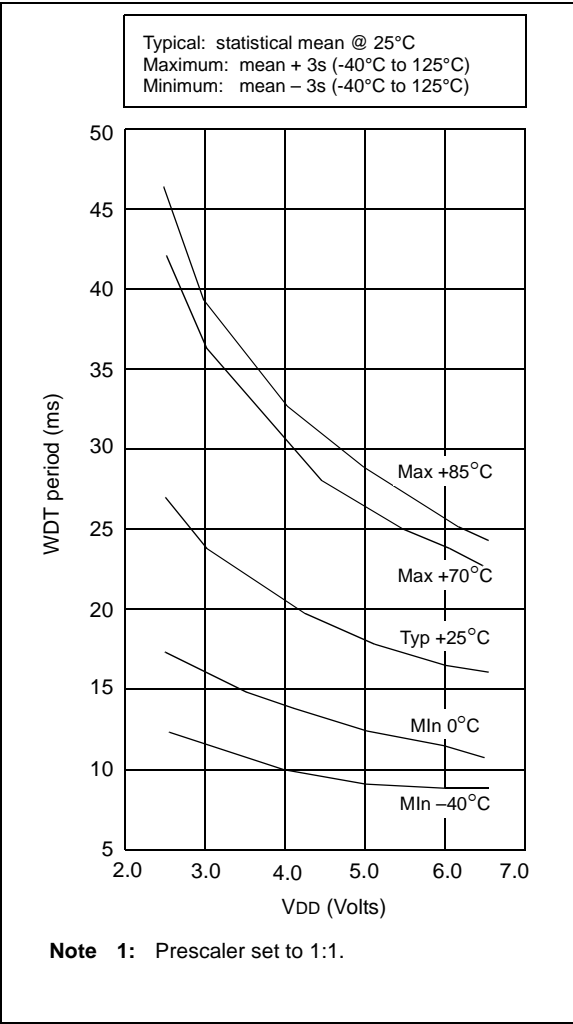
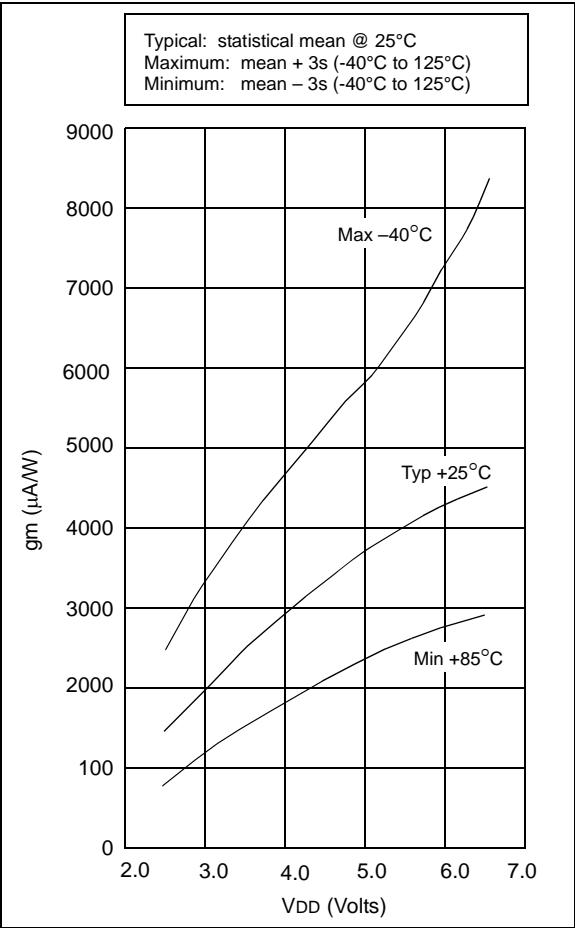


FIGURE 16-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD



PIC16C5X

FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF, 25°C

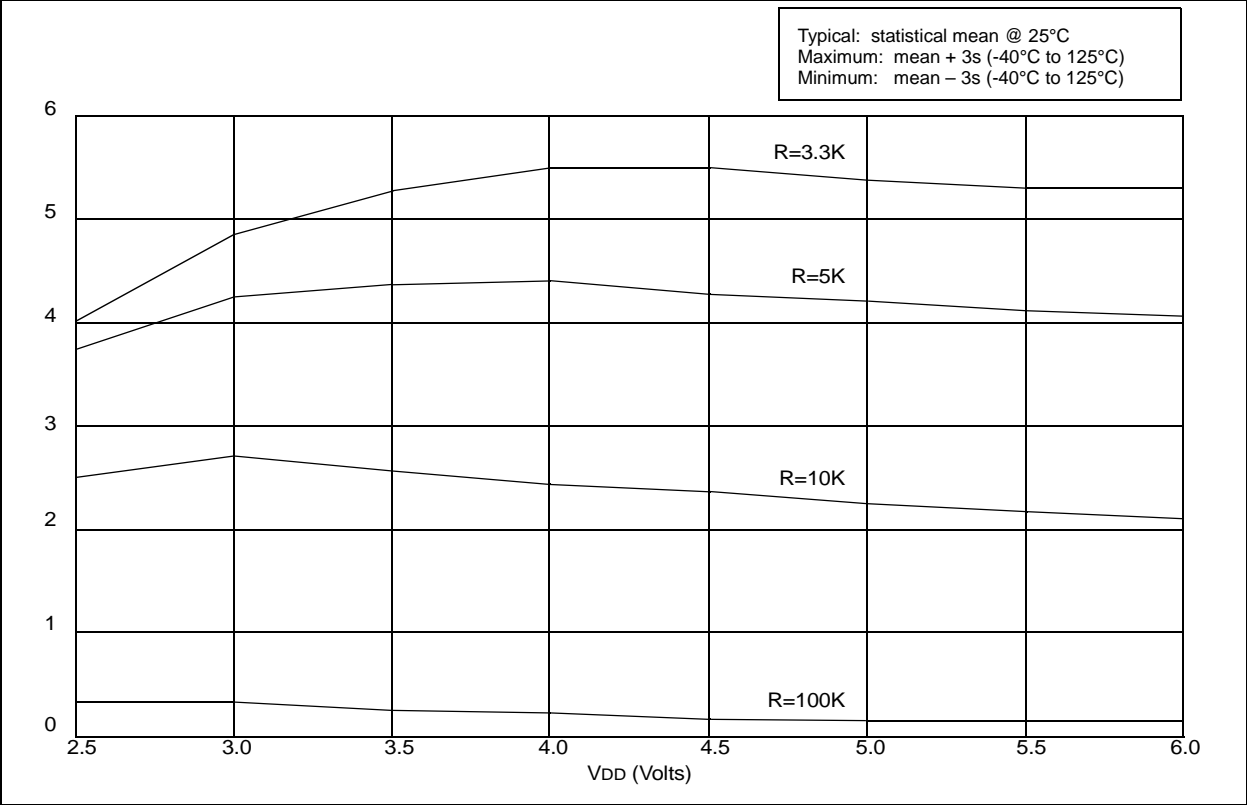


FIGURE 18-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF, 25°C

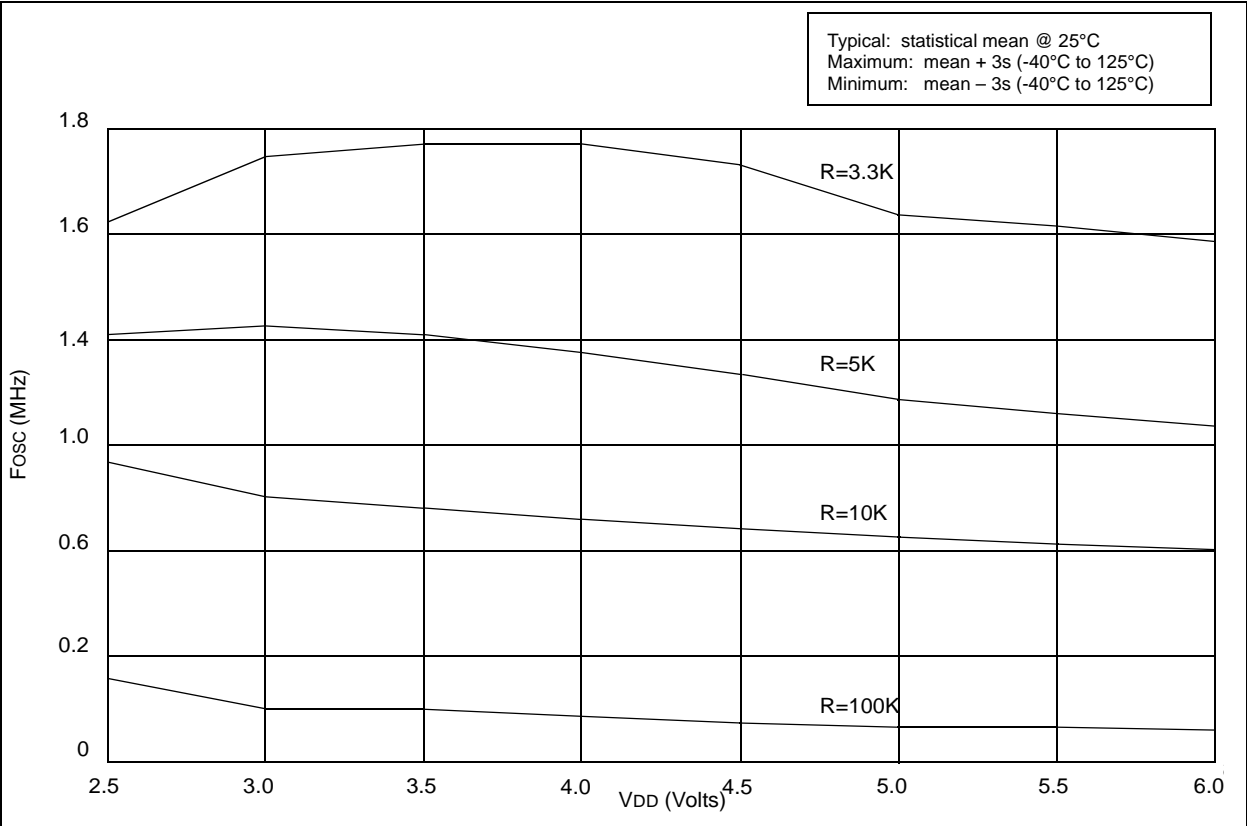


FIGURE 18-8: V_{TH} (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. V_{DD}

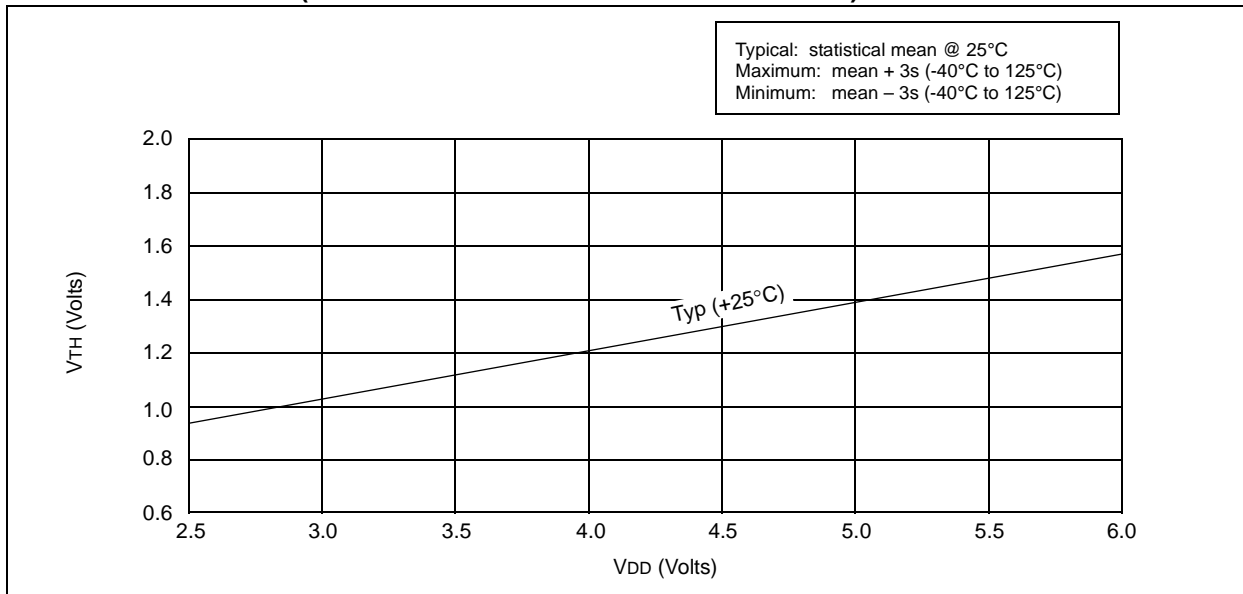


FIGURE 18-9: V_{IH} , V_{IL} OF \overline{MCLR} , $T0CKI$ AND $OSC1$ (IN RC MODE) vs. V_{DD}

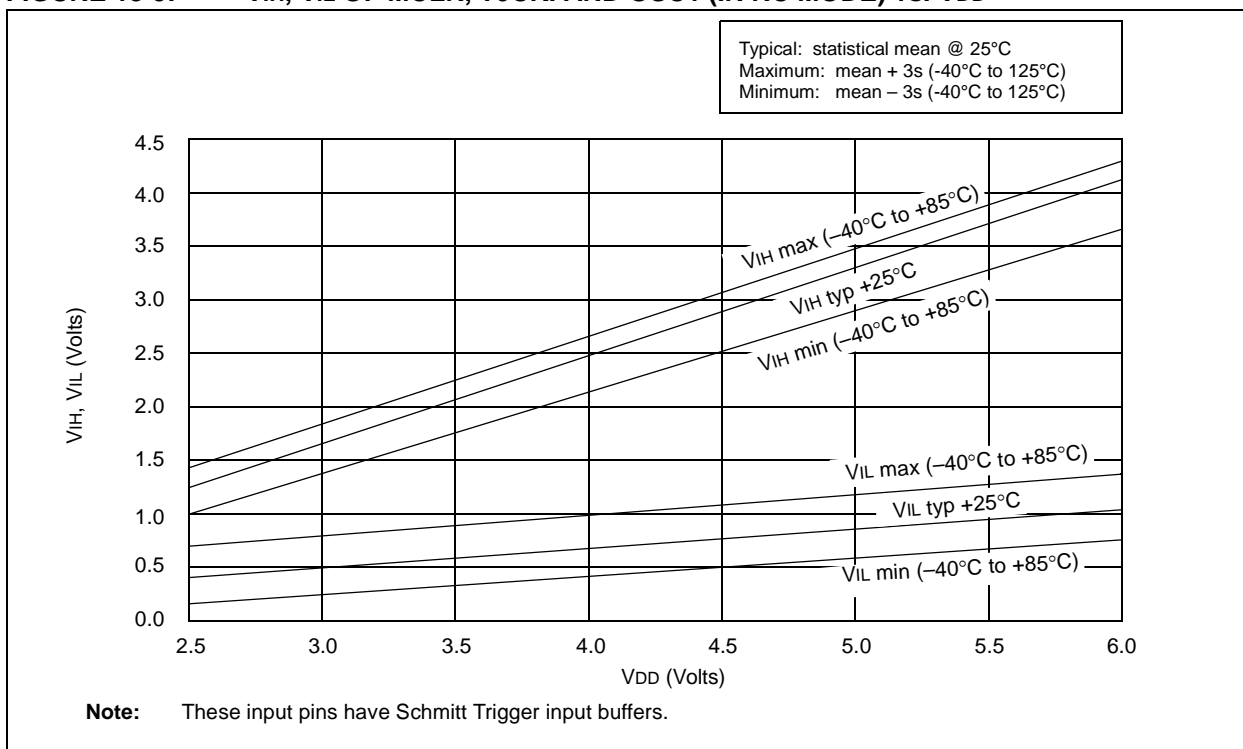


FIGURE 18-10: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (IN XT, HS AND LP MODES) vs. VDD

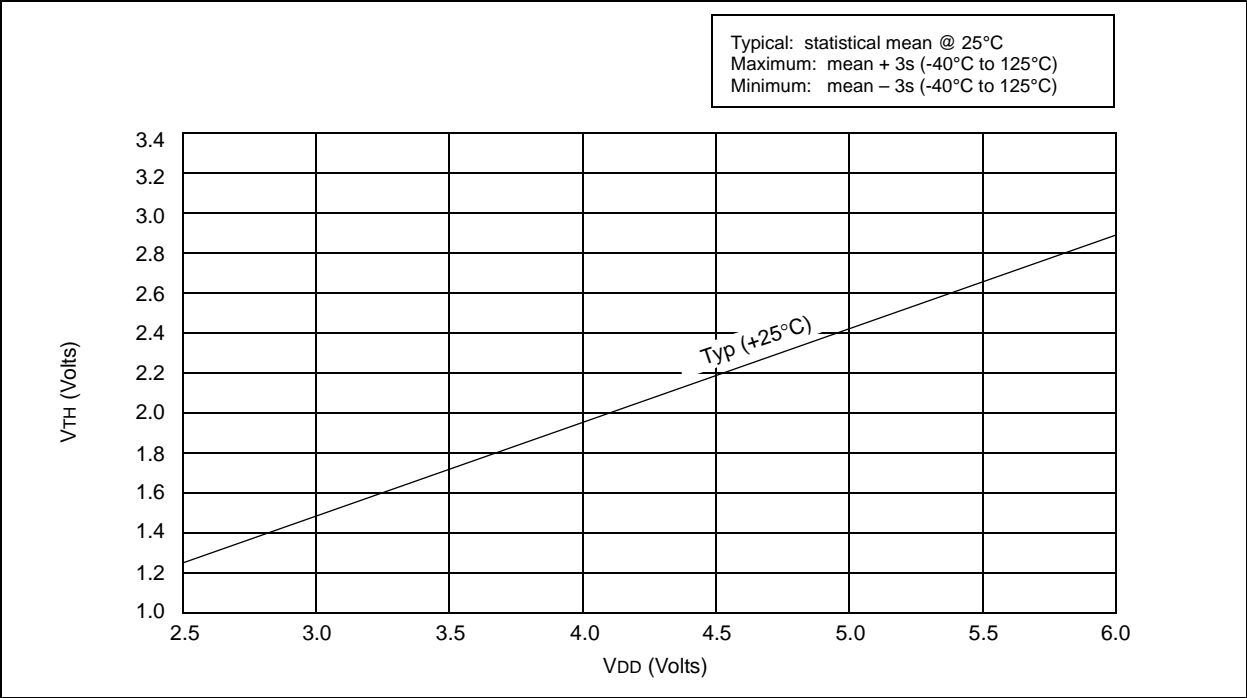
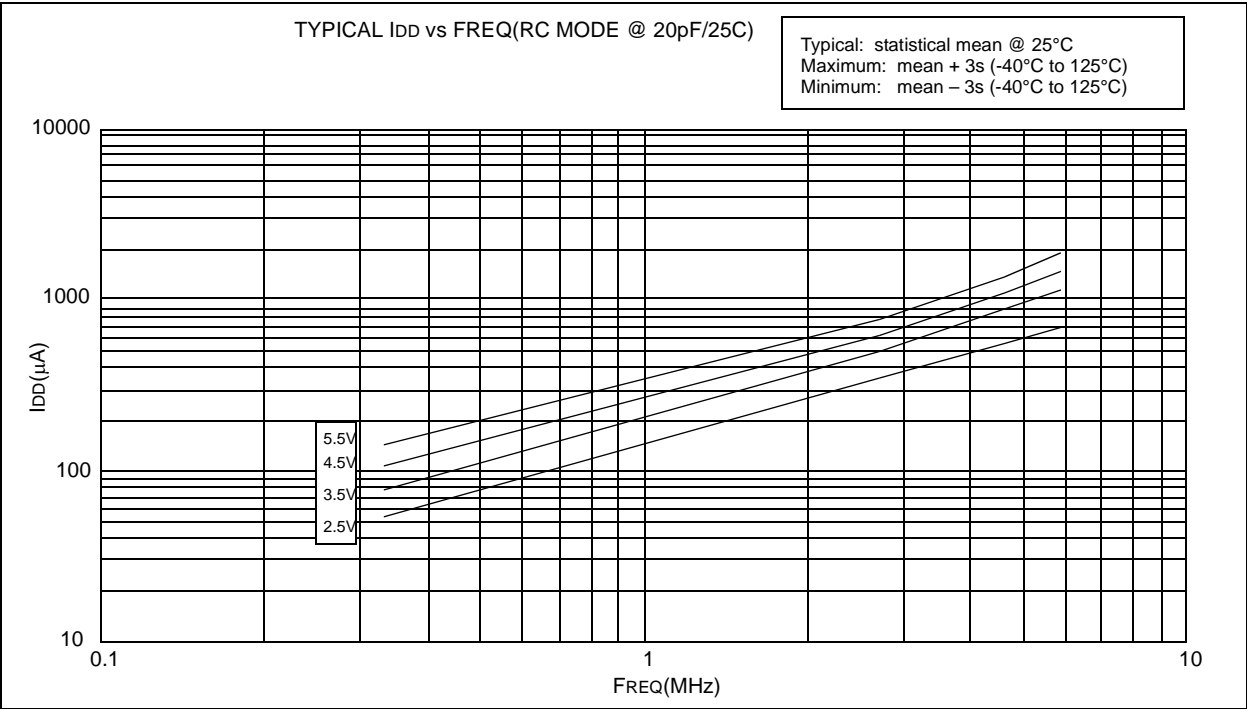


FIGURE 18-11: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, 25°C)



19.0 ELECTRICAL CHARACTERISTICS - PIC16LC54C 40MHz

Absolute Maximum Ratings^(†)

Ambient temperature under bias	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS.....	0 to +14V
Voltage on all other pins with respect to VSS	–0.6V to (VDD + 0.6V)
Total power dissipation ⁽¹⁾	800 mW
Max. current out of Vss pin	150 mA
Max. current into VDD pin	100 mA
Max. current into an input pin (T0CKI only)	±500 μ A
Input clamp current, I _{IK} (V _I < 0 or V _I > VDD).....	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > VDD)	±20 mA
Max. output current sunk by any I/O pin	25 mA
Max. output current sourced by any I/O pin	20 mA
Max. output current sourced by a single I/O (Port A, B or C)	50 mA
Max. output current sunk by a single I/O (Port A, B or C).....	50 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

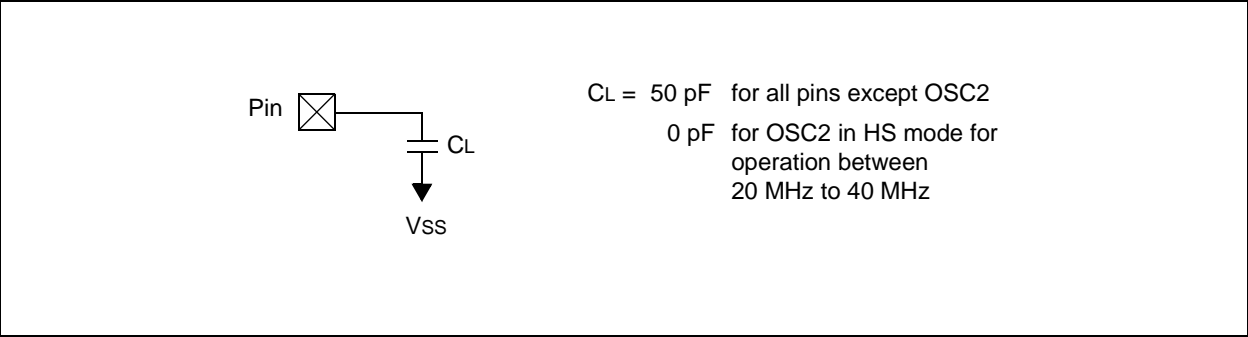
19.3 Timing Parameter Symbolology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

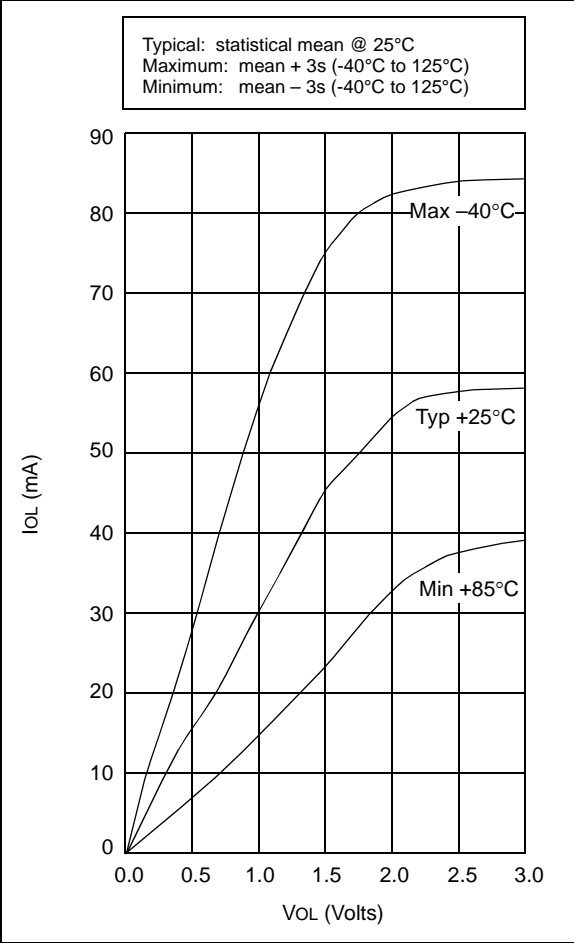
T		T	Time
F	Frequency		
Lowercase letters (pp) and their meanings:			
pp		mc	MCLR
2	to	osc	oscillator
ck	CLKOUT	os	OSC1
cy	cycle time	t0	T0CKI
drt	device reset timer	wdt	watchdog timer
io	I/O port		
Uppercase letters and their meanings:			
S		P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	Hi-impedance
L	Low		

FIGURE 19-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54C/C55A/C56A/C57C/C58B-40



PIC16C5X

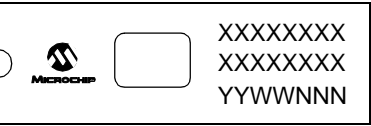
FIGURE 20-9: I_{OL} vs. V_{OL} , $V_{DD} = 5\text{ V}$



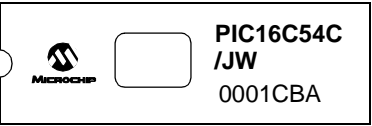
PIC16C5X

Package Marking Information (Cont'd)

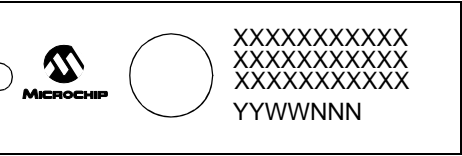
18-Lead Cerdip Windowed



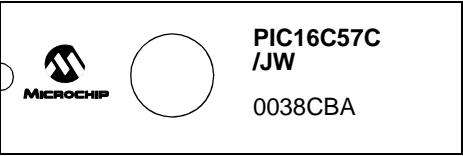
Example



28-Lead Cerdip Windowed



Example



Legend:

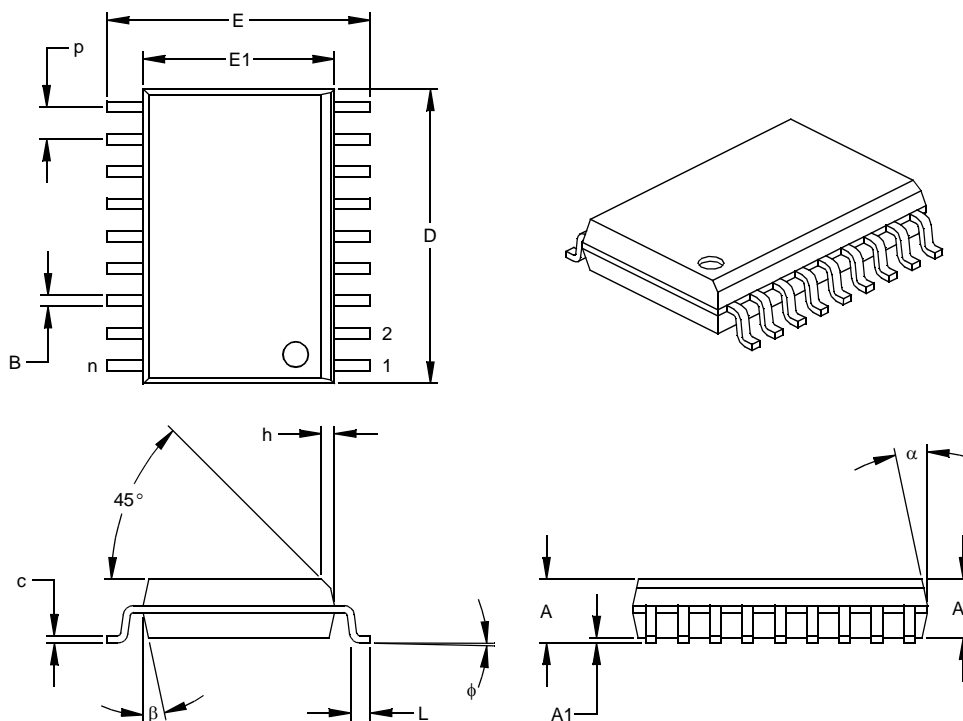
XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

PIC16C5X

18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-013

Drawing No. C04-051