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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c54t-xti-so

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6.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 6-1).

The Special Registers can be classified into two sets. The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Details on Page
N/A	TRIS	I/O Cont	I/O Control Registers (TRISA, TRISB, TRISC)						1111 1111	35	
N/A	OPTION	Contains	s control b	oits to cor	figure Ti	mer0 and	Timer0/V	VDT pres	caler	11 1111	30
00h	INDF	Uses co	Uses contents of FSR to address data memory (not a physical register)					egister)	XXXX XXXX	32	
01h	TMR0	Timer0 I	Timer0 Module Register							XXXX XXXX	38
02h ⁽¹⁾	PCL	Low ord	Low order 8 bits of PC							1111 1111	31
03h	STATUS	PA2	PA1	PA0	TO	PD	Z	DC	С	0001 1xxx	29
04h	FSR	Indirect	Indirect data memory address pointer					1xxx xxxx (3)	32		
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	xxxx	35
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	XXXX XXXX	35
07h ⁽²⁾	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	XXXX XXXX	35

|--|

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 6.5 for an explanation of how to access these bits.

2: File address 07h is a General Purpose Register on the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16CR58 and PIC16CR58.

3: These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for MCLR and WDT Reset, the value is 111u uuuu.

6.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not

writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as $000u \ u1uu$ (where u = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 10.0, Instruction Set Summary.

REGISTER 6-1: STATUS REGISTER (ADDRESS: 03h)

	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
	PA2	PA1	PA0	TO	PD	Z	DC	С
	bit 7							bit 0
bit 7:	PA2: This bi	t unused at th	is time.					
	Use of the P. compatibility	A2 bit as a ge with future pr	neral purpos oducts.	e read/write k	oit is not recor	nmended, sin	ice this may a	ffect upward
bit 6-5:	PA<1:0> : Pr	ogram page p	preselect bits	(PIC16C56/0	CR56)(PIC16	C57/CR57)(P	IC16C58/CR5	58)
	00 = Page 0	(000h - 1FFh) - PIC16C56	6/CR56, PIC1	6C57/CR57,	PIC16C58/C	R58	
	01 = Page 1	(200h - 3FFh) - PIC16C5	6/CR56, PIC1	6C57/CR57,	PIC16C58/C	R58	
	10 = Page 2 11 = Page 3	. (400h - 3FFh . (600h - 7FFh) - PIC16C5	7/CR57, PIC1	16C58/CR58			
	Each page is	s 512 words.	.,	., e ,				
	Using the PA	A<1:0> bits as	general purp	oose read/wri	te bits in devi	ces which do	not use them	for program
1.1.4	page presele	ect is not reco	mmended si	nce this may	affect upward	l compatibility	with future pr	oducts.
Dit 4:	IO: Time-ou	it dit						
	1 = After power of the second secon	ime-out occur	T instruction	I, OF SLEEP IF	Istruction			
bit 3:	PD: Power-c	down bit						
	1 = After power-up or by the CLRWDT instruction							
	0 = By execution of the SLEEP instruction							
bit 2:	Z: Zero bit							
	1 = The result of an arithmetic or logic operation is zero							
bit 1.	D = The lest	$\frac{1}{100}$ $\frac{1}$	(for ADDWE 2		tructions)			
DIC 1.			(IOI ADDWF a		silucions			
	1 = A carry f	rom the 4th lo	w order bit o	f the result of	ccurred			
	0 = A carry f	rom the 4th lo	w order bit o	f the result di	d not occur			
	SUBWF	from the Ath	low order bit	of the requit	did not occur			
	1 = A borrow 0 = A borrow	v from the 4th	low order bit	of the result	occurred			
bit 0:	C: Carry/bor	row bit (for AD	DWF, SUBWF	and RRF, RLI	F instructions))		
	ADDWF		SUBW	/F		RRF or RLF		
	1 = A carry c	bccurred	1 = A	borrow did no	ot occur red	Loaded with	LSb or MSb,	respectively
	v = A carry c		0 = A I					
Lenendi								

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

6.5 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.

For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0> (Figure 6-7, Figure 6-8 and Figure 6-9).

For the PIC16C56, PIC16CR56, PIC16C57, PIC16CR57, PIC16C58 and PIC16CR58, a page number must be supplied as well. Bit5 and bit6 of the STA-TUS Register provide page information to bit9 and bit10 of the PC (Figure 6-8 and Figure 6-9).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 6-7 and Figure 6-8).

Instructions where the PCL is the destination, or modify PCL instructions, include MOVWF PCL, ADDWF PCL, and BSF PCL, 5.

For the PIC16C56, PIC16CR56, PIC16C57, PIC16CR57, PIC16C58 and PIC16CR58, a page number again must be supplied. Bit5 and bit6 of the STA-TUS Register provide page information to bit9 and bit10 of the PC (Figure 6-8 and Figure 6-9).

Note:	Because PC<8> is cleared in the CALL instruction, or any modify PCL instruction,
	limited to the first 256 locations of any pro-
	gram memory page (512 words long).

FIGURE 6-7: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C54, PIC16CR54, PIC16C55



FIGURE 6-8:

LOADING OF PC BRANCH INSTRUCTIONS - PIC16C56/PIC16CR56



FIGURE 6-9:

LOADING OF PC BRANCH INSTRUCTIONS - PIC16C57/PIC16CR57, AND PIC16C58/ PIC16CR58



7.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., MOVF PORTB, W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

7.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used (RA<3:0>). Bits 7-4 are unimplemented and read as '0's.

7.2 PORTB

PORTB is an 8-bit I/O Register (PORTB<7:0>).

7.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16CR56, PIC16CR56, PIC16CS8 and PIC16CR58.

7.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the TRIS f instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

Note:	A read of the ports reads the pins, not the					
	output data latches. That is, if an output					
	driver on a pin is enabled and driven high,					
	but the external system is holding it low, a					
	read of the port will indicate that the pin is					
	low.					

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

TABLE 7-1:	SUMMARY O	F PORT	REGISTERS
			LOIOI LIVO

Value on Value on Bit 4 Bit 3 Bit 1 Bit 0 MCLR and Address Name Bit 7 Bit 6 Bit 5 Bit 2 Power-On Reset WDT Reset TRIS N/A I/O Control Registers (TRISA, TRISB, TRISC) 1111 1111 1111 1111 05h PORTA RA3 RA2 RA1 RA0 _ _ _ _ xxxx _ _ _ _ uuuu PORTB 06h RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0 XXXX XXXX uuuu uuuu 07h PORTC RC7 RC6 RC5 RC4 RC3 RC2 RC1 RC0 XXXX XXXX uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'

7.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 7-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

FIGURE 7-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of realtime applications. The PIC16C5X family of microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator Selection (Section 4.0)
- RESET (Section 5.0)
- Power-On Reset (Section 5.1)
- Device Reset Timer (Section 5.2)
- Watchdog Timer (WDT) (Section 9.2)
- SLEEP (Section 9.3)
- Code protection (Section 9.4)
- ID locations (Section 9.5)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in RESET until the crystal oscillator is stable. With this timer on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake up from SLEEP through external RESET or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

10.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 10-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers in that bank is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 10-1:	OPCODE FIELD
	DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x1F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1)
	The assembler will generate code with $x = 0$.
	It is the recommended form of use for com-
	patibility with all Microchip software tools.
d	Destination select;
	d = 0 (store result in W)
	d = 1 (store result in file register 'f')
	Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
TO	Time-out bit
PD	Power-down bit
dest	Destination, either the W register or the
	specified register file location
[]	Options
()	Contents
\rightarrow	Assigned to
< >	Register bit field
E	In the set of
italics	User defined term (font is courier)

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time would be 1 μ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time would be 2 μ s.

Figure 10-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations					
<u>11 6</u>	5	4 0			
OPCODE	d	f (FILE #)			
d = 0 for destination W d = 1 for destination f f = 5-bit file register address					
Bit-oriented file register	r ope	erations			
11 8	7	5 4 0			
OPCODE	b (Bl	IT #) f (FILE #)			
 f = 5-bit file register address Literal and control operations (except GOTO) 					
<u>11</u>	8	7 0			
OPCODE		k (literal)			
k = 8-bit immediate value					
Literal and control operations - GOTO instruction					
11	9	8 0			
OPCODE k (literal)					
k = 9-bit immediate value					

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GOTO	Unconditional Branch				
Syntax:	[label]	GOTO	k		
Operands:	$0 \le k \le 511$				
Operation:	$k \rightarrow PC < 8:0>;$ STATUS<6:5> $\rightarrow PC < 10:9>$				
Status Affected:	None				
Encoding:	101k	kkkk	kkkk		
Description:	GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two- cycle instruction.				
Words:	1				
Cycles:	2				
Example:	GOTO TH	IERE			
After Instructi PC =	on address	G (THER	E)		

INCF	Increment f
Syntax:	[label] INCF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$
Operation:	(f) + 1 \rightarrow (dest)
Status Affected:	Z
Encoding:	0010 10df ffff
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
Words:	1
Cycles:	1
Example:	INCF CNT, 1
Before Instru CNT Z After Instructi CNT Z	ction = 0xFF = 0 ion = 0x00 = 1

INCFSZ	Increment f, Skip if 0					
Syntax:	[label] INCFSZ f,d					
Operands:	$\begin{array}{l} 0\leq f\leq 31\\ d\in [0,1] \end{array}$					
Operation:	(f) + 1 \rightarrow (dest), skip if result = 0					
Status Affected:	None					
Encoding:	0011 11df ffff					
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-					
Words:	1					
Cycles:	1(2)					
Example:	HERE INCFSZ CNT, 1 GOTO LOOP					
	CONTINUE • • •					
Before Instru	iction					
PC	= address (HERE)					
After Instruct	ion					
CNT	= CNT + 1;					
if CNT	= 0,					
PC	= address (CONTINUE);					
if CNT	≠ 0, 					
PC	= address (HERE +1)					

MOVWF	Move W to f								
Syntax:	[label]	MOVWF	f						
Operands:	$0 \le f \le 31$								
Operation:	$(W) \rightarrow (f)$								
Status Affected:	None								
Encoding:	0000	001f	ffff						
Description:	Move data from the W register to register 'f'.								
Words:	1								
Cycles:	1								
Example:	MOVWF	TEMP_RE	lG						
Before Instru TEMP_F W After Instructi TEMP_F W	ction REG = on REG = =	0xFF 0x4F 0x4F 0x4F 0x4F							

NOP	No Operation					
Syntax:	[label]	NOP				
Operands:	None					
Operation:	No opera	ation				
Status Affected:	None					
Encoding:	0000	0000	0000]		
Description:	No opera	ation.		-		
Words:	1					
Cycles:	1					
Example:	NOP					

OPTION	Load OPTION Register								
Syntax:	[label]	OPTIO	N						
Operands:	None								
Operation:	$(W) \rightarrow OPTION$								
Status Affected:	None								
Encoding:	0000	0000	0010						
Description:	The cont loaded in	tent of the	e W regis PTION re	ter is gister.					
Words:	1								
Cycles:	1								
Example	OPTION								
Before Instrue	ction								
W	= 0x07								
After Instructi	on								
OPTION	= 0x07								

RETLW	Return w	ith Liter	al in W					
Syntax:	[label]	RETLW	k					
Operands:	$0 \leq k \leq 25$	5						
Operation:	$k \rightarrow (W);$ TOS $\rightarrow P$	С						
Status Affected:	None							
Encoding:	1000	kkkk	kkkk					
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.							
Words:	1							
Cycles:	2							
Example:	CALL TAN	BLE ;W ;tal ;val ;W r ;val	contair ole offs lue. now has lue.	ns set table				
TABLE	ADDWF PC RETLW k: RETLW k:	C ;W = 1 ;Beg 2 ; n ; En	= offset gin tabl nd of ta	le le able				
Before Instru	ction							
W	= 0x0)7						
After Instruct	ion .	(1.5						
VV	= valu	ue of k8						

11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for precompiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

11.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multiproject software development tool.

11.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft[®] Windows environment were chosen to best make these features available to you, the end user.

11.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

12.2 DC Characteristics: PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial				
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions
D001	Vdd	Supply Voltage PIC16C5X-RCI PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-HSI	3.0 3.0 4.5 4.5		6.25 6.25 5.5 5.5 6.25	V V V V	
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	2.5	1.5*		V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current ⁽²⁾ PIC16C5X-RCI ⁽³⁾ PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-HSI PIC16C5X-LPI		1.8 1.8 4.8 9.0 15	3.3 3.3 10 10 20 40	mA mA mA mA μA	Fosc = 4 MHz, VDD = $5.5V$ Fosc = 4 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 20 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $3.0V$, WDT disabled
D020	IPD	Power-down Current ⁽²⁾	_	4.0 0.6	14 12	μΑ μΑ	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

- † Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

AC Chara	cteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions	
1	Tosc	External CLKIN Period ⁽¹⁾	250			ns	XT OSC mode	
			100		—	ns	10 MHz mode	
			50		—	ns	HS OSC mode (Comm/Ind)	
			62.5		—	ns	HS OSC mode (Ext)	
			25		—	μS	LP OSC mode	
		Oscillator Period ⁽¹⁾	250	—	—	ns	RC OSC mode	
			250		10,000	ns	XT OSC mode	
			100		250	ns	10 MHz mode	
			50		250	ns	HS OSC mode (Comm/Ind)	
			62.5		250	ns	HS OSC mode (Ext)	
			25		—	μS	LP OSC mode	
2	Тсу	Instruction Cycle Time ⁽²⁾	—	4/Fosc	—	—		
3	TosL,	Clock in (OSC1) Low or High	85*	—	—	ns	XT oscillator	
	TosH	Time	20*	—	—	ns	HS oscillator	
			2.0*		—	μS	LP oscillator	
4	TosR,	Clock in (OSC1) Rise or Fall	—	_	25*	ns	XT oscillator	
	TosF	Time	—	—	25*	ns	HS oscillator	
			—	—	50*	ns	LP oscillator	

TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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14.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.





TABLE 14-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Average Fosc @ 5 V, 25°C				
20 pF	3.3K	5 MHz	± 27%			
	5K	3.8 MHz	± 21%			
	10K	2.2 MHz	± 21%			
	100K	262 kHz	± 31%			
100 pF	3.3K	1.6 MHz	± 13%			
	5K	1.2 MHz	± 13%			
	10K	684 kHz	± 18%			
	100K	71 kHz	± 25%			
300 pF	3.3K	660 kHz	± 10%			
	5.0K	484 kHz	± 14%			
	10K	267 kHz	± 15%			
	100K	29 kHz	± 19%			

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviations from the average value for VDD = 5V.



FIGURE 14-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED



FIGURE 14-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED



FIGURE 14-7: T

TYPICAL IPD vs. VDD, WATCHDOG ENABLED



FIGURE 14-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED



IPD, with WDT enabled, has two components: The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At -40° C, the latter dominates explaining the apparently anomalous behavior.



FIGURE 16-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD



17.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial) PIC16C5X PIC16CR5X (Commercial, Industrial)				Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrialStandard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial					
Param No.	Symbol	Characteristic/Device	Min Typ† Max Units Conditions				Conditions		
	Vdd	Supply Voltage							
D001		PIC16LC5X	2.5 2.7 2.5		5.5 5.5 5.5	V V V	$\begin{array}{l} -40^{\circ}C \leq TA \leq +\ 85^{\circ}C,\ 16LCR5X \\ -40^{\circ}C \leq TA \leq 0^{\circ}C,\ 16LC5X \\ 0^{\circ}C \leq TA \leq +\ 85^{\circ}C \ 16LC5X \end{array}$		
D001A		PIC16C5X	3.0 4.5		5.5 5.5	V V	RC, XT, LP and HS mode from 0 - 10 MHz from 10 - 20 MHz		
D002	Vdr	RAM Data Retention Volt- age ⁽¹⁾	-	1.5*	-	V	Device in SLEEP mode		
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	_	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	_	V/ms	See Section 5.1 for details on Power-on Reset		

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

17.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial)				ard Ope ting Terr	e rating peratu	Condit ire	ions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial	
PIC16C5X PIC16CR5X (Commercial, Industrial)			Stand Opera	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$				
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions	
	IPD	Power-down Current ⁽²⁾						
D020		PIC16LC5X	—	0.25	2	μΑ	VDD = 2.5V, WDT disabled, Commercial	
			—	0.25	3	μA	VDD = 2.5V, WDT disabled, Industrial	
			_	1 1 25	5	μΑ	VDD = $2.5V$, WDT enabled, Commercial VDD = $2.5V$ WDT enabled Industrial	
		PIC16C5X		0.25	4.0	μ.	$V_{DD} = 3.0V$ WDT disabled Commercial	
DOZOR			_	0.25	5.0	μΑ	$V_{DD} = 3.0V$, W_{DT} disabled, our intercent VDD = 3.0V. WDT disabled. Industrial	
			—	1.8	7.0*	μA	VDD = 5.5V, WDT disabled, Commercial	
			—	2.0	8.0*	μA	VDD = 5.5V, WDT disabled, Industrial	
			—	4	12*	μΑ	VDD = 3.0V, WDT enabled, Commercial	
			—	4	14*	μA	VDD = 3.0V, WDT enabled, Industrial	
			—	9.8	27*	μA	VDD = 5.5V, WDT enabled, Commercial	
			—	12	30*	μA	VDD = 5.5V, WDT enabled, Industrial	

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

19.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)⁽¹⁾

PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)				Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial				
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
D001	Vdd	Supply Voltage	4.5	—	5.5	V	HS mode from 20 - 40 MHz	
D002	Vdr	RAM Data Retention Voltage ⁽²⁾	—	1.5*	—	V	Device in SLEEP mode	
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset	
D004	SVDD	VDD Rise Rate to ensure Power- on Reset	0.05*	—		V/ms	See Section 5.1 for details on Power-on Reset	
D010	IDD	Supply Current ⁽³⁾		5.2 6.8	12.3 16	mA mA	FOSC = 40 MHz, VDD = 4.5V, HS mode FOSC = 40 MHz, VDD = 5.5V, HS mode	
D020	IPD	Power-down Current ⁽³⁾	_	1.8 9.8	7.0 27*	μΑ μΑ	VDD = 5.5V, WDT disabled, Commercial VDD = 5.5V, WDT enabled, Commercial	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- **Note 1:** Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected, HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 19.1.
 - **2:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - **3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

19.3 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS

2. TppS		
Т		
F	Frequency	T Time
Lowercase letters (pp) and their meanings:		
рр		
2	to	mc MCLR
ck	CLKOUT	osc oscillator
су	cycle time	os OSC1
drt	device reset timer	t0 T0CKI
io	I/O port	wdt watchdog timer
Uppercase letters and their meanings:		
S		
F	Fall	P Period
Н	High	R Rise
Ι	Invalid (Hi-impedance)	V Valid
L	Low	Z Hi-impedance

FIGURE 19-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS -PIC16C54C/C55A/C56A/C57C/C58B-40



APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

- 1. Check any CALL, GOTO or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
- 2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change RESET vector to proper value for processor used.
- 6. Remove any use of the ADDLW, RETURN and SUBLW instructions.
- 7. Rewrite any code segments that use interrupts.

APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.