



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c55-10i-ss

7.6 I/O Programming Considerations

7.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 7-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

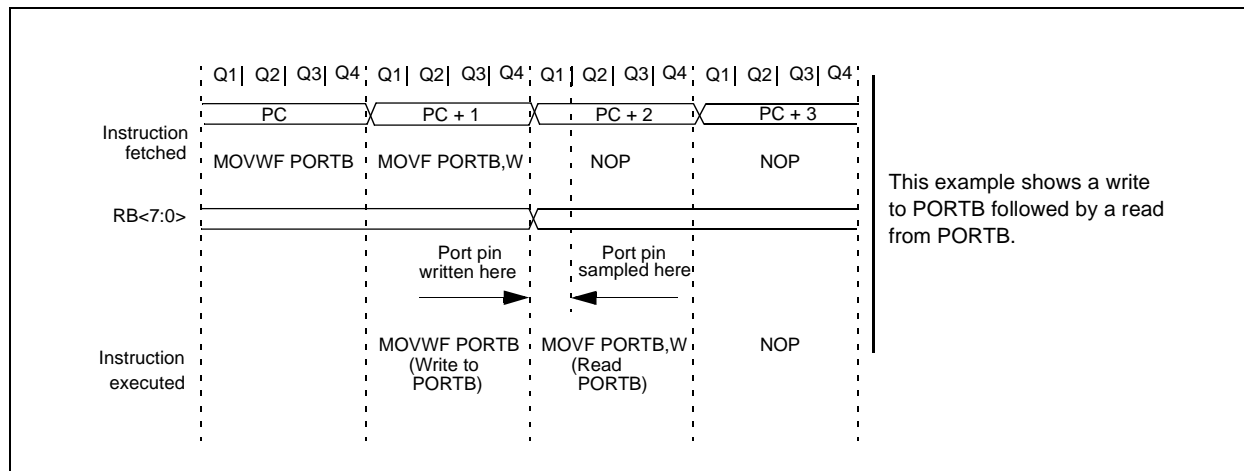
EXAMPLE 7-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;
;          PORT latch  PORT pins
;          -----
BCF  PORTB, 7  ;01pp pppp  11pp pppp
BCF  PORTB, 6  ;10pp pppp  11pp pppp
MOVLW H'3F'    ;
TRIS  PORTB    ;10pp pppp  10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

7.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 7-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 7-2: SUCCESSIVE I/O OPERATION



8.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
 - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
 - Edge select for external clock

Figure 8-1 is a simplified block diagram of the Timer0 module, while Figure 8-2 shows the electrical structure of the Timer0 input.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 8-3 and Figure 8-4). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 8.1.

Note: The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both.

The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 8.2 details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 8-1.

FIGURE 8-1: TIMER0 BLOCK DIAGRAM

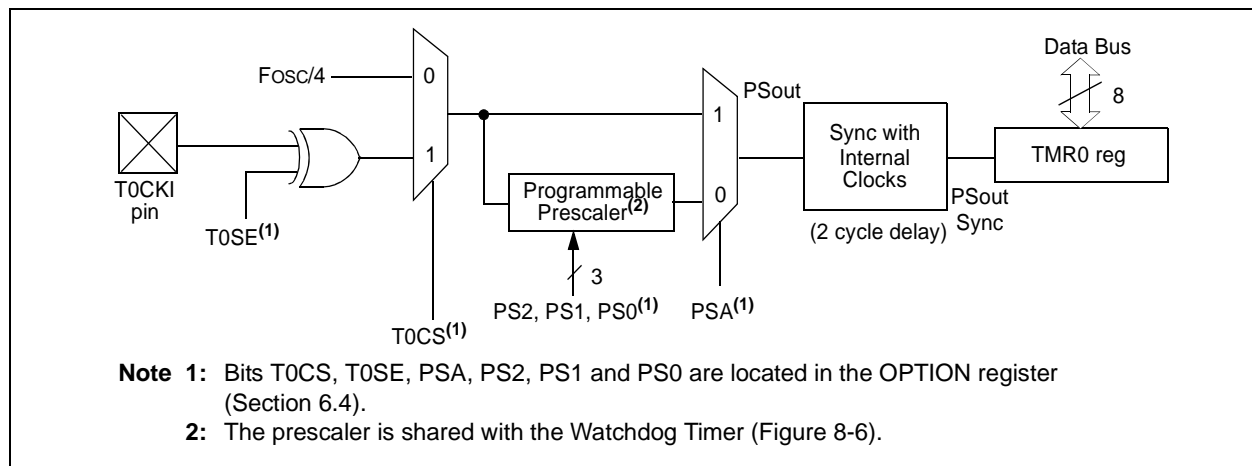
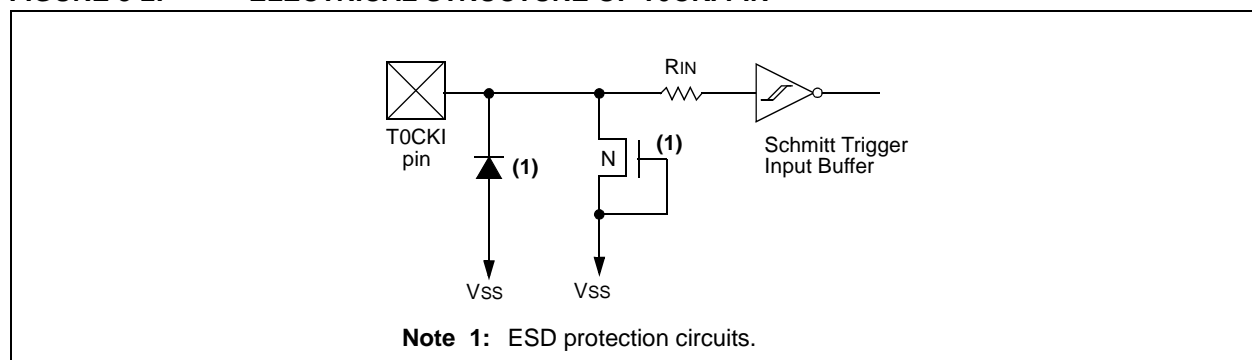


FIGURE 8-2: ELECTRICAL STRUCTURE OF T0CKI PIN



PIC16C5X

FIGURE 8-3: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALER

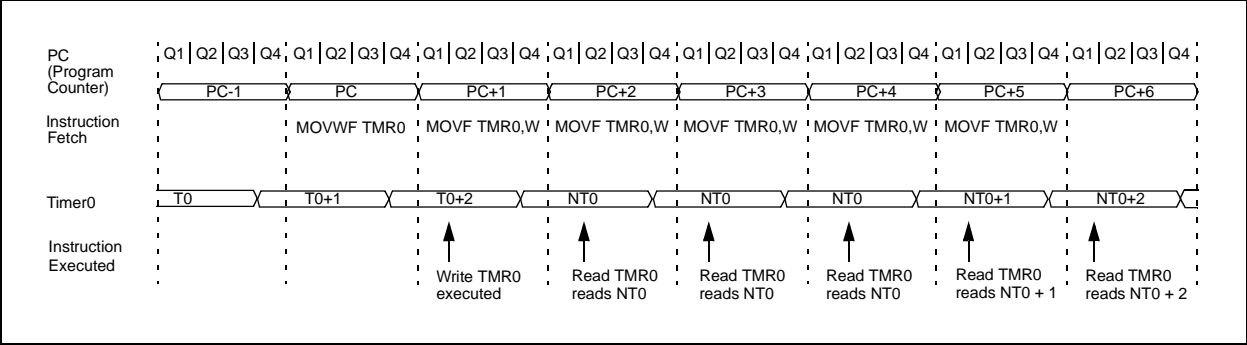


FIGURE 8-4: TIMER0 TIMING: INTERNAL CLOCK/PRESCALER 1:2

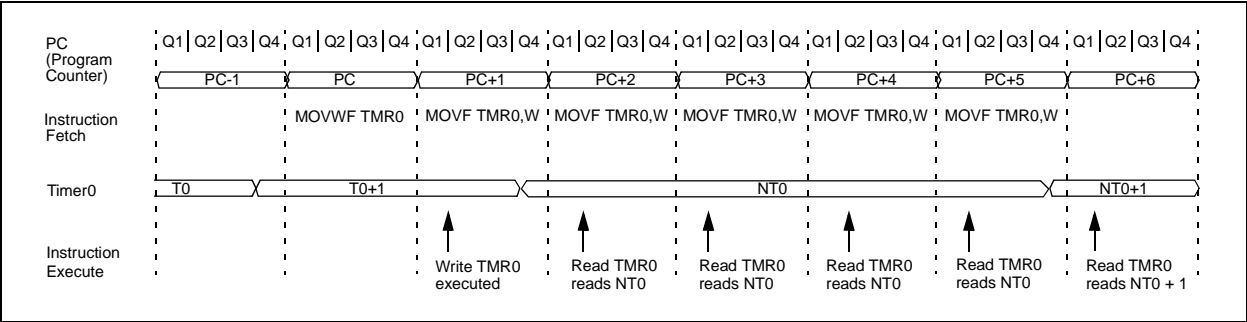


TABLE 8-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on MCLR and WDT Reset
01h	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells not used by Timer0.

8.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 9.2.1). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1,x, etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

8.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 8-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 8-1: CHANGING PRESCALER (TIMER0→WDT)

```
CLRWDT          ;Clear WDT
CLRF    TMR0     ;Clear TMR0 & Prescaler
MOVLW  B'00xx1111' ;Last 3 instructions in
                    this example
OPTION          ;are required only if
                ;desired
CLRWDT          ;PS<2:0> are 000 or
                ;001
MOVLW  B'00xx1xxx' ;Set Prescaler to
OPTION          ;desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 8-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

EXAMPLE 8-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT          ;Clear WDT and
                ;prescaler
MOVLW  B'xxxx0xxx' ;Select TMR0, new
                ;prescale value and
                ;clock source
OPTION
```

PIC16C5X

9.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a `SLEEP` instruction. During normal operation or `SLEEP`, a WDT Reset or Wake-up Reset generates a device RESET.

The \overline{TO} bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset (Section 6.3).

The WDT can be permanently disabled by programming the configuration bit `WDTE` as a '0' (Section 9.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

9.2.1 WDT PERIOD

An 8-bit counter is available as a prescaler for the Timer0 module (Section 8.2), or as a postscaler for the Watchdog Timer (WDT), respectively. For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not

both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The `PSA` and `PS<2:0>` bits (OPTION<3:0>) determine prescaler assignment and prescale ratio (Section 6.4).

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the `OPTION` register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, `VDD` and part-to-part process variations (see Device Characterization).

Under worst case conditions (`VDD` = Min., Temperature = Max., WDT prescaler = 1:128), it may take several seconds before a WDT time-out occurs.

9.2.2 WDT PROGRAMMING CONSIDERATIONS

The `CLRWDT` instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The `SLEEP` instruction RESETS the WDT and the prescaler, if assigned to the WDT. This gives the maximum `SLEEP` time before a WDT Wake-up Reset.

FIGURE 9-1: WATCHDOG TIMER BLOCK DIAGRAM

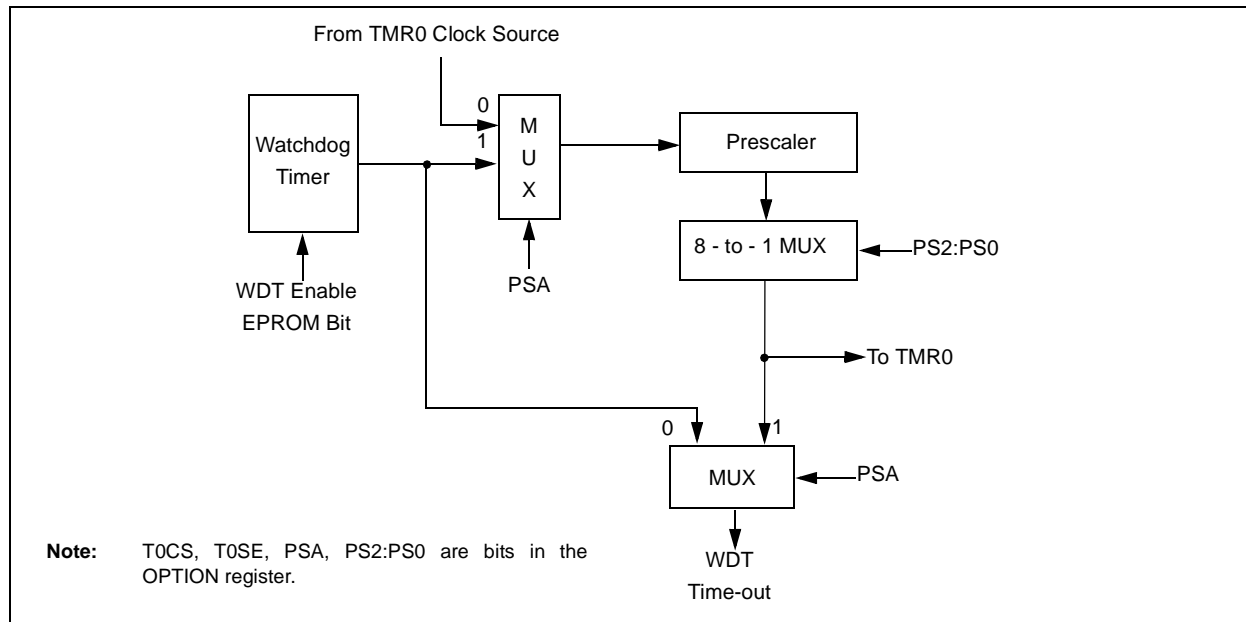


TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	OPTION	—	—	Tosc	Tose	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: u = unchanged, - = unimplemented, read as '0'. Shaded cells not used by Watchdog Timer.

CALL		Subroutine Call				
Syntax:	[<i>label</i>] CALL k					
Operands:	0 ≤ k ≤ 255					
Operation:	(PC) + 1 → TOS; k → PC<7:0>; (STATUS<6:5>) → PC<10:9>; 0 → PC<8>					
Status Affected:	None					
Encoding:	<table border="1"><tr><td>1001</td><td>kkkk</td><td>kkkk</td></tr></table>			1001	kkkk	kkkk
1001	kkkk	kkkk				
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two-cycle instruction.					
Words:	1					
Cycles:	2					
Example:	HERE CALL THERE					
Before Instruction						
PC = address (HERE)						
After Instruction						
PC = address (THERE)						
TOS = address (HERE + 1)						

CLRF	Clear f			
Syntax:	[<i>label</i>] CLRF f			
Operands:	$0 \leq f \leq 31$			
Operation:	00h \rightarrow (f); 1 \rightarrow Z			
Status Affected:	Z			
Encoding:	<table border="1"><tr><td>0000</td><td>011f</td><td>ffff</td></tr></table>	0000	011f	ffff
0000	011f	ffff		
Description:	The contents of register 'f' are cleared and the Z bit is set.			
Words:	1			
Cycles:	1			
Example:	CLRF FLAG_REG			
Before Instruction				
FLAG_REG	= 0x5A			
After Instruction				
FLAG_REG	= 0x00			
Z	= 1			

CLR W				
Syntax:	[<i>label</i>] CLRW			
Operands:	None			
Operation:	00h → (W); 1 → Z			
Status Affected:	Z			
Encoding:	<table border="1"><tr><td>0000</td><td>0100</td><td>0000</td></tr></table>	0000	0100	0000
0000	0100	0000		
Description:	The W register is cleared. Zero bit (Z) is set.			
Words:	1			
Cycles:	1			
Example:	CLR W			
Before Instruction				
W	= 0x5A			
After Instruction				
W	= 0x00			
Z	= 1			

CLRWD		Clear Watchdog Timer				
Syntax:	[<i>label</i>] CLRWD					
Operands:	None					
Operation:	00h → WDT; 0 → WDT prescaler (if assigned); 1 → \overline{TO} ; 1 → \overline{PD}					
Status Affected:	\overline{TO} , \overline{PD}					
Encoding:	<table border="1"><tr><td>0000</td><td>0000</td><td>0100</td></tr></table>			0000	0000	0100
0000	0000	0100				
Description:	The CLRWD instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits \overline{TO} and \overline{PD} are set.					
Words:	1					
Cycles:	1					
Example:	CLRWD					
Before Instruction						
WDT counter		=	?			
After Instruction						
WDT counter		=	0x00			
WDT prescaler		=	0			
\overline{TO}		=	1			
\overline{PD}		=	1			

11.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PIC MCUs and can be used to develop for this and other PIC microcontrollers. The MPLAB ICD utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

11.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in Stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable VDD and VPP supplies, which allow it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In Stand-alone mode, the PRO MATE II device programmer can read, verify, or program PIC devices. It can also set code protection in this mode.

11.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PIC devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

11.11 PICDEM 1 Low Cost PIC MCU Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE in-circuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

11.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I²C™ bus and separate headers for connection to an LCD module and a keypad.

PIC16C5X

NOTES:

12.6 Timing Parameter Symbolology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T		T
F	Frequency	Time

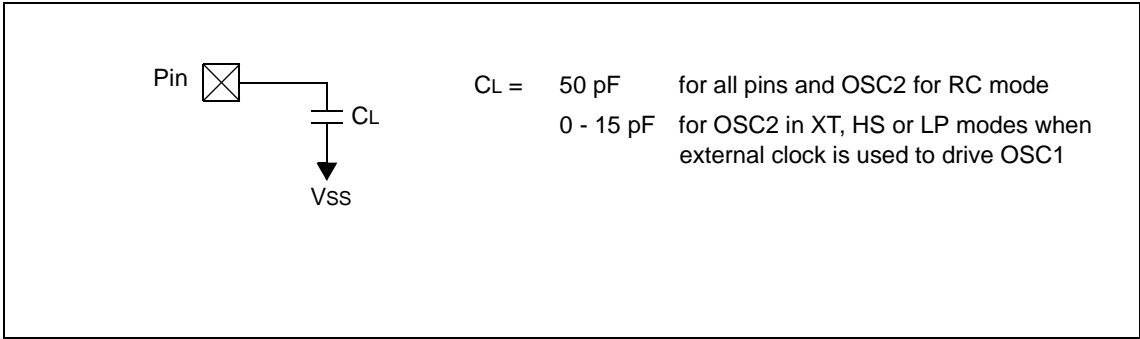
Lowercase letters (pp) and their meanings:

pp		
2	to	mc $\overline{\text{MCLR}}$
ck	CLKOUT	osc oscillator
cy	cycle time	os OSC1
drt	device reset timer	t0 T0CKI
io	I/O port	wdt watchdog timer

Uppercase letters and their meanings:

S		
F	Fall	P Period
H	High	R Rise
I	Invalid (Hi-impedance)	V Valid
L	Low	Z Hi-impedance

FIGURE 12-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54/55/56/57



PIC16C5X

FIGURE 12-5: TIMER0 CLOCK TIMINGS - PIC16C54/55/56/57

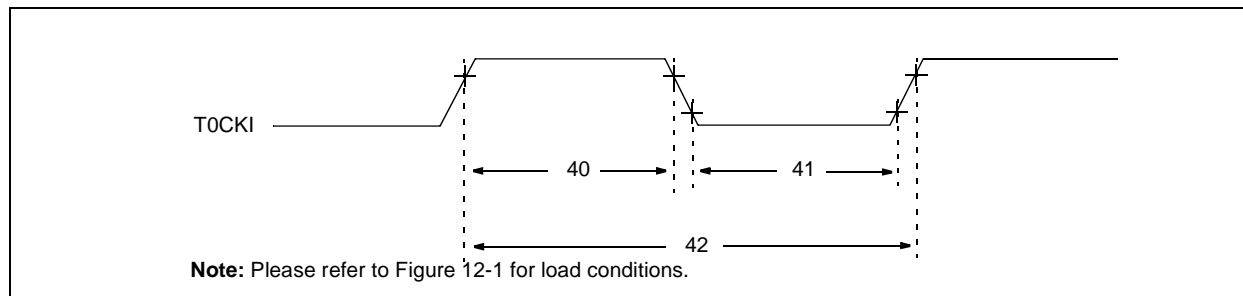


TABLE 12-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature 0°C ≤ TA ≤ +70°C for commercial −40°C ≤ TA ≤ +85°C for industrial −40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	0.5 TCY + 20*	—	—	ns	
		- No Prescaler					
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	0.5 TCY + 20*	—	—	ns	
		- No Prescaler					
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{TCY + 40^*}{N}$	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 14-2: TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 20 PF

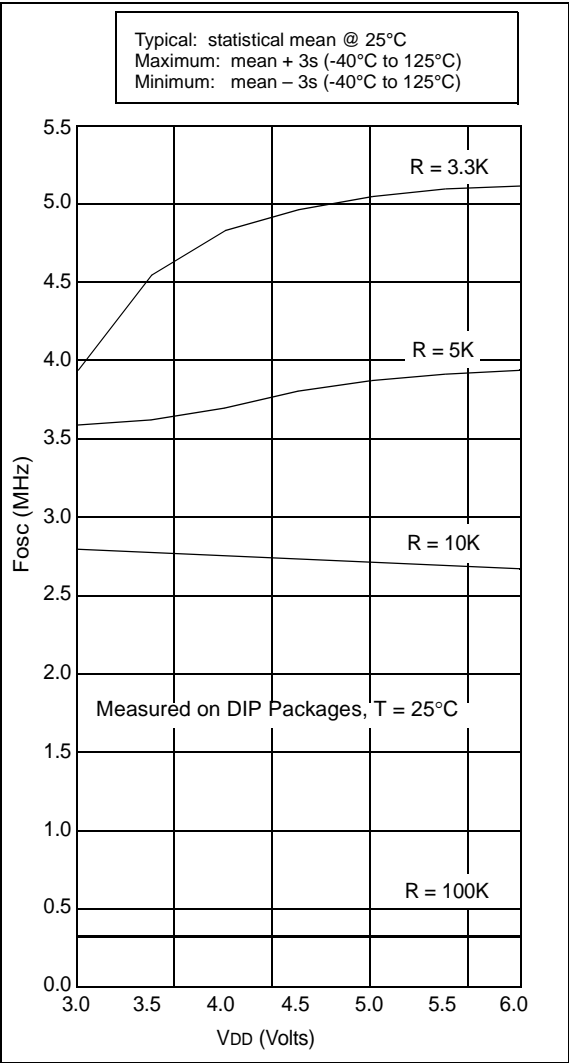


FIGURE 14-3: TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 100 PF

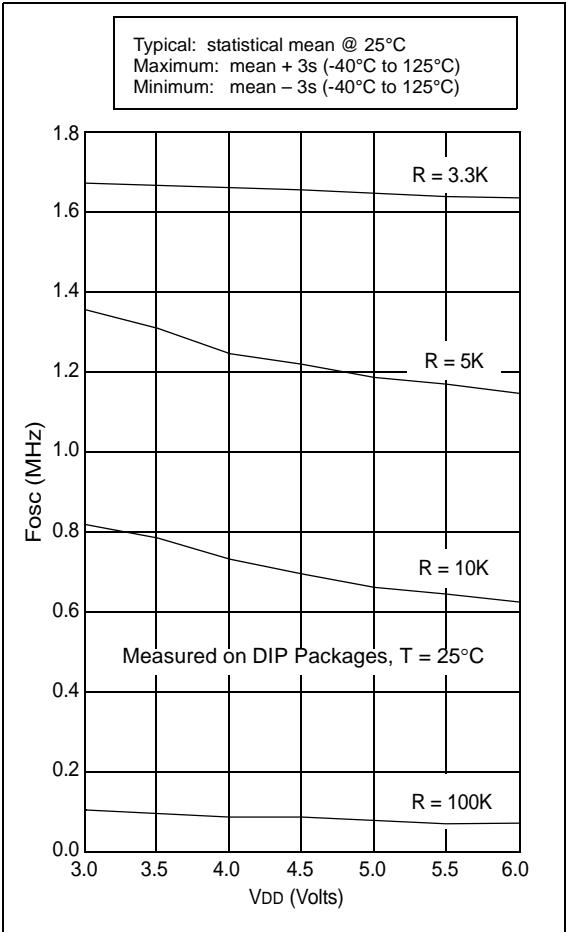


FIGURE 14-9: V_{TH} (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. V_{DD}

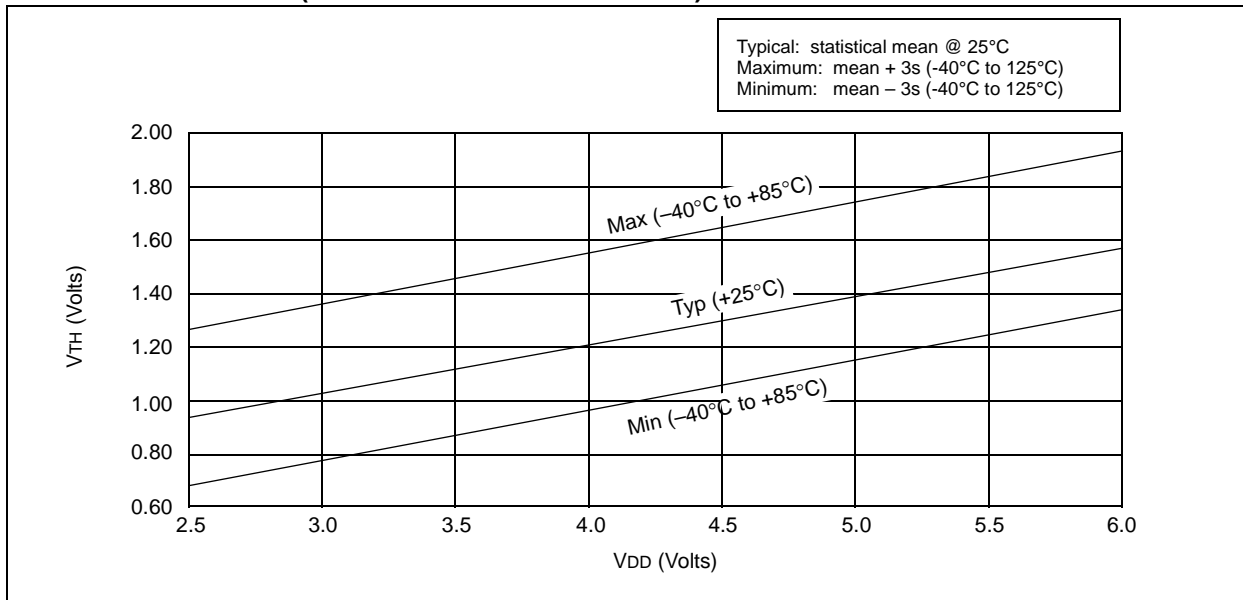
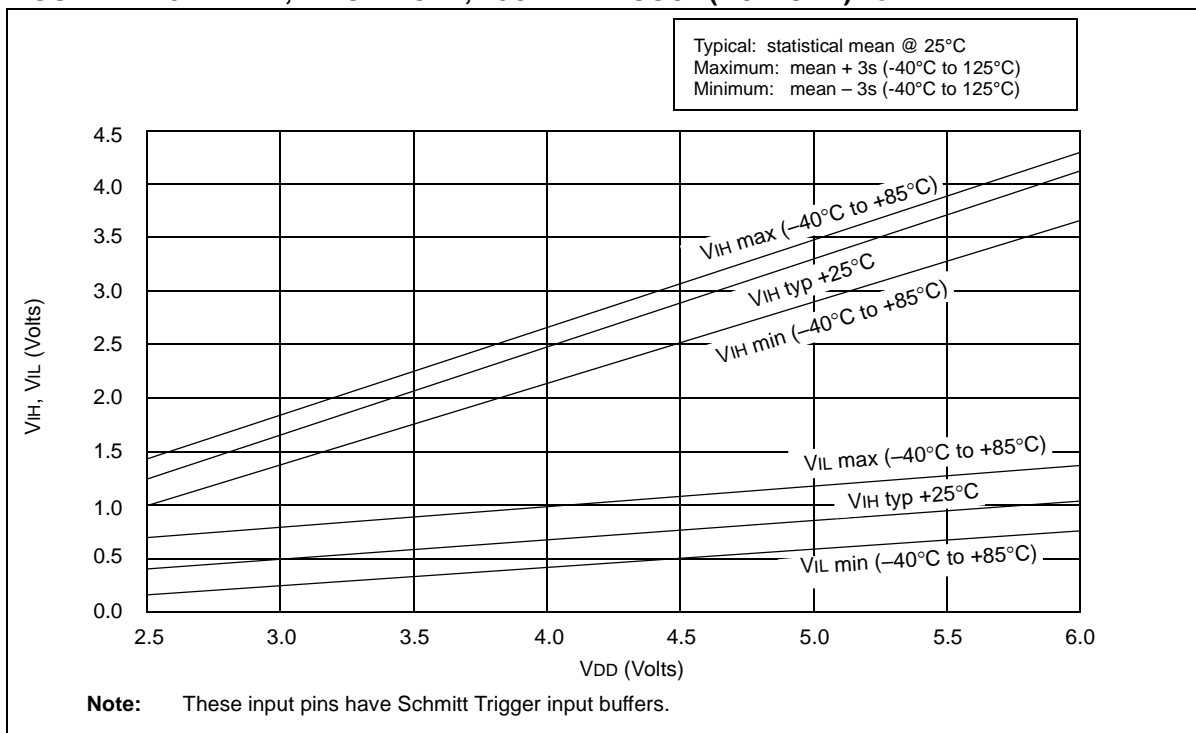


FIGURE 14-10: V_{IH} , V_{IL} OF MCLR, T0CKI AND OSC1 (RC MODE) vs. V_{DD}



PIC16C5X

15.3 DC Characteristics: PIC16LV54A-02 (Commercial) PIC16LV54A-02I (Industrial)

PIC16LV54A-02 PIC16LV54A-02I (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-20^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	V _{DD}	Supply Voltage RC and XT modes	2.0	—	3.8	V	
D002	V _{DR}	RAM Data Retention Voltage⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	V _{POR}	V_{DD} Start Voltage to ensure Power-on Reset	—	V _{SS}	—	V	See Section 5.1 for details on Power-on Reset
D004	S _{VDD}	V_{DD} Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	I _{DD}	Supply Current⁽²⁾ RC ⁽³⁾ and XT modes LP mode, Commercial LP mode, Industrial	— — —	0.5 11 14	— 27 35	mA μA μA	FOSC = 2.0 MHz, V _{DD} = 3.0V FOSC = 32 kHz, V _{DD} = 2.5V WDT disabled FOSC = 32 kHz, V _{DD} = 2.5V WDT disabled
D020	I _{PD}	Power-down Current^(2,4) Commercial Commercial Industrial Industrial	— — — —	2.5 0.25 3.5 0.3	12 4.0 14 5.0	μA μA μA μA	V _{DD} = 2.5V, WDT enabled V _{DD} = 2.5V, WDT disabled V _{DD} = 2.5V, WDT enabled V _{DD} = 2.5V, WDT disabled

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- Note 1:** This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.
- 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
- a) The test conditions for all I_{DD} measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS}, T_{0CKI} = V_{DD}, MCLR = V_{DD}; WDT enabled/disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3:** Does not include current through R_{EXT}. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ.
- 4:** The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection on wake-up from SLEEP mode or during initial power-up.

FIGURE 18-6: TYPICAL I_{PD} vs. V_{DD} , WATCHDOG ENABLED (25°C)

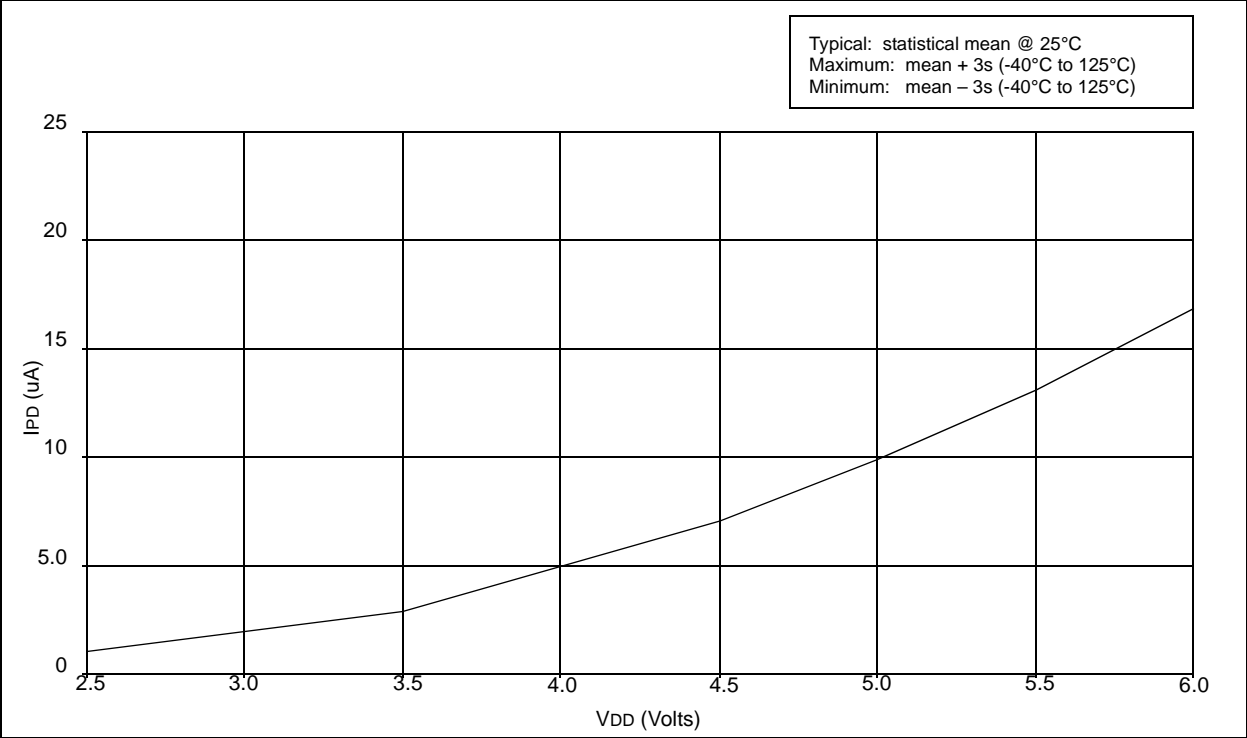


FIGURE 18-7: TYPICAL I_{PD} vs. V_{DD} , WATCHDOG ENABLED (-40°C, 85°C)

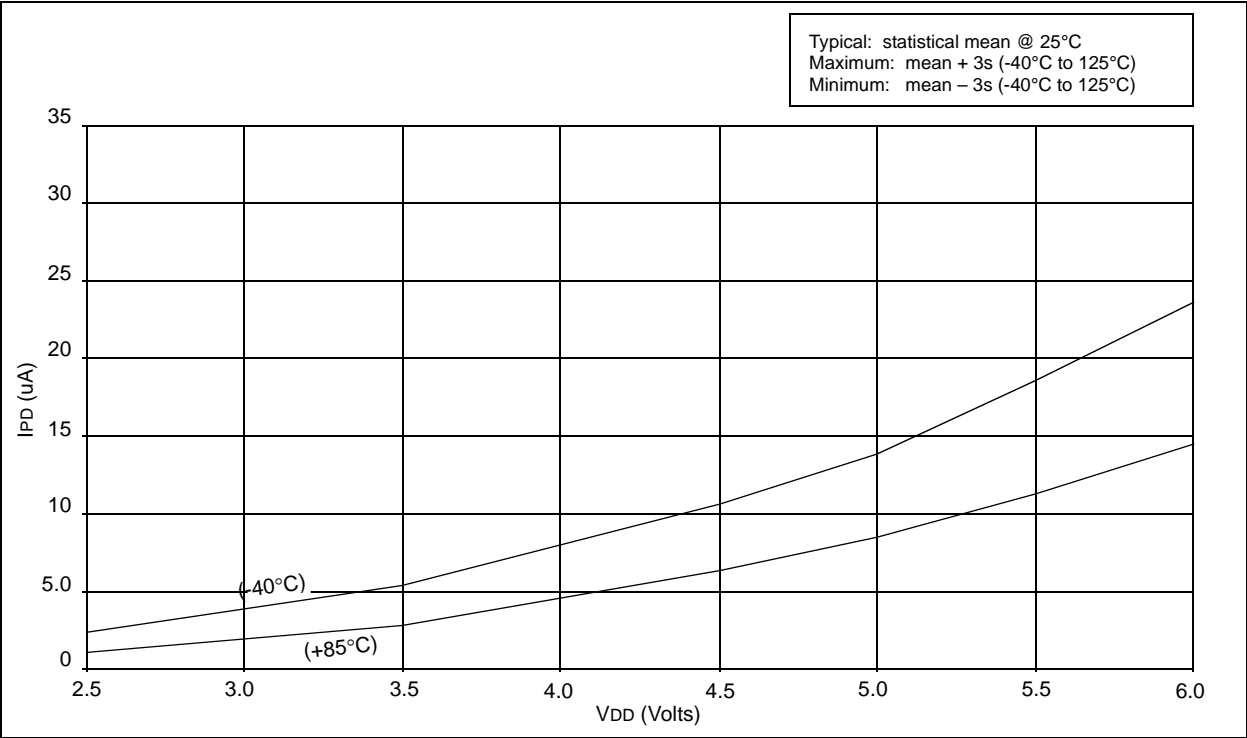


FIGURE 18-12: TYPICAL I_{DD} vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, 25°C)

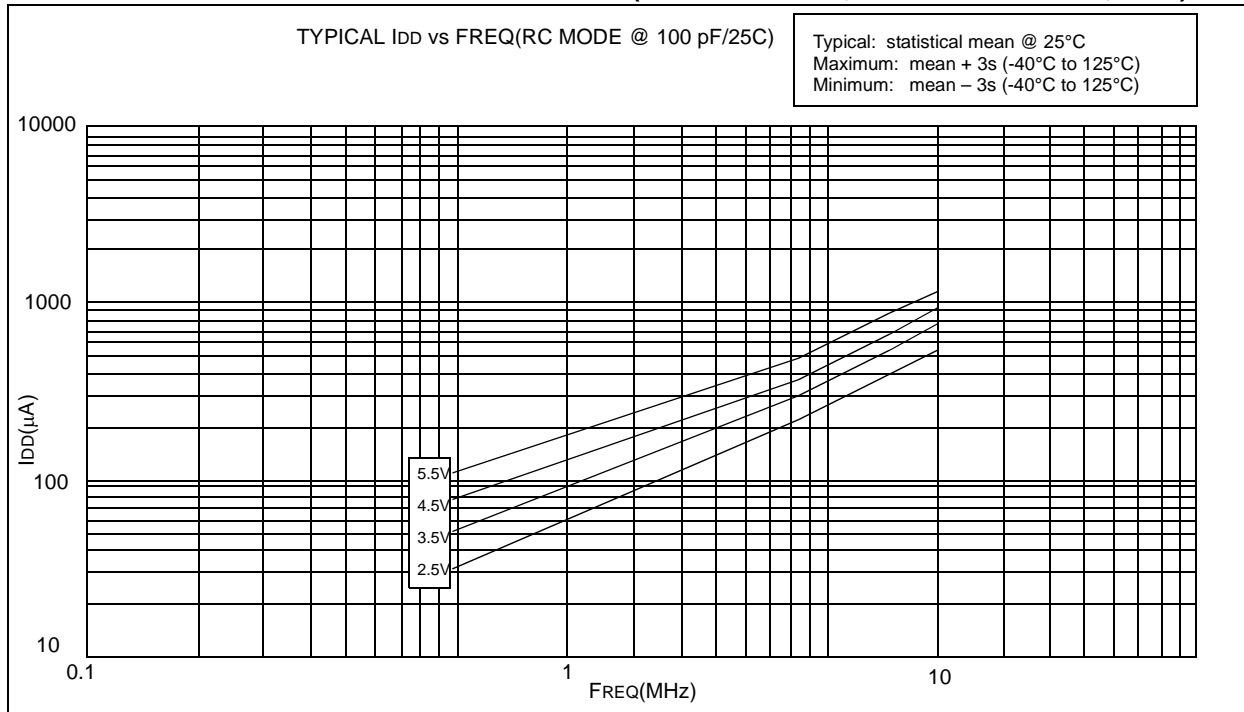


FIGURE 18-13: TYPICAL I_{DD} vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, 25°C)

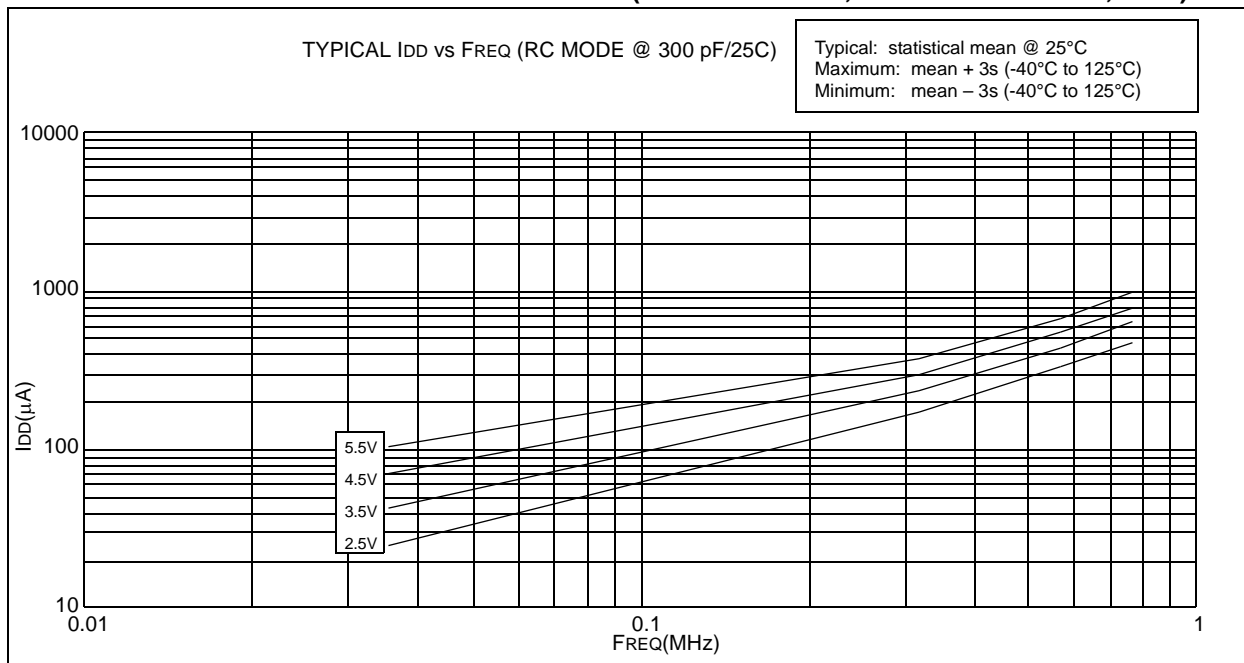


FIGURE 18-16: PORTA, B AND C I_{OH} vs. V_{OH} , $V_{DD} = 5\text{ V}$

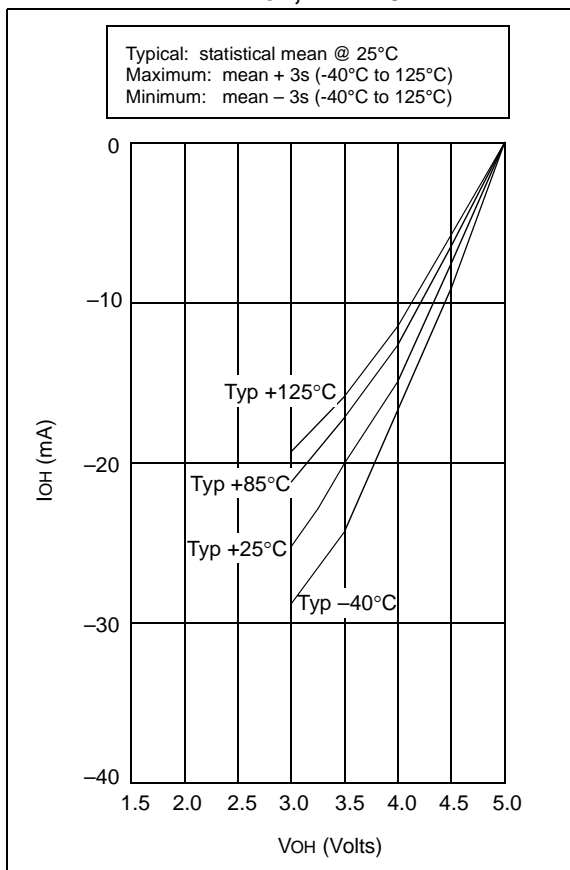
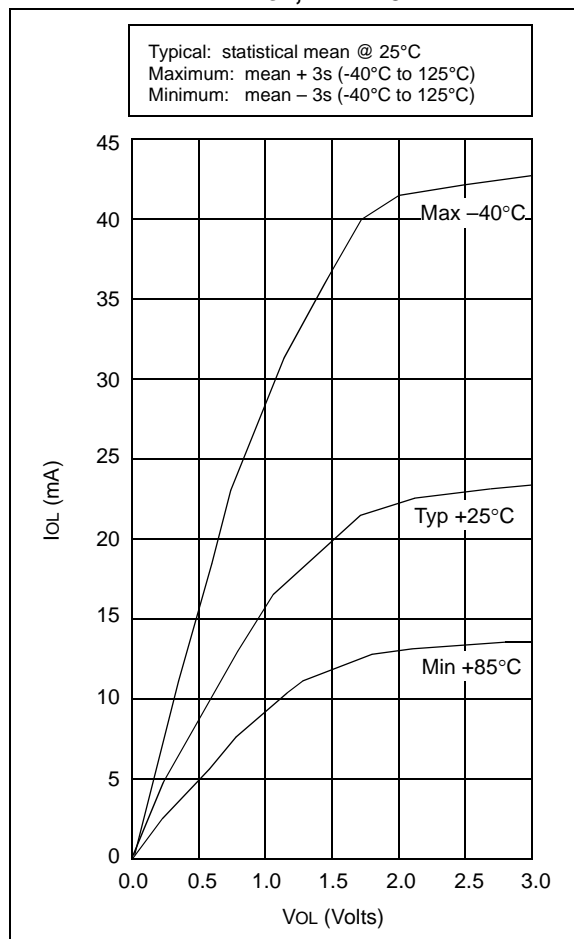


FIGURE 18-17: PORTA, B AND C I_{OL} vs. V_{OL} , $V_{DD} = 3\text{ V}$



19.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)⁽¹⁾

PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature 0°C ≤ TA ≤ +70°C for commercial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	4.5	—	5.5	V	HS mode from 20 - 40 MHz
D002	VDR	RAM Data Retention Voltage ⁽²⁾	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current ⁽³⁾	—	5.2 6.8	12.3 16	mA mA	FOSC = 40 MHz, VDD = 4.5V, HS mode FOSC = 40 MHz, VDD = 5.5V, HS mode
D020	IPD	Power-down Current ⁽³⁾	—	1.8 9.8	7.0 27*	μA μA	VDD = 5.5V, WDT disabled, Commercial VDD = 5.5V, WDT enabled, Commercial

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- Note 1:** Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected, HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 19.1.
- 2:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
- 3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

PIC16C5X

FIGURE 19-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X-40

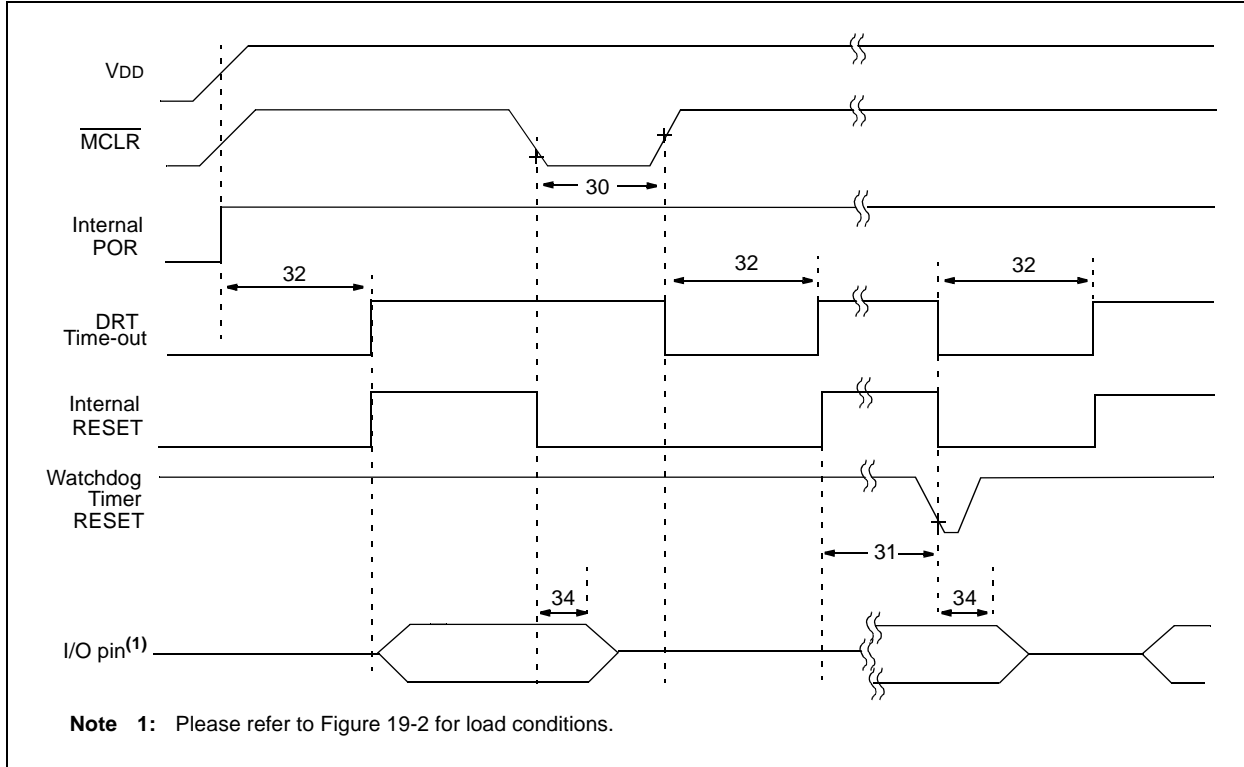


TABLE 19-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X-40

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics							
Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial)							
Operating Voltage VDD range is described in Section 19.1.							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	1000*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns	

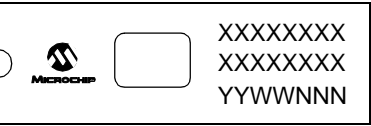
* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

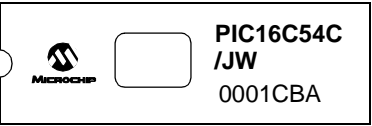
PIC16C5X

Package Marking Information (Cont'd)

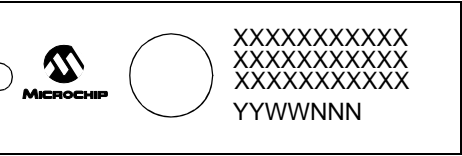
18-Lead Cerdip Windowed



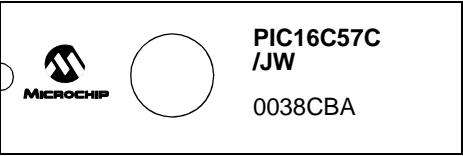
Example



28-Lead Cerdip Windowed



Example



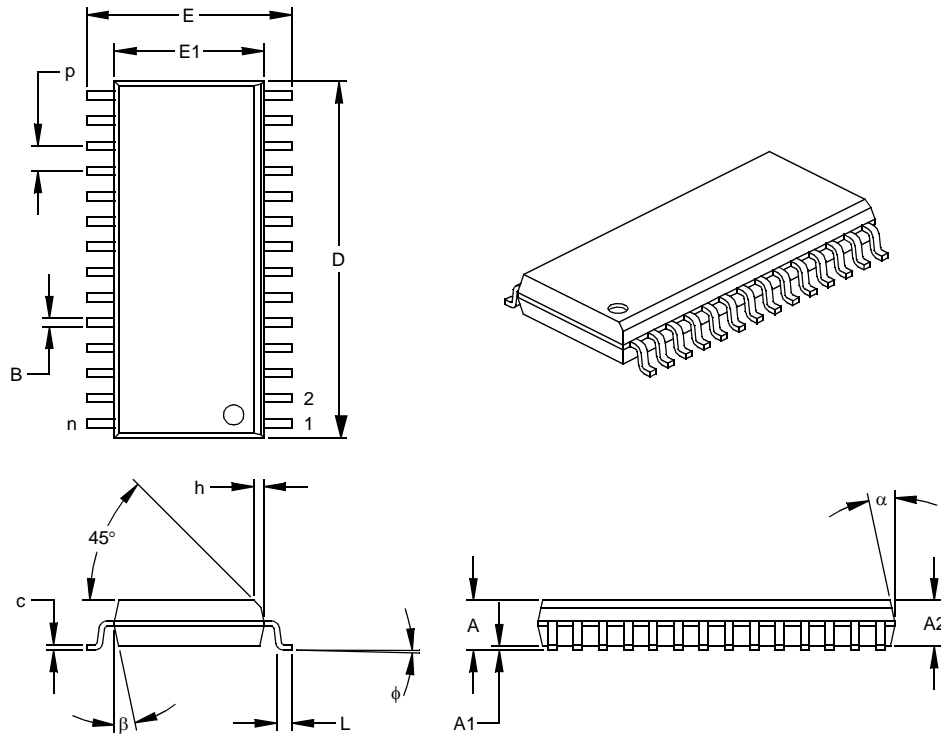
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

28-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59
Overall Length	D	.695	.704	.712	17.65	17.87	18.08
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle Top	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-013

Drawing No. C04-052