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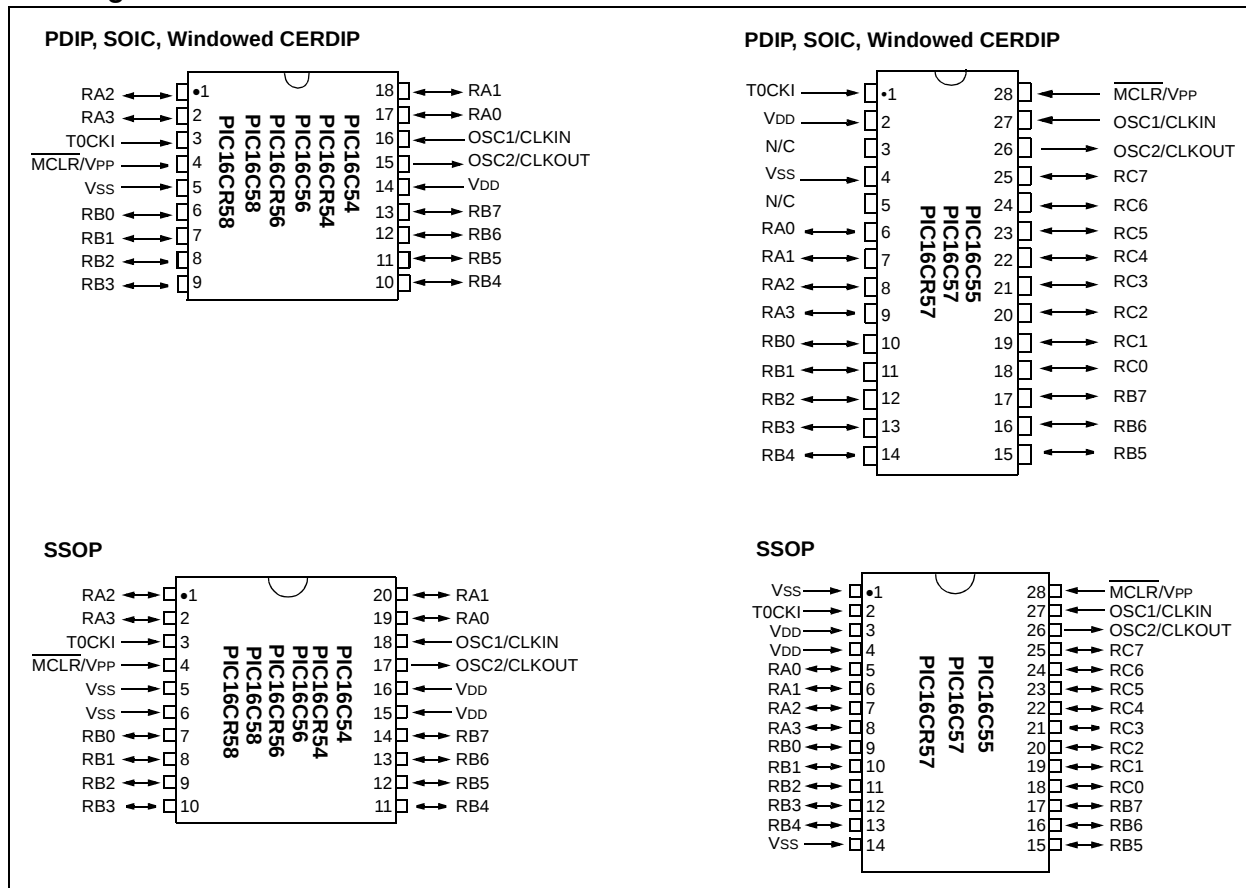
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	24 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c55-hsi-so

PIC16C5X

Pin Diagrams



Device Differences

Device	Voltage Range	Oscillator Selection (Program)	Oscillator	Process Technology (Microns)	ROM Equivalent	MCLR Filter
PIC16C54	2.5-6.25	Factory	See Note 1	1.2	PIC16CR54A	No
PIC16C54A	2.0-6.25	User	See Note 1	0.9	—	No
PIC16C54C	2.5-5.5	User	See Note 1	0.7	PIC16CR54C	Yes
PIC16C55	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C55A	2.5-5.5	User	See Note 1	0.7	—	Yes
PIC16C56	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C56A	2.5-5.5	User	See Note 1	0.7	PIC16CR56A	Yes
PIC16C57	2.5-6.25	Factory	See Note 1	1.2	—	No
PIC16C57C	2.5-5.5	User	See Note 1	0.7	PIC16CR57C	Yes
PIC16C58B	2.5-5.5	User	See Note 1	0.7	PIC16CR58B	Yes
PIC16CR54A	2.5-6.25	Factory	See Note 1	1.2	N/A	Yes
PIC16CR54C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR56A	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR57C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR58B	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

Note: The table shown above shows the generic names of the PIC16C5X devices. For device varieties, please refer to Section 2.0.

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4.3 External Crystal Oscillator Circuit

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 4-3 shows an implementation example of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 k Ω resistor provides the negative feedback for stability. The 10 k Ω potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 4-3: EXAMPLE OF EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)

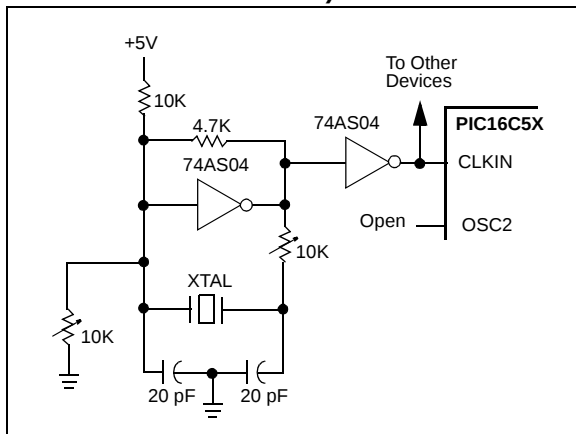
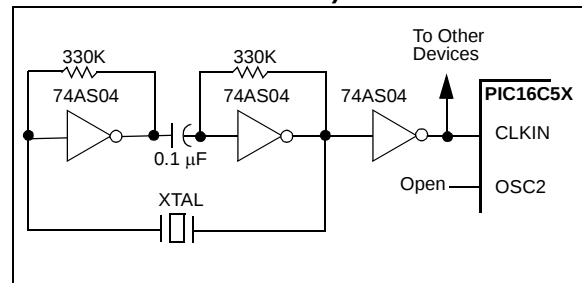


Figure 4-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 k Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 4-4: EXAMPLE OF EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)



PIC16C5X

6.5.1 PAGING CONSIDERATIONS – PIC16C56/CR56, PIC16C57/CR57 AND PIC16C58/CR58

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS Register will not be updated. Therefore, the next `GOTO`, `CALL` or modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA<1:0>).

For example, a `NOP` at location 1FFh (page 0) increments the PC to 200h (page 1). A `GOTO xxx` at 200h will return the program to address xxh on page 0 (assuming that PA<1:0> are clear).

To prevent this, the page preselect bits must be updated under program control.

6.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the RESET vector).

The STATUS Register page preselect bits are cleared upon a RESET, which means that page 0 is preselected.

Therefore, upon a RESET, a `GOTO` instruction at the RESET vector location will automatically cause the program to jump to page 0.

6.6 Stack

PIC16C5X devices have a 10-bit or 11-bit wide, two-level hardware push/pop stack.

A `CALL` instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential `CALL`'s are executed, only the most recent two return addresses are stored.

A `RETLW` instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential `RETLW`'s are executed, the stack will be filled with the address previously stored in level 2. Note that the W Register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the `RETLW` instruction, the PC is loaded with the Top of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC, therefore, paging is not an issue when returning from a subroutine.

7.6 I/O Programming Considerations

7.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 7-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

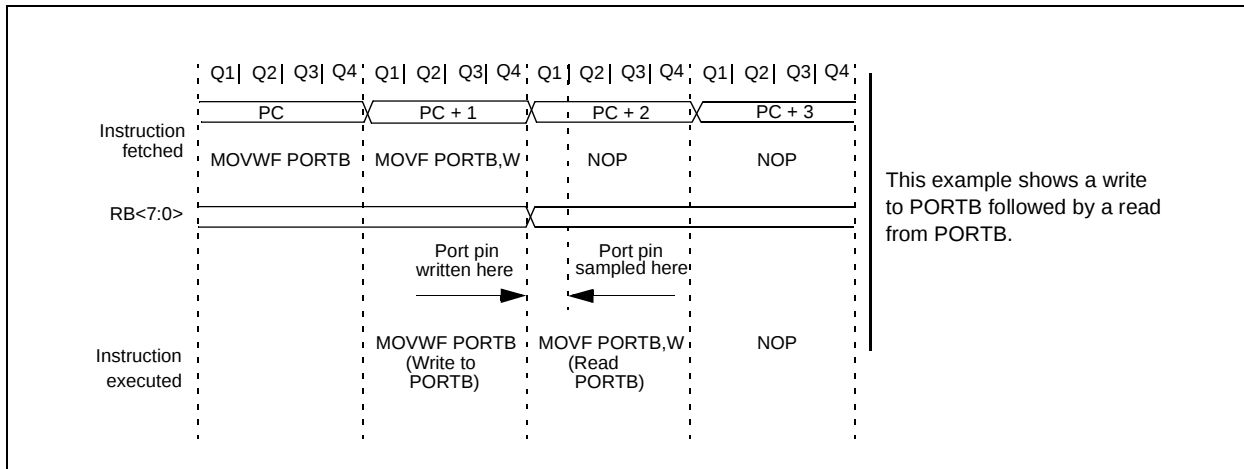
EXAMPLE 7-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                                PORT latch  PORT pins
;                                -----
BCF  PORTB, 7  ;01pp pppp  11pp pppp
BCF  PORTB, 6  ;10pp pppp  11pp pppp
MOVLW H'3F'    ;
TRIS  PORTB    ;10pp pppp  10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

7.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 7-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 7-2: SUCCESSIVE I/O OPERATION



PIC16C5X

COMF Complement f

Syntax: `[label] COMF f,d`

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

0010	01df	ffff
------	------	------

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: `COMF REG1, 0`

Before Instruction
 REG1 = 0x13
 After Instruction
 REG1 = 0x13
 W = 0xEC

DECF Decrement f

Syntax: `[label] DECF f,d`

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) - 1 \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

0000	11df	ffff
------	------	------

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: `DECF CNT, 1`

Before Instruction
 CNT = 0x01
 Z = 0
 After Instruction
 CNT = 0x00
 Z = 1

DECFSZ Decrement f, Skip if 0

Syntax: `[label] DECFSZ f,d`

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) - 1 \rightarrow d$; skip if result = 0

Status Affected: None

Encoding:

0010	11df	ffff
------	------	------

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example: `HERE DECFSZ CNT, 1
 GOTO LOOP
 CONTINUE`

Before Instruction
 PC = address (HERE)
 After Instruction
 CNT = CNT - 1;
 if CNT = 0,
 PC = address (CONTINUE);
 if CNT $\neq$ 0,
 PC = address (HERE+1)

PIC16C5X

12.5 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	V_{IL}	Input Low Voltage					
		I/O ports	V_{SS}	—	$0.15 V_{DD}$	V	Pin at hi-impedance
		MCLR (Schmitt Trigger)	V_{SS}	—	$0.15 V_{DD}$	V	
		T0CKI (Schmitt Trigger)	V_{SS}	—	$0.15 V_{DD}$	V	
		OSC1 (Schmitt Trigger)	V_{SS}	—	$0.15 V_{DD}$	V	PIC16C5X-RC only ⁽³⁾
		OSC1 (Schmitt Trigger)	V_{SS}	—	$0.3 V_{DD}$	V	PIC16C5X-XT, 10, HS, LP
D040	V_{IH}	Input High Voltage					
		I/O ports	$0.45 V_{DD}$	—	V_{DD}	V	For all V_{DD} ⁽⁴⁾
		I/O ports	2.0	—	V_{DD}	V	$4.0\text{V} < V_{DD} \leq 5.5\text{V}$ ⁽⁴⁾
		I/O ports	$0.36 V_{DD}$	—	V_{DD}	V	$V_{DD} > 5.5\text{V}$
		MCLR (Schmitt Trigger)	$0.85 V_{DD}$	—	V_{DD}	V	
		T0CKI (Schmitt Trigger)	$0.85 V_{DD}$	—	V_{DD}	V	
		OSC1 (Schmitt Trigger)	$0.85 V_{DD}$	—	V_{DD}	V	PIC16C5X-RC only ⁽³⁾
		OSC1 (Schmitt Trigger)	$0.7 V_{DD}$	—	V_{DD}	V	PIC16C5X-XT, 10, HS, LP
D050	V_{HYS}	Hysteresis of Schmitt Trigger inputs	$0.15 V_{DD}^*$	—	—	V	
D060	I_{IL}	Input Leakage Current ^(1,2)					
		I/O ports	–1	0.5	+1	μA	For $V_{DD} \leq 5.5\text{V}$: $V_{SS} \leq V_{PIN} \leq V_{DD}$, pin at hi-impedance
		MCLR	–5	—	—	μA	$V_{PIN} = V_{SS} + 0.25\text{V}$
		MCLR	—	0.5	+5	μA	$V_{PIN} = V_{DD}$
		T0CKI	–3	0.5	+3	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$
		OSC1	–3	0.5	+3	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, PIC16C5X-XT, 10, HS, LP
D080	V_{OL}	Output Low Voltage					
		I/O ports	—	—	0.6	V	$I_{OL} = 8.7\text{ mA}$, $V_{DD} = 4.5\text{V}$
		OSC2/CLKOUT	—	—	0.6	V	$I_{OL} = 1.6\text{ mA}$, $V_{DD} = 4.5\text{V}$, PIC16C5X-RC
D090	V_{OH}	Output High Voltage ⁽²⁾					
		I/O ports	$V_{DD} - 0.7$	—	—	V	$I_{OH} = -5.4\text{ mA}$, $V_{DD} = 4.5\text{V}$
		OSC2/CLKOUT	$V_{DD} - 0.7$	—	—	V	$I_{OH} = -1.0\text{ mA}$, $V_{DD} = 4.5\text{V}$, PIC16C5X-RC

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C . This data is for design guidance only and is not tested.

Note 1: The leakage current on the $\overline{\text{MCLR}}/\text{VPP}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

13.0 ELECTRICAL CHARACTERISTICS - PIC16CR54A

Absolute Maximum Ratings^(†)

Ambient Temperature under bias	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on V _{DD} with respect to V _{SS}	0 to +7.5V
Voltage on MCLR with respect to V _{SS} ⁽¹⁾	0 to +14V
Voltage on all other pins with respect to V _{SS}	–0.6V to (V _{DD} + 0.6V)
Total power dissipation ⁽²⁾	800 mW
Max. current out of V _{SS} pin	150 mA
Max. current into V _{DD} pin	50 mA
Max. current into an input pin (TOCKI only)	±500 µA
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD})	±20 mA
Max. output current sunk by any I/O pin	25 mA
Max. output current sourced by any I/O pin	20 mA
Max. output current sourced by a single I/O port (PORTA or B)	40 mA
Max. output current sunk by a single I/O port (PORTA or B)	50 mA

Note 1: Voltage spikes below V_{SS} at the MCLR pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a low level to the MCLR pin rather than pulling this pin directly to V_{SS}.

2: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIC16C5X

13.4 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	V _{IL}	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	V _{SS} V _{SS} V _{SS} V _{SS} V _{SS}	— — — — —	0.15 V _{DD} 0.15 V _{DD} 0.15 V _{DD} 0.15 V _{DD} 0.3 V _{DD}	V V V V V	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes
D040	V _{IH}	Input High Voltage I/O ports I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	0.45 V _{DD} 2.0 0.36 V _{DD} 0.85 V _{DD} 0.85 V _{DD} 0.85 V _{DD} 0.7 V _{DD}	— — — — — — —	V _{DD} V _{DD} V _{DD} V _{DD} V _{DD} V _{DD} V _{DD}	V V V V V V V	For all V _{DD} ⁽⁴⁾ 4.0V < V _{DD} ≤ 5.5V ⁽⁴⁾ V _{DD} > 5.5V RC mode only ⁽³⁾ XT, HS and LP modes
D050	V _{HYS}	Hysteresis of Schmitt Trigger inputs	0.15 V _{DD} *	—	—	V	
D060	I _{IL}	Input Leakage Current^(1,2) I/O ports MCLR MCLR T0CKI OSC1	−1.0 −5.0 — −3.0 −3.0	0.5 — 0.5 0.5 0.5	+1.0 — +5.0 +3.0 +3.0	μA μA μA μA μA	For V_{DD} ≤ 5.5V: V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance V _{PIN} = V _{SS} + 0.25V V _{PIN} = V _{DD} V _{SS} ≤ V _{PIN} ≤ V _{DD} V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT, HS and LP modes
D080	V _{OL}	Output Low Voltage I/O ports OSC2/CLKOUT	— —	— —	0.6 0.6	V V	I _{OL} = 8.7 mA, V _{DD} = 4.5V I _{OL} = 1.6 mA, V _{DD} = 4.5V, RC mode only
D090	V _{OH}	Output High Voltage⁽²⁾ I/O ports OSC2/CLKOUT	V _{DD} − 0.7 V _{DD} − 0.7	— —	— —	V V	I _{OH} = −5.4 mA, V _{DD} = 4.5V I _{OH} = −1.0 mA, V _{DD} = 4.5V, RC mode only

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/V_{PP} pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

FIGURE 14-6: MAXIMUM IPD vs. VDD,
WATCHDOG DISABLED

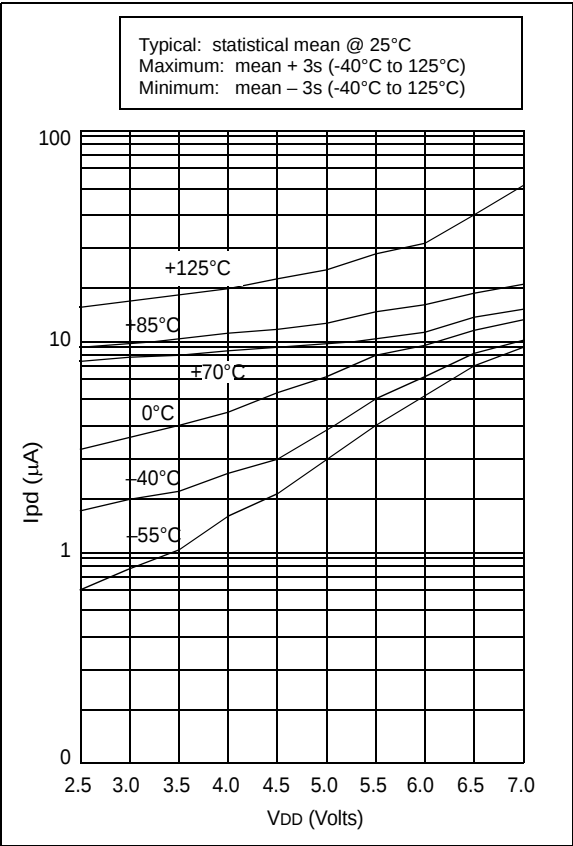


FIGURE 14-7: TYPICAL IPD vs. VDD,
WATCHDOG ENABLED

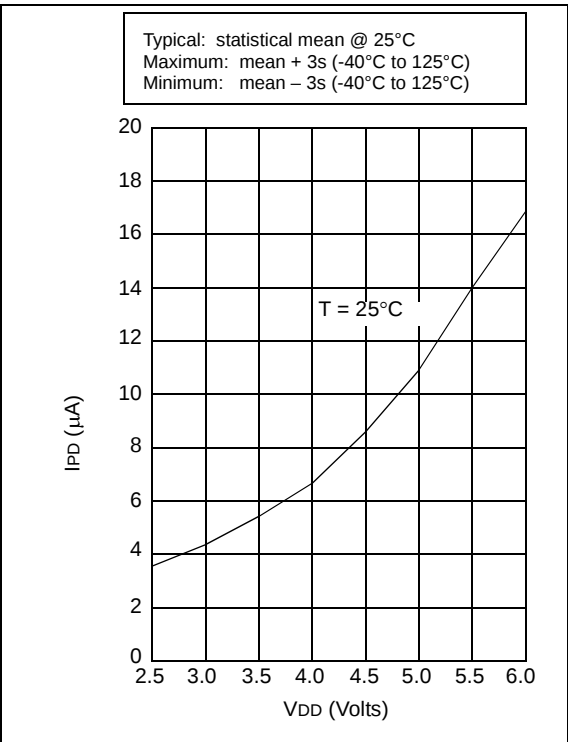
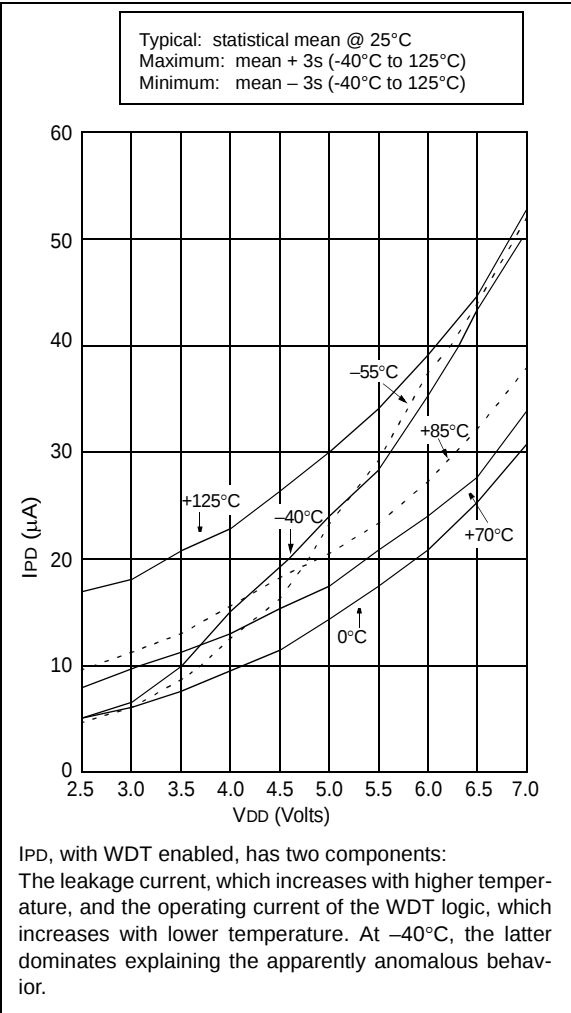


FIGURE 14-8: MAXIMUM IPD vs. VDD,
WATCHDOG ENABLED



15.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended) PIC16LC54A-04E (Extended)

PIC16LC54A-04E (Extended)		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
PIC16C54A-04E, 10E, 20E (Extended)		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D020	IPD	Power-down Current⁽²⁾					
		PIC16LC54A	—	2.5	15	μA	$V_{DD} = 2.5\text{V}$, WDT enabled, Extended
			—	0.25	7.0	μA	$V_{DD} = 2.5\text{V}$, WDT disabled, Extended
D020A		PIC16C54A	—	5.0	22	μA	$V_{DD} = 3.5\text{V}$, WDT enabled
			—	0.8	18*	μA	$V_{DD} = 3.5\text{V}$, WDT disabled

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C . This data is for design guidance only and is not tested.

Note 1: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all I_{DD} measurements in active Operation mode are: $OSC1$ = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS} , $T0CKI = V_{DD}$, $MCLR = V_{DD}$; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through R_{EXT} . The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in $k\Omega$.

FIGURE 16-14: TYPICAL I_{DD} vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, 25°C)

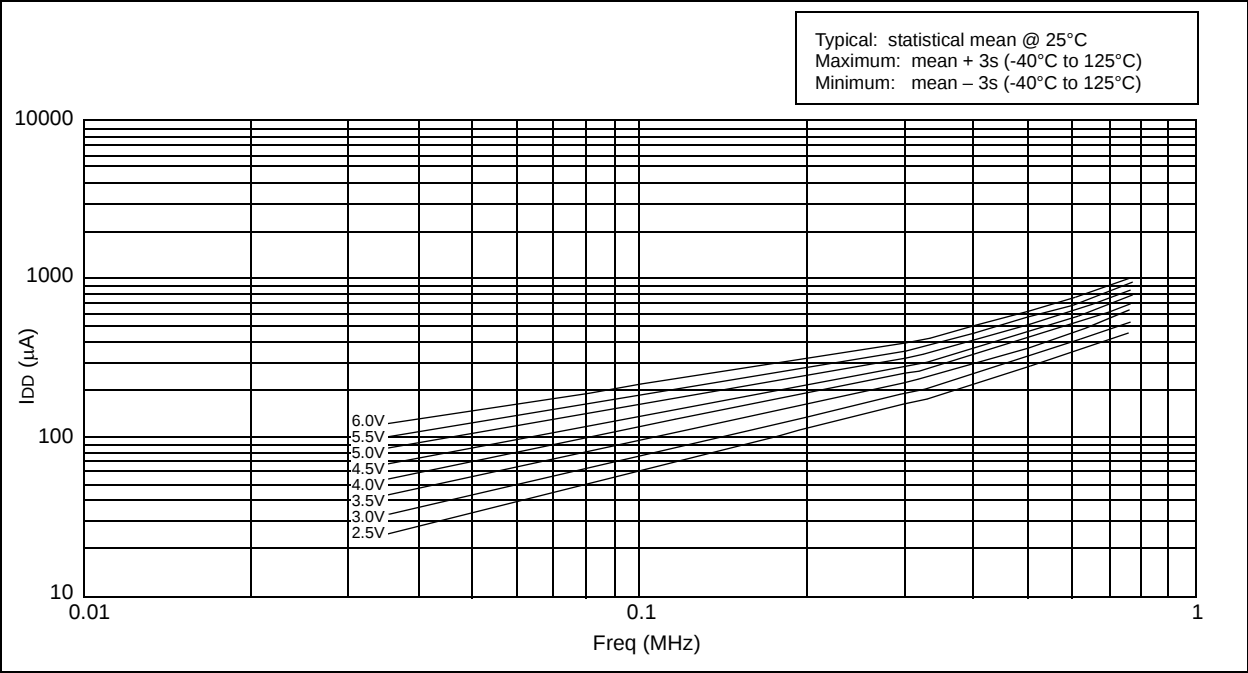


FIGURE 16-15: MAXIMUM I_{DD} vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, -40°C to +85°C)

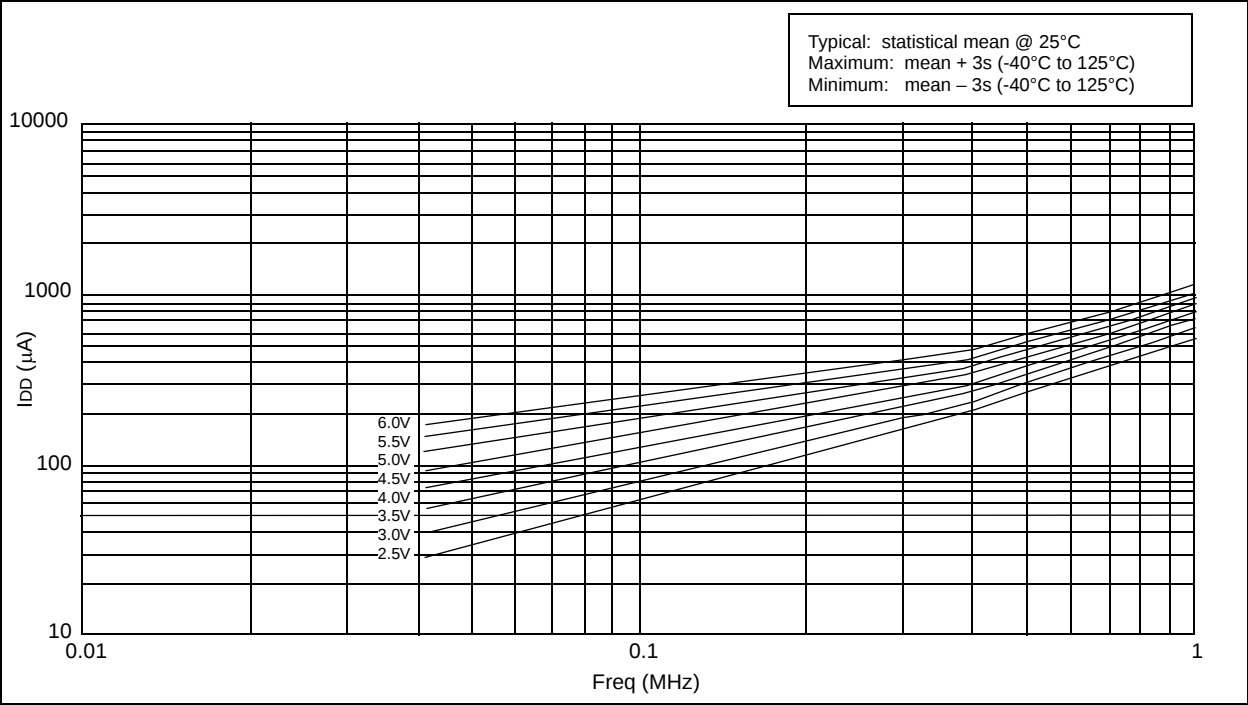


FIGURE 16-20: PORTA, B AND C I_{OH} vs. V_{OH} , $V_{DD} = 3V$

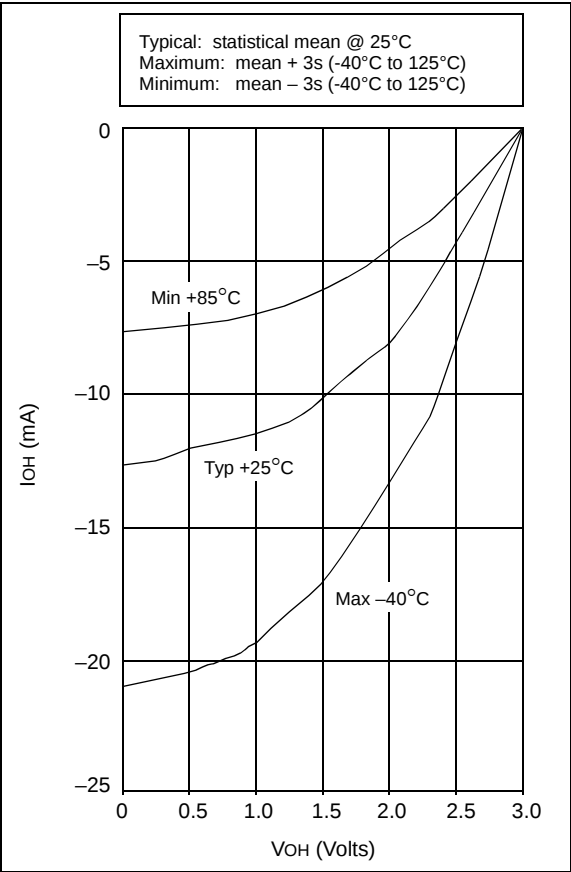


FIGURE 16-21: PORTA, B AND C I_{OH} vs. V_{OH} , $V_{DD} = 5V$

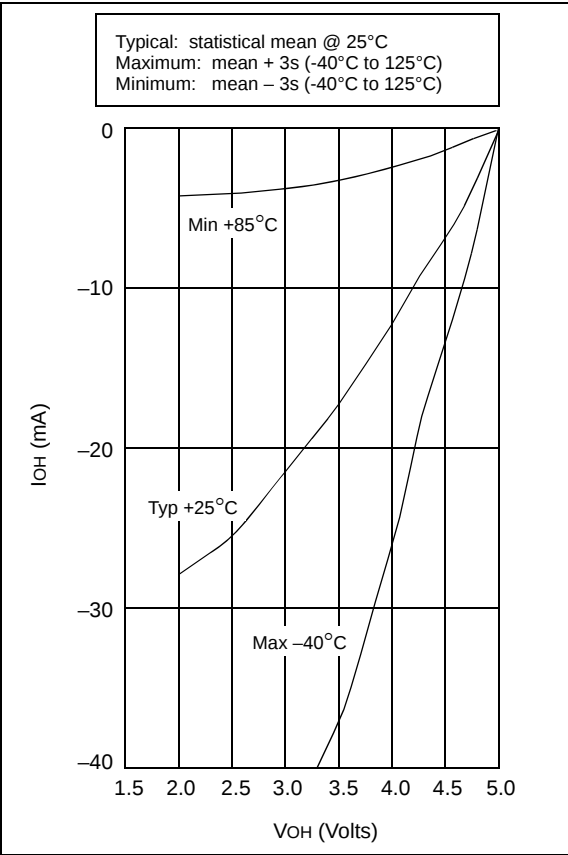


TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
2	Tcy	Instruction Cycle Time ⁽²⁾	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

FIGURE 17-8: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X, PIC16CR5X

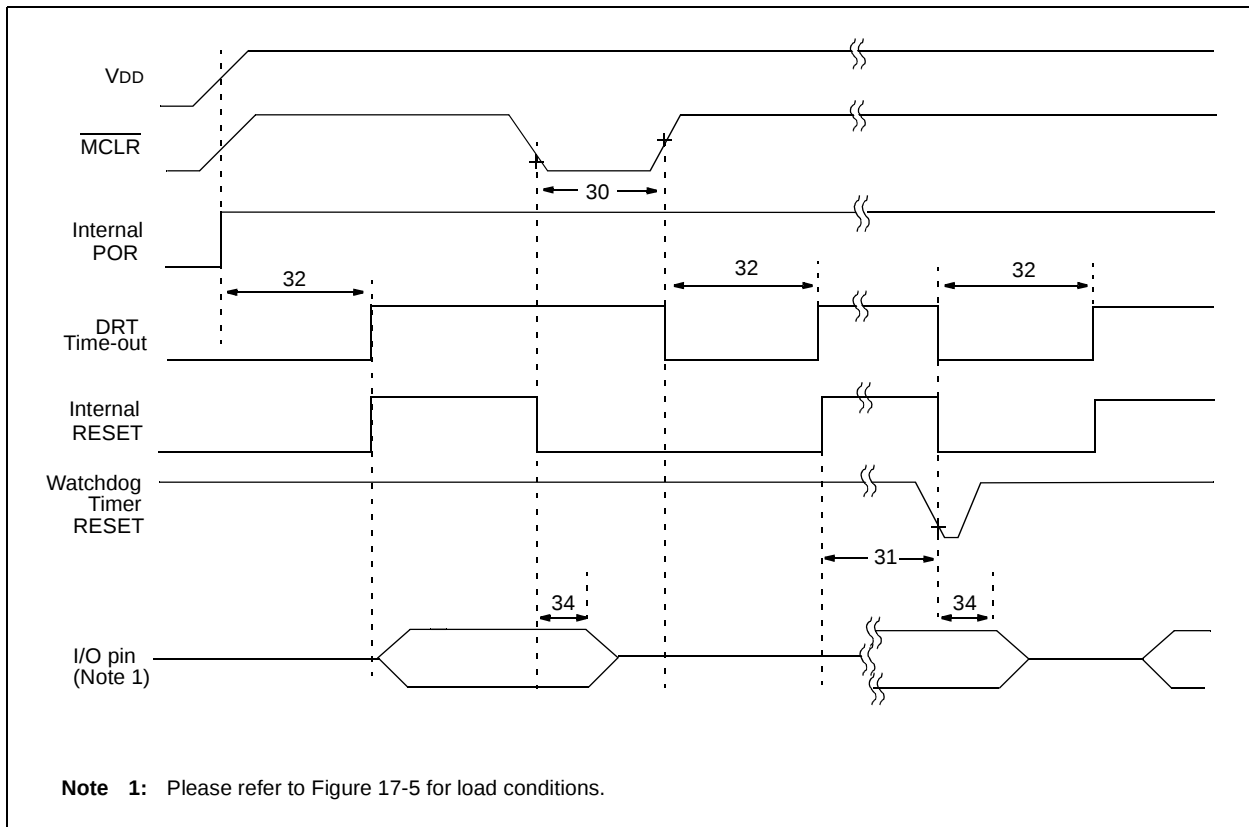


TABLE 17-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X, PIC16CR5X

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics		Operating Temperature					
		0°C ≤ TA ≤ +70°C for commercial					
		-40°C ≤ TA ≤ +85°C for industrial					
		-40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1000*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C5X

FIGURE 17-9: TIMER0 CLOCK TIMINGS - PIC16C5X, PIC16CR5X

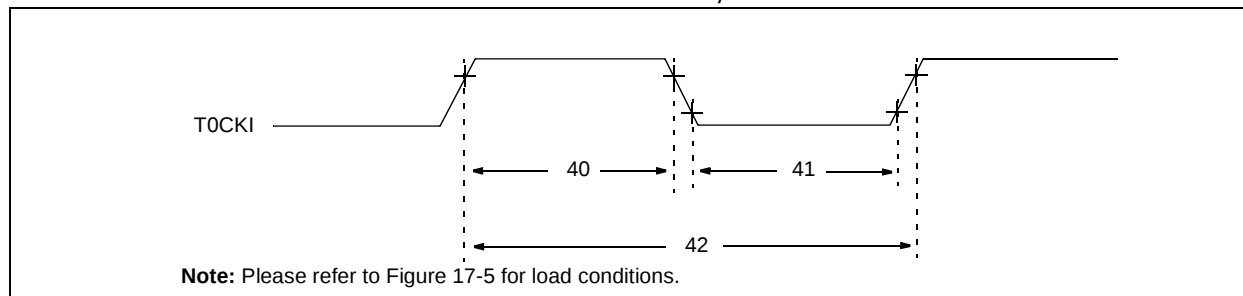


TABLE 17-4: TIMER0 CLOCK REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature					
		0°C ≤ TA ≤ +70°C for commercial					
		–40°C ≤ TA ≤ +85°C for industrial					
		–40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width					
		- No Prescaler	0.5 Tcy + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width					
		- No Prescaler	0.5 Tcy + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{Tcy + 40}{N}$ *	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 18-10: V_{TH} (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (IN XT, HS AND LP MODES) vs. V_{DD}

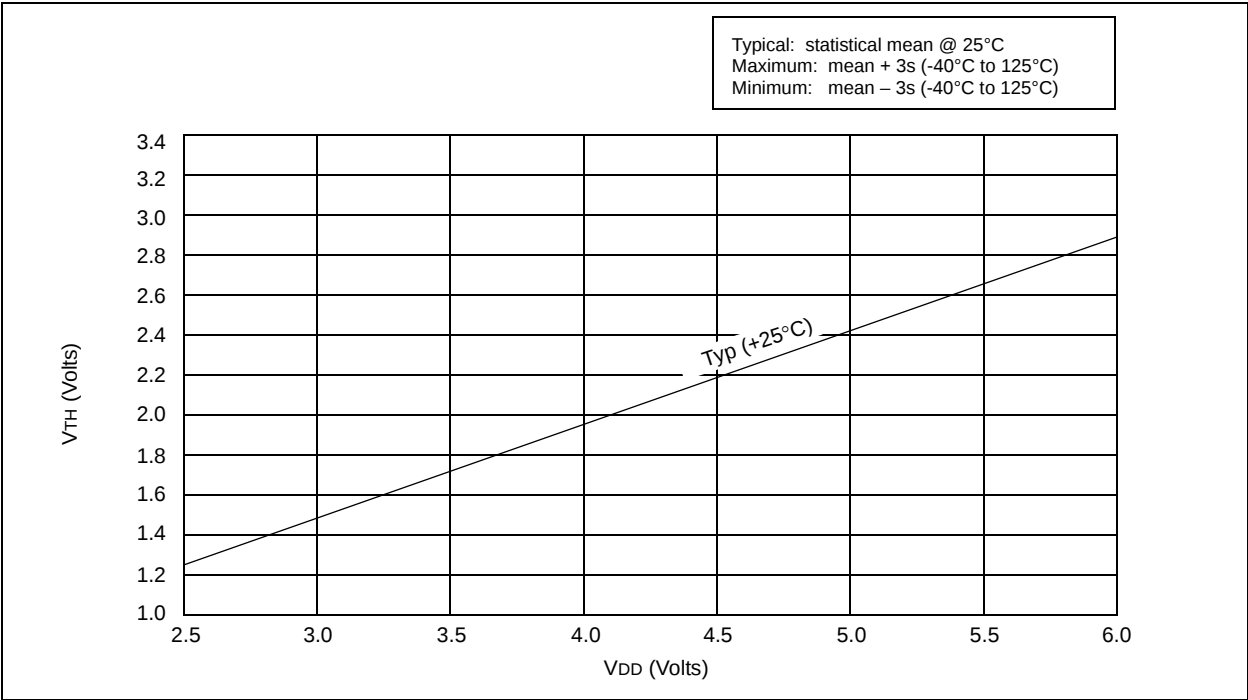


FIGURE 18-11: TYPICAL I_{DD} vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, 25°C)

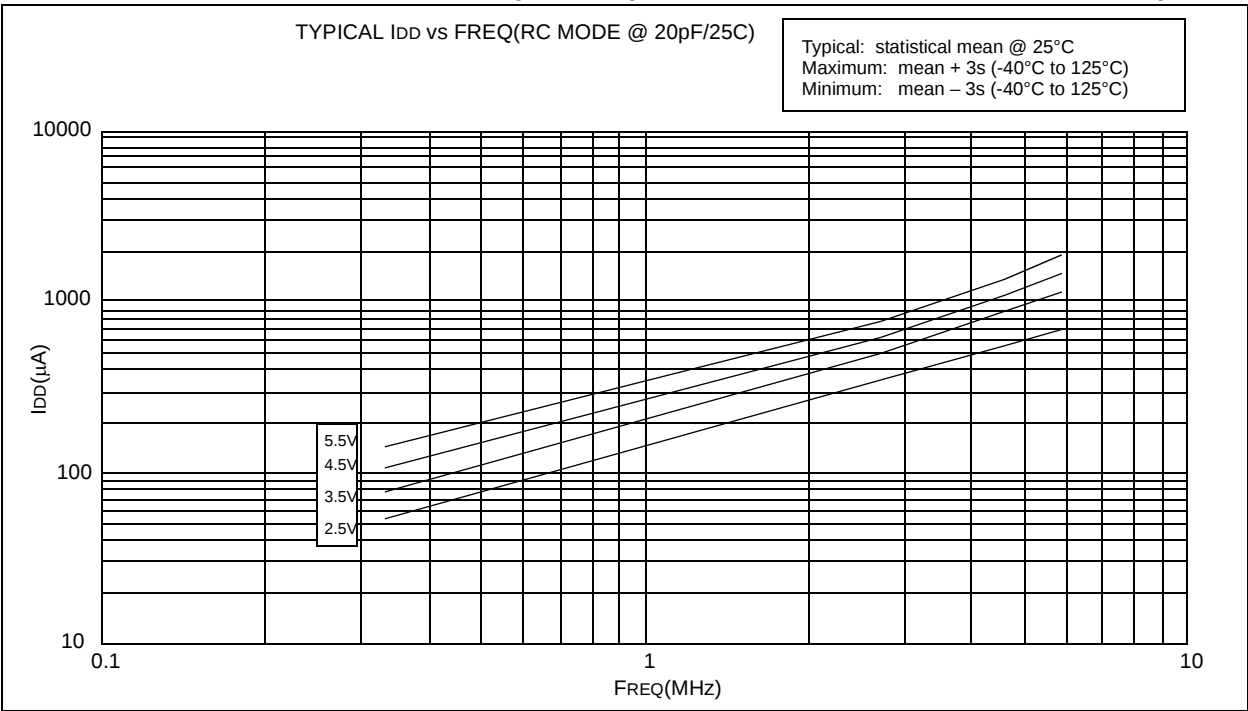


FIGURE 19-4: CLKOUT AND I/O TIMING - PIC16C5X-40

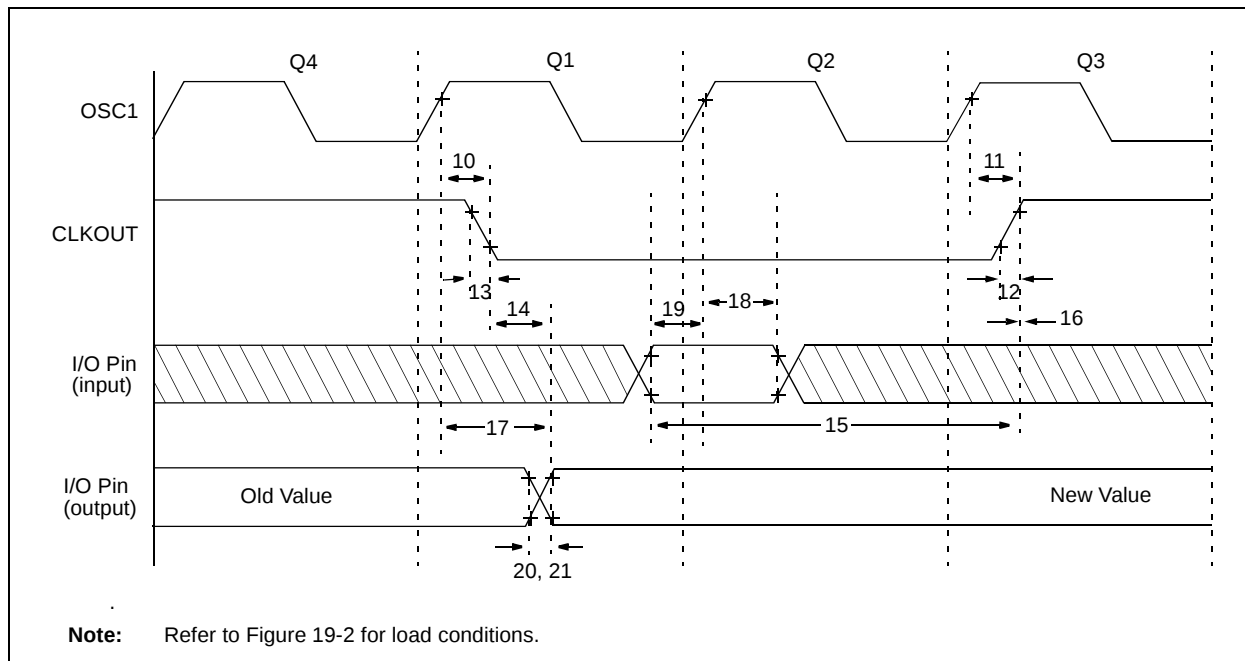


TABLE 19-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X-40

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ^(1,2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ^(1,2)	—	15	30**	ns
12	TckR	CLKOUT rise time ^(1,2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time ^(1,2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ^(1,2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ^(1,2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ ^(1,2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽²⁾	—	—	100	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽²⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Refer to Figure 19-2 for load conditions.

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XORWF 60

Z

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NOTES: