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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	24 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c55-hsi-sp

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TABLE 1-1: PIC16C5X FAMILY OF DEVICES

Features	PIC16C54	PIC16CR54	PIC16C55	PIC16C56	PIC16CR56					
Maximum Operation Frequency	40 MHz	20 MHz	40 MHz	40 MHz	20 MHz					
EPROM Program Memory (x12 words)	512	—	512	1K	—					
ROM Program Memory (x12 words)	—	512	—	—	1K					
RAM Data Memory (bytes)	25	25	24	25	25					
Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0					
I/O Pins	12	12	20	12	12					
Number of Instructions	33	33	33	33	33					
Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP					
All PIC [®] Family devices have Power-on I/O current capability.	All PIC [®] Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high									

PIC16C58 Features **PIC16C57** PIC16CR57 PIC16CR58 Maximum Operation Frequency 20 MHz 40 MHz 40 MHz 20 MHz EPROM Program Memory (x12 words) 2K 2K ____ _ ROM Program Memory (x12 words) 2K 2K _ _ RAM Data Memory (bytes) 72 72 73 73 Timer Module(s) TMR0 TMR0 TMR0 TMR0 I/O Pins 20 20 12 12 Number of Instructions 33 33 33 33 28-pin DIP, SOIC; 28-pin DIP, SOIC; 18-pin DIP, SOIC; 18-pin DIP, SOIC; Packages 28-pin SSOP 28-pin SSOP 20-pin SSOP 20-pin SSOP All PIC® Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A twostage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle except for program branches.

The PIC16C54/CR54 and PIC16C55 address 512 x 12 of program memory, the PIC16C56/CR56 address 1K x 12 of program memory, and the PIC16C57/CR57 and PIC16C58/CR58 address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly. The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 (for PIC16C54/56/58) and Table 3-2 (for PIC16C55/57).

	Pi	n Numb	er	Pin	Buffer	
Pin Name	DIP	SOIC	SSOP	Туре	Туре	Description
RA0	17	17	19	I/O	TTL	Bi-directional I/O port
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RB0	6	6	7	I/O	TTL	Bi-directional I/O port
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	
RB5	11	11	12	I/O	TTL	
RB6	12	12	13	I/O	TTL	
RB7	13	13	14	I/O	TTL	
TOCKI	3	3	3	I	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in use, to reduce current consumption.
MCLR/Vpp	4	4	4	I	ST	Master clear (RESET) input/programming voltage input. This pin is an active low RESET to the device. Voltage on the MCLR/VPP pin must not exceed VDD to avoid unin- tended entering of Programming mode.
OSC1/CLKIN	16	16	18	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	17	0		Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
Vdd	14	14	15,16	Р	_	Positive supply for logic and I/O pins.
Vss	5	5	5,6	Р	_	Ground reference for logic and I/O pins.

TABLE 3-1:PINOUT DESCRIPTION - PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16CR58,
PIC16CR58

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

3.1 **Clocking Scheme/Instruction** Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2 and Example 3-1.

3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).



FIGURE 3-2: **CLOCK/INSTRUCTION CYCLE**

EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



is "flushed" from the pipeline, while the new instruction is being fetched and then executed.

TABLE 5-3: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-On Reset	MCLR or WDT Reset
W	N/A	xxxx xxxx	uuuu uuuu
TRIS	N/A	1111 1111	1111 1111
OPTION	N/A	11 1111	11 1111
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	XXXX XXXX	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000q quuu
FSR ⁽¹⁾	04h	1xxx xxxx	luuu uuuu
PORTA	05h	xxxx	uuuu
PORTB	06h	XXXX XXXX	uuuu uuuu
PORTC ⁽²⁾	07h	XXXX XXXX	uuuu uuuu
General Purpose Register Files	07-7Fh	xxxx xxxx	սսսս սսսս

Legend: x = unknown u = unchanged - = unimplemented, read as '0'<math>q = see tables in Table 5-1 for possible values.

- Note 1: These values are valid for PIC16C57/CR57/CR58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for MCLR and WDT Reset, the value is 111u uuuu.
 - **2:** General purpose register file on PIC16C54/CR54/C56/CR56/C58/CR58.

FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the MCLR/VPP pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is <u>RESET</u>. The DRT timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where MCLR is not tied to VDD is shown in Figure 5-3. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset TDRT msec after MCLR goes high.

In Figure 5-4, the on-chip Power-On Reset feature is being used (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the MCLR/VPP pin, and when the MCLR/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

Note: When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the <u>Embedded Control Handbook</u>.

The POR circuit does not produce an internal RESET when VDD declines.

FIGURE 5-2:

EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 k Ω will limit any current flowing into \overline{MCLR} from external capacitor C in the event of \overline{MCLR} pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

6.0 MEMORY ORGANIZATION

PIC16C5X memory is organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one or two STATUS Register bits. For devices with a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Selection Register (FSR).

6.1 Program Memory Organization

The PIC16C54, PIC16CR54 and PIC16C55 have a 9bit Program Counter (PC) capable of addressing a 512 x 12 program memory space (Figure 6-1). The PIC16C56 and PIC16CR56 have a 10-bit Program Counter (PC) capable of addressing a 1K x 12 program memory space (Figure 6-2). The PIC16CR57, PIC16C58 and PIC16CR58 have an 11-bit Program Counter capable of addressing a 2K x 12 program memory space (Figure 6-3). Accessing a location above the physically implemented address will cause a wraparound.

A NOP at the RESET vector location will cause a restart at location 000h. The RESET vector for the PIC16C54, PIC16CR54 and PIC16C55 is at 1FFh. The RESET vector for the PIC16C56 and PIC16CR56 is at 3FFh. The RESET vector for the PIC16C57, PIC16CR57, PIC16C58, and PIC16CR58 is at 7FFh. See Section 6.5 for additional information using CALL and GOTO instructions.

FIGURE 6-1: PIC16C54/CR54/C55 PROGRAM MEMORY MAP AND STACK



FIGURE 6-2:

PIC16C56/CR56 PROGRAM MEMORY MAP AND STACK



FIGURE 6-3:

PIC16C57/CR57/C58/ CR58 PROGRAM MEMORY MAP AND STACK



9.1 Configuration Bits

Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. Nine bits are code protection bits for the PIC16C54A, PIC16CR54A, PIC16C55A, PIC16C56A, PIC16CR56A, PIC16CR57C, PIC1

PIC16C58B, and PIC16CR58B devices (Register 9-1). One bit is for code protection for the PIC16C54, PIC16C55, PIC16C56 and PIC16C57 devices (Register 9-2).

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" diagrams in the back of this data sheet).

REGISTER 9-1: CONFIGURATION WORD FOR PIC16C54A/CR54A/C54C/CR54C/C55A/C56A/ CR56A/C57C/CR57C/C58B/CR58B

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0
bit 11											bit 0

bit 11-3: CP: Code Protection Bit

- 1 = Code protection off
 - 0 =Code protection on
- bit 2: WDTE: Watchdog timer enable bit
 - 1 = WDT enabled
 - 0 = WDT disabled

bit 1-0: FOSC1:FOSC0: Oscillator Selection Bit

- 00 = LP oscillator
- 01 = XT oscillator
- 10 = HS oscillator
- 11 = RC oscillator

Note 1: Refer to the PIC16C5X Programming Specification (Literature Number DS30190) to determine how to access the configuration word.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

12.3 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

PIC16C (Exten	PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended						
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions			
D001	Vdd	Supply Voltage PIC16C5X-RCE PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-LPE	3.25 3.25 4.5 4.5 2.5		6.0 6.0 5.5 5.5 6.0	V V V V V				
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	_	V	Device in SLEEP mode			
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset			
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset			
D010	IDD	Supply Current ⁽²⁾ PIC16C5X-RCE ⁽³⁾ PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-HSE PIC16C5X-LPE		1.8 1.8 4.8 9.0 19	3.3 3.3 10 10 20 55	mA mA mA mA μA	Fosc = 4 MHz, VDD = $5.5V$ Fosc = 4 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 16 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $3.25V$, WDT disabled			
D020	IPD	Power-down Current ⁽²⁾	_	5.0 0.8	22 18	μΑ μΑ	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled			

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .



FIGURE 12-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING -PIC16C54/55/56/57

TABLE 12-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57

AC CharacteristicsStandard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended							
Param No.	Symbol	Characteristic Min Typ† Max Units Condit					
30	TmcL	MCLR Pulse Width (low)	100*	—		ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low		_	100*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 12-5: TIMER0 CLOCK TIMINGS - PIC16C54/55/56/57



TABLE 12-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54/55/56/57

AC Ch	AC CharacteristicsStandard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended									
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions			
40	Tt0H	TOCKI High Pulse Width - No Prescaler - With Prescaler	0.5 Tcy + 20* 10*		_	ns ns				
41	TtOL	T0CKI Low Pulse Width - No Prescaler - With Prescaler	0.5 Tcy + 20* 10*			ns ns				
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> * N	_	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)			

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



FIGURE 14-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD



15.2 DC Characteristics: PIC16

PIC16C54A-04E, 10E, 20E (Extended) PIC16LC54A-04E (Extended)

PIC16L (Extend	C54A-04E ded)	1	Standa Opera	ard Ope ting Terr	rating	j Condi ure	tions (unless otherwise specified) $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended
PIC16C54A-04E, 10E, 20E (Extended)				ard Ope ting Terr	rating	j Condi ure	tions (unless otherwise specified) $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
	IPD	Power-down Current ⁽²⁾					
D020		PIC16LC54A	—	2.5	15	μΑ	VDD = 2.5V, WDT enabled,
			_	0.25	7.0	μA	Extended VDD = 2.5V, WDT disabled, Extended
D020A		PIC16C54A	—	5.0	22	μA	VDD = 3.5V, WDT enabled
				0.8	18^	μΑ	VDD = $3.5V$, VVD I disabled

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- **Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

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NOTES:



FIGURE 16-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD



17.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended) PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

PIC160 PIC160 (Exter	54C/C55/ R54C/CR nded)	A/C56A/C57C/C58B-04E, 20E 56A/CR57C/CR58B-04E, 20E	Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended						
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions		
D001	Vdd	Supply Voltage	3.0 4.5		5.5 5.5	V V	RC, XT, LP, and HS mode from 0 - 10 MHz from 10 - 20 MHz		
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode		
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset		
D010	IDD	Supply Current ⁽²⁾ XT and RC ⁽³⁾ modes HS mode	_	1.8 9.0	3.3 20	mA mA	Fosc = 4.0 MHz, Vdd = 5.5V Fosc = 20 MHz, Vdd = 5.5V		
D020	IPD	Power-down Current ⁽²⁾		0.3 10 12 4.8 18 26	17 50* 60* 31* 68* 90*	μΑ μΑ μΑ μΑ μΑ	VDD = 3.0V, WDT disabled VDD = 4.5V, WDT disabled VDD = 5.5V, WDT disabled VDD = 3.0V, WDT enabled VDD = 4.5V, WDT enabled VDD = 5.5V, WDT enabled		

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.



FIGURE 17-8: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X, PIC16CR5X

TABLE 17-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X, PIC16CR5X

$\label{eq:AC Characteristics} \begin{tabular}{lllllllllllllllllllllllllllllllllll$							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1000*		—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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PIC16C5X

FIGURE 19-1: PIC16C54C/C55A/C56A/C57C/C58B-40 VOLTAGE-FREQUENCY GRAPH, $0^{\circ}C \le T_A \le +70^{\circ}C$





- **2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
- **3:** Operation between 20 to 40 MHz requires the following:
 - VDD between 4.5V. and 5.5V
 - OSC1 externally driven
 - OSC2 not connected
 - HS mode
 - Commercial temperatures

Devices qualified for 40 MHz operation have -40 designation (ex: PIC16C54C-40/P).

4: For operation between DC and 20 MHz, see Section 17.1.



FIGURE 19-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X-40

TABLE 19-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X-40

AC Characteristics		Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial)Operating Voltage VDD range is described in Section 19.1.					
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1000*		_	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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