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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	24 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c55-lpi-ss

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4.4 RC Oscillator

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (R_{EXT}) and capacitor (C_{EXT}) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low C_{EXT} values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 4-5 shows how the R/C combination is connected to the PIC16C5X. For R_{EXT} values below 2.2 k Ω , the oscillator operation may become unstable, or stop completely. For very high R_{EXT} values (e.g., 1 M Ω) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping R_{EXT} between 3 k Ω and 100 k Ω .

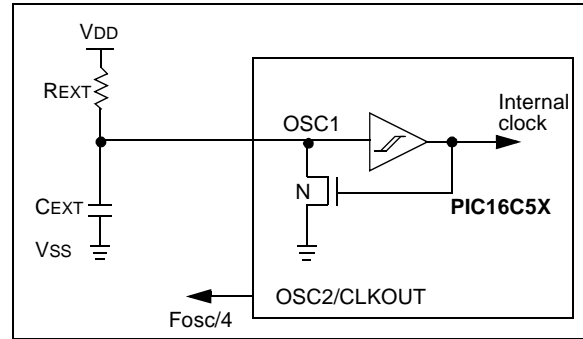
Although the oscillator will operate with no external capacitor ($C_{EXT} = 0$ pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications sections for variation of oscillator frequency due to V_{DD} for given R_{EXT}/C_{EXT} values as well as frequency variation due to operating temperature for given R, C, and V_{DD} values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic.

FIGURE 4-5: RC OSCILLATOR MODE



Note: If you change from this device to another device, please verify oscillator characteristics in your application.

5.2 Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides an 18 ms nominal time-out on RESET regardless of Oscillator mode used. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows VDD to rise above VDD min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after the voltage on the MCLR/VPP pin has reached a logic high (VIH) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The Device Reset time delay will vary from chip to chip due to VDD, temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the PIC16C5X from SLEEP mode automatically.

5.3 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be RESET in the event of a brown-out.

To RESET PIC16C5X devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 5-6, Figure 5-7 and Figure 5-8.

FIGURE 5-6: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1

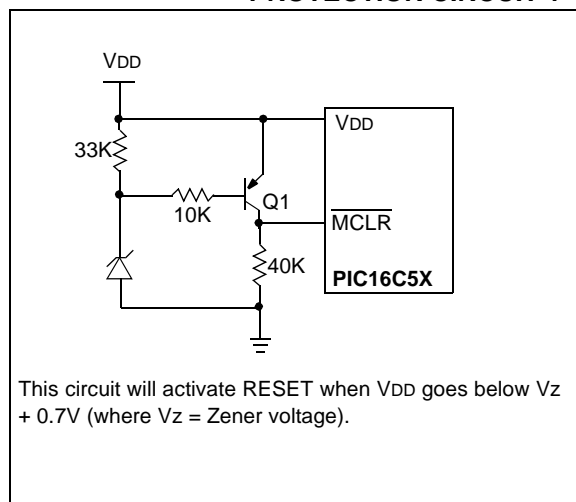


FIGURE 5-7: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2

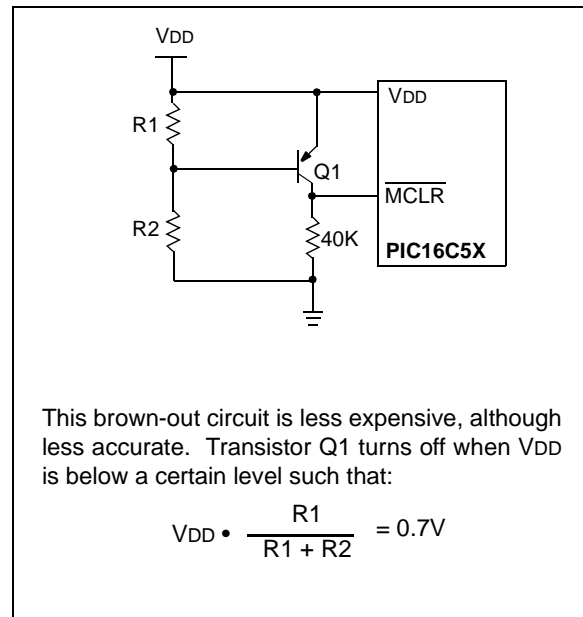
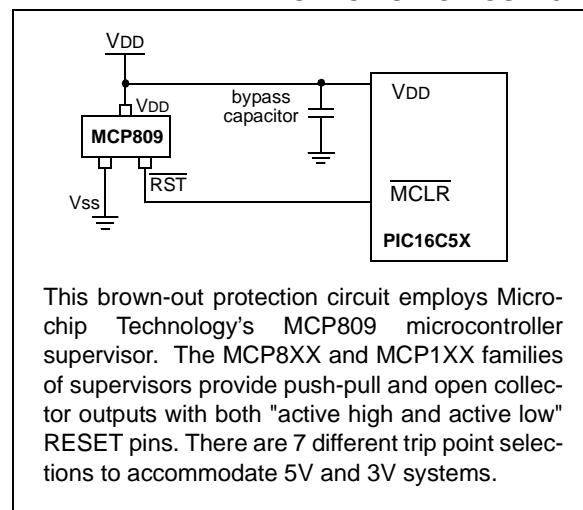


FIGURE 5-8: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



PIC16C5X

9.1 Configuration Bits

Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. Nine bits are code protection bits for the PIC16C54A, PIC16CR54A, PIC16C54C, PIC16CR54C, PIC16C55A, PIC16C56A, PIC16CR56A, PIC16C57C, PIC16CR57C,

PIC16C58B, and PIC16CR58B devices (Register 9-1). One bit is for code protection for the PIC16C54, PIC16C55, PIC16C56 and PIC16C57 devices (Register 9-2).

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" diagrams in the back of this data sheet).

REGISTER 9-1: CONFIGURATION WORD FOR PIC16C54A/CR54A/C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0
bit 11										bit 0	

bit 11-3: **CP**: Code Protection Bit

1 = Code protection off
0 = Code protection on

bit 2: **WDTE**: Watchdog timer enable bit

1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection Bit

00 = LP oscillator
01 = XT oscillator
10 = HS oscillator
11 = RC oscillator

Note 1: Refer to the PIC16C5X Programming Specification (Literature Number DS30190) to determine how to access the configuration word.

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

1 = bit is set

0 = bit is cleared

x = bit is unknown

PIC16C5X

IORLW Inclusive OR literal with W

Syntax: [*label*] IORLW *k*
Operands: $0 \leq k \leq 255$
Operation: (W) .OR. (*k*) \rightarrow (W)
Status Affected: Z
Encoding:

1101	kkkk	kkkk
------	------	------

Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.
Words: 1
Cycles: 1
Example: IORLW 0x35

Before Instruction
W = 0x9A
After Instruction
W = 0xBF
Z = 0

IORWF Inclusive OR W with f

Syntax: [*label*] IORWF *f*,*d*
Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
Operation: (W).OR. (*f*) \rightarrow (*dest*)
Status Affected: Z
Encoding:

0001	00df	ffff
------	------	------

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
Words: 1
Cycles: 1
Example: IORWF RESULT, 0

Before Instruction
RESULT = 0x13
W = 0x91
After Instruction
RESULT = 0x13
W = 0x93
Z = 0

MOVF Move f

Syntax: [*label*] MOVF *f*,*d*
Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
Operation: (*f*) \rightarrow (*dest*)
Status Affected: Z
Encoding:

0010	00df	ffff
------	------	------

Description: The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.
Words: 1
Cycles: 1
Example: MOVF FSR, 0

After Instruction
W = value in FSR register

MOVLW Move Literal to W

Syntax: [*label*] MOVLW *k*
Operands: $0 \leq k \leq 255$
Operation: *k* \rightarrow (W)
Status Affected: None
Encoding:

1100	kkkk	kkkk
------	------	------

Description: The eight bit literal 'k' is loaded into the W register.
Words: 1
Cycles: 1
Example: MOVLW 0x5A

After Instruction
W = 0x5A

11.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
 - MPASM™ Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
 - MPLAB ICD
- Device Programmers
 - PRO MATE® II Universal Device Programmer
 - PICSTART® Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
 - PICDEM™ 1 Demonstration Board
 - PICDEM 2 Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 17 Demonstration Board
 - KEELQ® Demonstration Board

11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows®-based application that contains:

- An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file
 - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

11.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
1	TOSC	External CLKIN Period ⁽¹⁾	250	—	—	ns	XT osc mode
			100	—	—	ns	10 MHz mode
			50	—	—	ns	HS osc mode (Comm/Ind)
			62.5	—	—	ns	HS osc mode (Ext)
			25	—	—	μs	LP osc mode
		Oscillator Period ⁽¹⁾	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			100	—	250	ns	10 MHz mode
			50	—	250	ns	HS osc mode (Comm/Ind)
			62.5	—	250	ns	HS osc mode (Ext)
			25	—	—	μs	LP osc mode
2	Tcy	Instruction Cycle Time ⁽²⁾	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

FIGURE 14-4: TYPICAL RC OSC
FREQUENCY vs. VDD,
CEXT = 300 PF

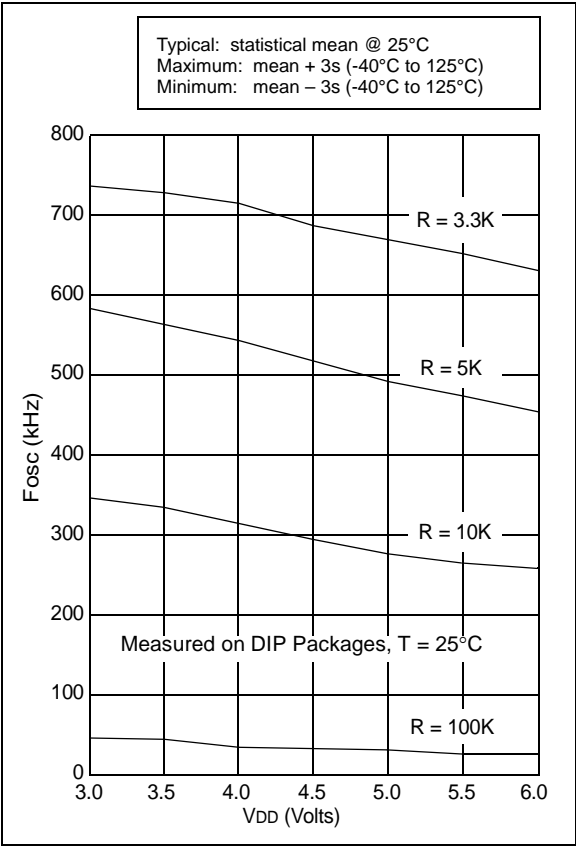


FIGURE 14-5: TYPICAL IPD vs. VDD,
WATCHDOG DISABLED

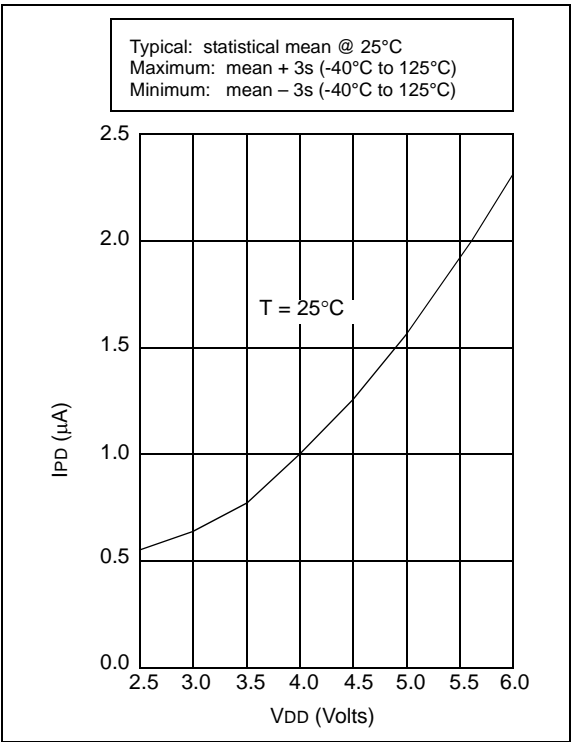


FIGURE 14-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

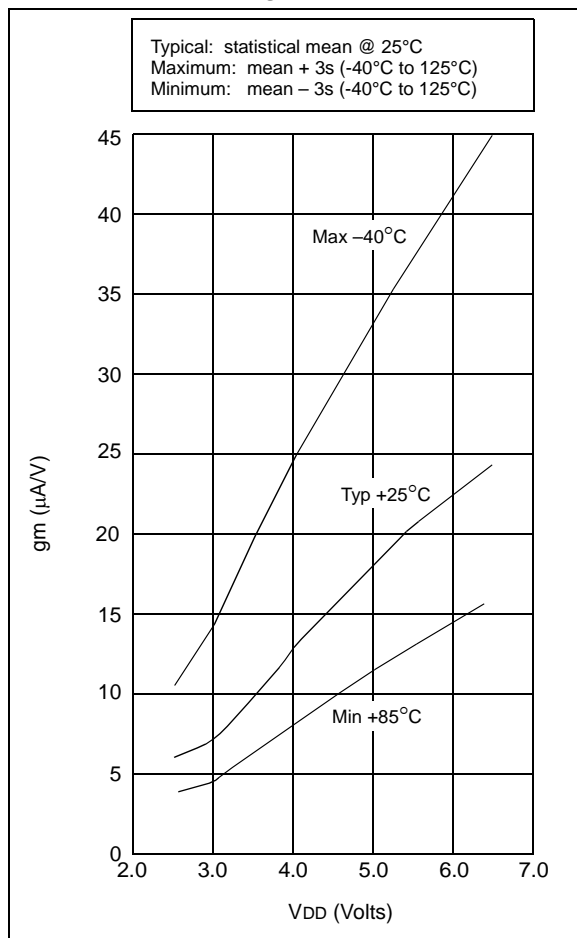
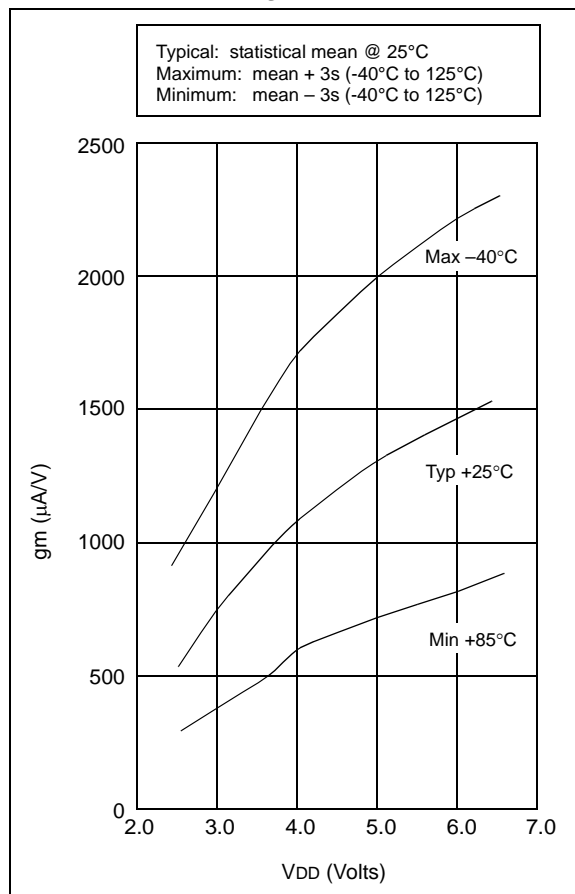


FIGURE 14-18: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD



15.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended) PIC16LC54A-04E (Extended)

PIC16LC54A-04E (Extended)		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
PIC16C54A-04E, 10E, 20E (Extended)		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D020	IPD	Power-down Current⁽²⁾					
		PIC16LC54A	—	2.5	15	μA	$V_{DD} = 2.5\text{V}$, WDT enabled, Extended
			—	0.25	7.0	μA	$V_{DD} = 2.5\text{V}$, WDT disabled, Extended
D020A		PIC16C54A	—	5.0	22	μA	$V_{DD} = 3.5\text{V}$, WDT enabled
			—	0.8	18*	μA	$V_{DD} = 3.5\text{V}$, WDT disabled

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C . This data is for design guidance only and is not tested.

Note 1: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all I_{DD} measurements in active Operation mode are: $OSC1$ = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS} , $T0CKI = V_{DD}$, $MCLR = V_{DD}$; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through R_{EXT} . The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in $k\Omega$.

15.6 Timing Diagrams and Specifications

FIGURE 15-2: EXTERNAL CLOCK TIMING - PIC16C54A

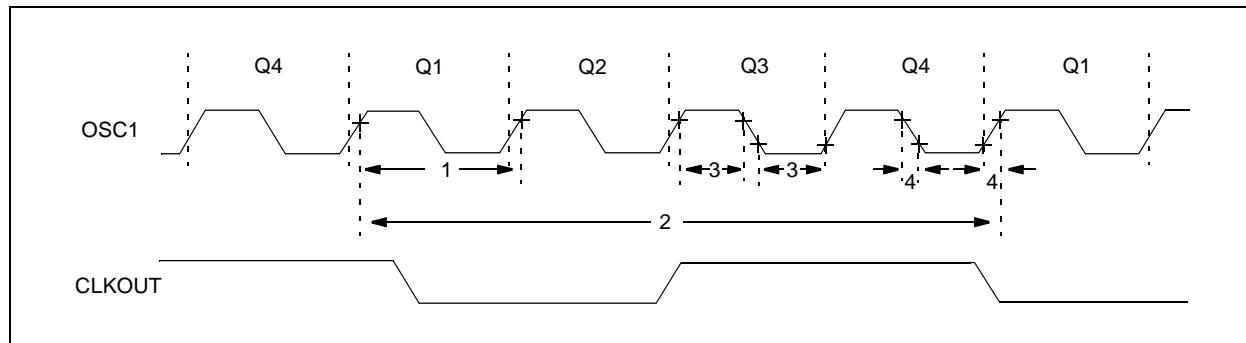


TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-20^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial - PIC16LV54A-02I $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended							
AC Characteristics							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency ⁽¹⁾	DC	—	4.0	MHz	XT osc mode
			DC	—	2.0	MHz	XT osc mode (PIC16LV54A)
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency ⁽¹⁾	DC	—	4.0	MHz	RC osc mode
			DC	—	2.0	MHz	RC osc mode (PIC16LV54A)
			0.1	—	4.0	MHz	XT osc mode
			0.1	—	2.0	MHz	XT osc mode (PIC16LV54A)
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	10	MHz	HS osc mode (10)
			4.0	—	20	MHz	HS osc mode (20)
			5.0	—	200	kHz	LP osc mode

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

PIC16C5X

FIGURE 15-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A

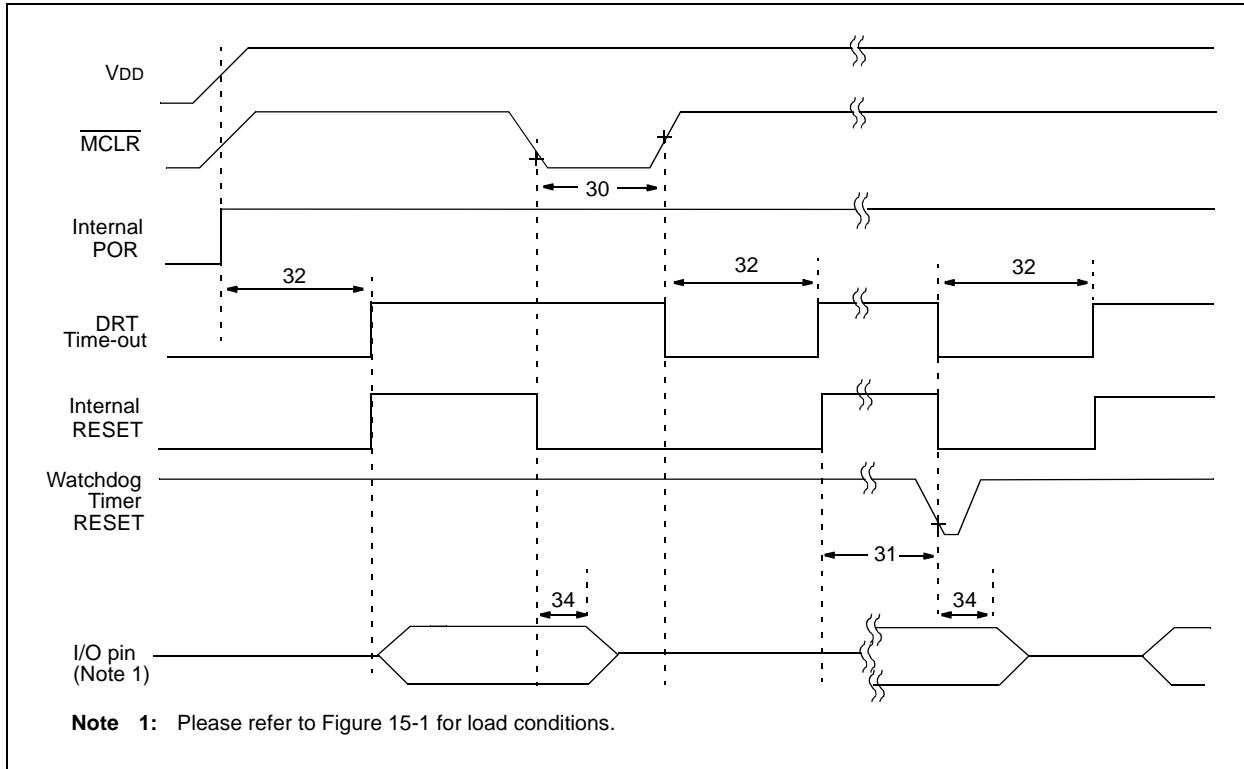


TABLE 15-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics							
		Operating Temperature					
		0°C ≤ TA ≤ +70°C for commercial					
		-40°C ≤ TA ≤ +85°C for industrial					
		-20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I					
		-40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	100* 1	— —	— —	ns μs	VDD = 5.0V VDD = 5.0V (PIC16LV54A only)
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	TioZ	I/O Hi-impedance from MCLR Low	— —	— —	100* 1μs	ns —	(PIC16LV54A only)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 16-7: V_{TH} (INPUT THRESHOLD VOLTAGE) OF I/O PINS - V_{DD}

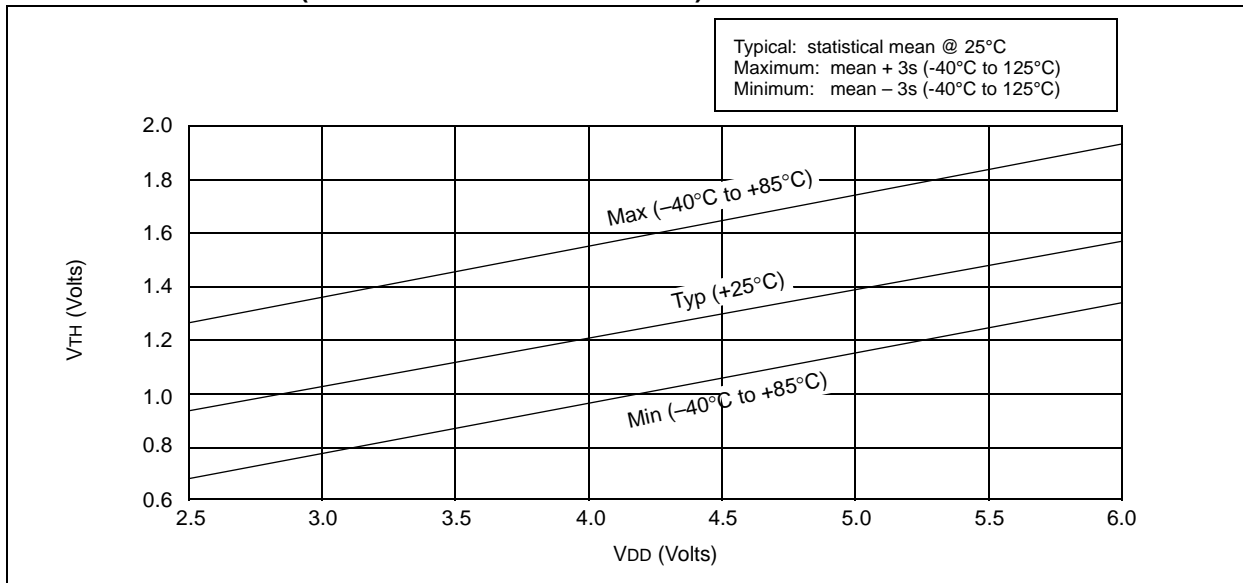


FIGURE 16-8: V_{TH} (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. V_{DD}

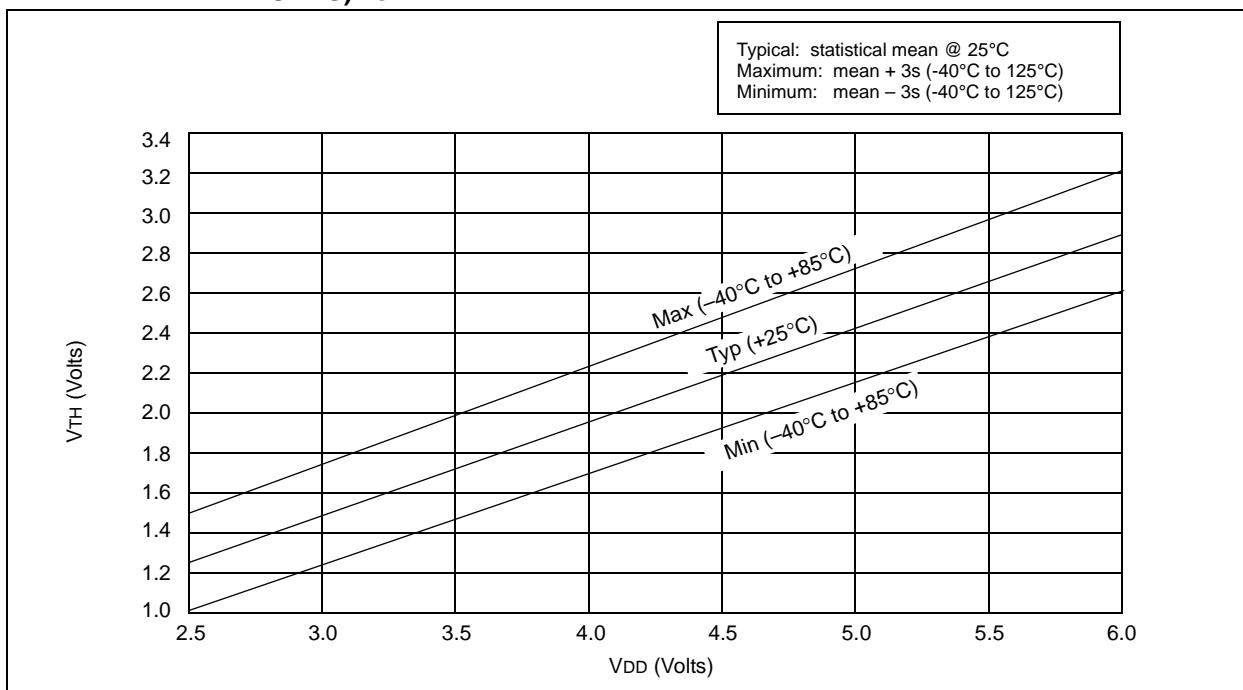


FIGURE 16-20: PORTA, B AND C I_{OH} vs. V_{OH} , $V_{DD} = 3V$

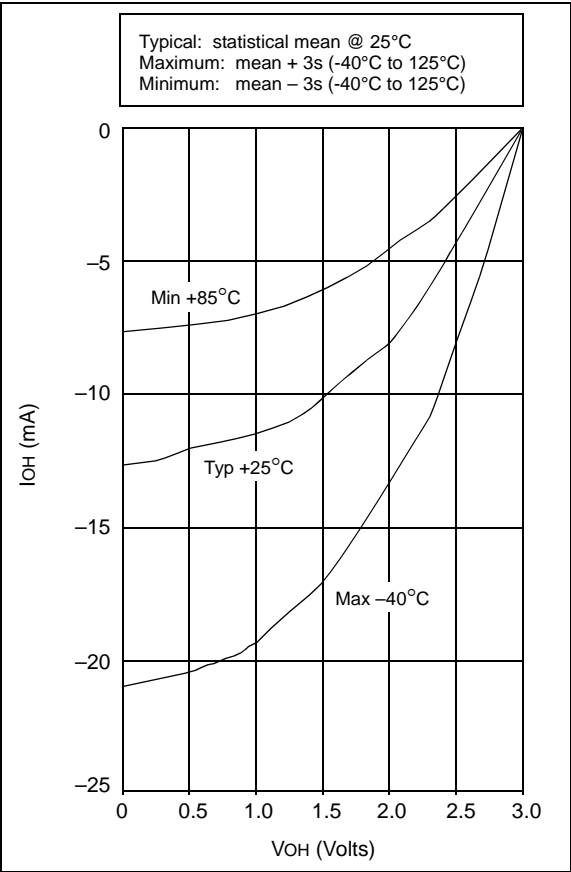
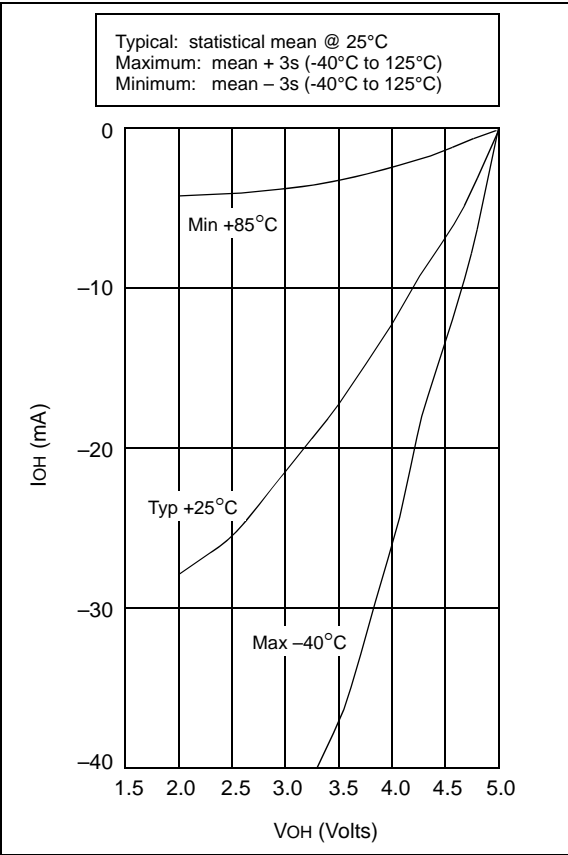


FIGURE 16-21: PORTA, B AND C I_{OH} vs. V_{OH} , $V_{DD} = 5V$



17.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended) PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)				Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended			
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	3.0 4.5	— —	5.5 5.5	V V	RC, XT, LP, and HS mode from 0 - 10 MHz from 10 - 20 MHz
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current ⁽²⁾ XT and RC ⁽³⁾ modes HS mode	— —	1.8 9.0	3.3 20	mA mA	FOSC = 4.0 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V
D020	IPD	Power-down Current ⁽²⁾	— — — — — —	0.3 10 12 4.8 18 26	17 50* 60* 31* 68* 90*	μA μA μA μA μA μA	VDD = 3.0V, WDT disabled VDD = 4.5V, WDT disabled VDD = 5.5V, WDT disabled VDD = 3.0V, WDT enabled VDD = 4.5V, WDT enabled VDD = 5.5V, WDT enabled

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{EXT}$ (mA) with REXT in kΩ.

PIC16C5X

FIGURE 17-7: CLKOUT AND I/O TIMING - PIC16C5X, PIC16CR5X

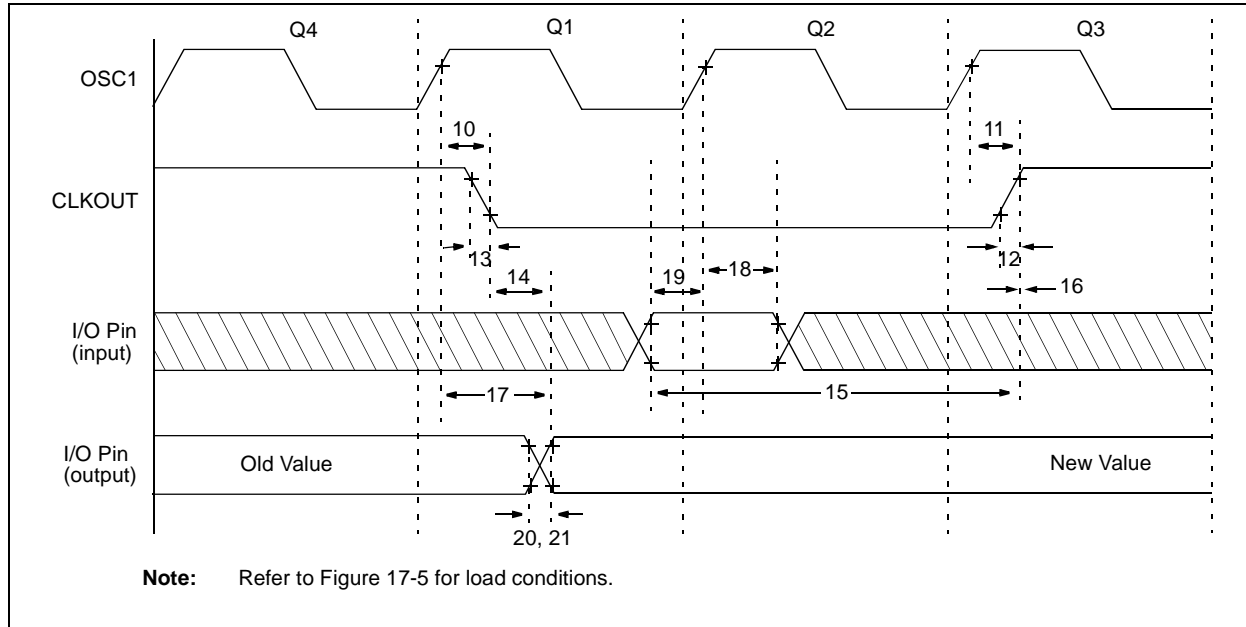


TABLE 17-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature				
		0°C ≤ TA ≤ +70°C for commercial				
		-40°C ≤ TA ≤ +85°C for industrial				
		-40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽¹⁾	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ ⁽¹⁾	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽²⁾	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽²⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

2: Refer to Figure 17-5 for load conditions.

FIGURE 18-6: TYPICAL I_{PD} vs. V_{DD} , WATCHDOG ENABLED (25°C)

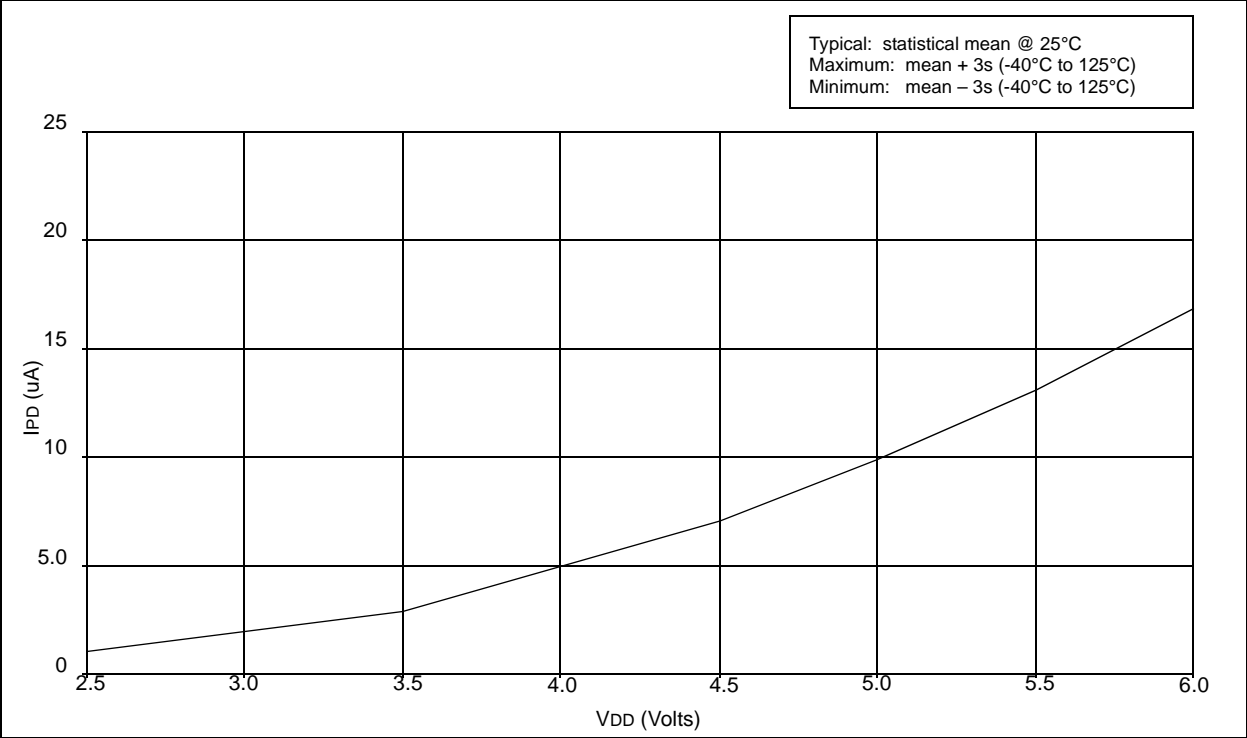
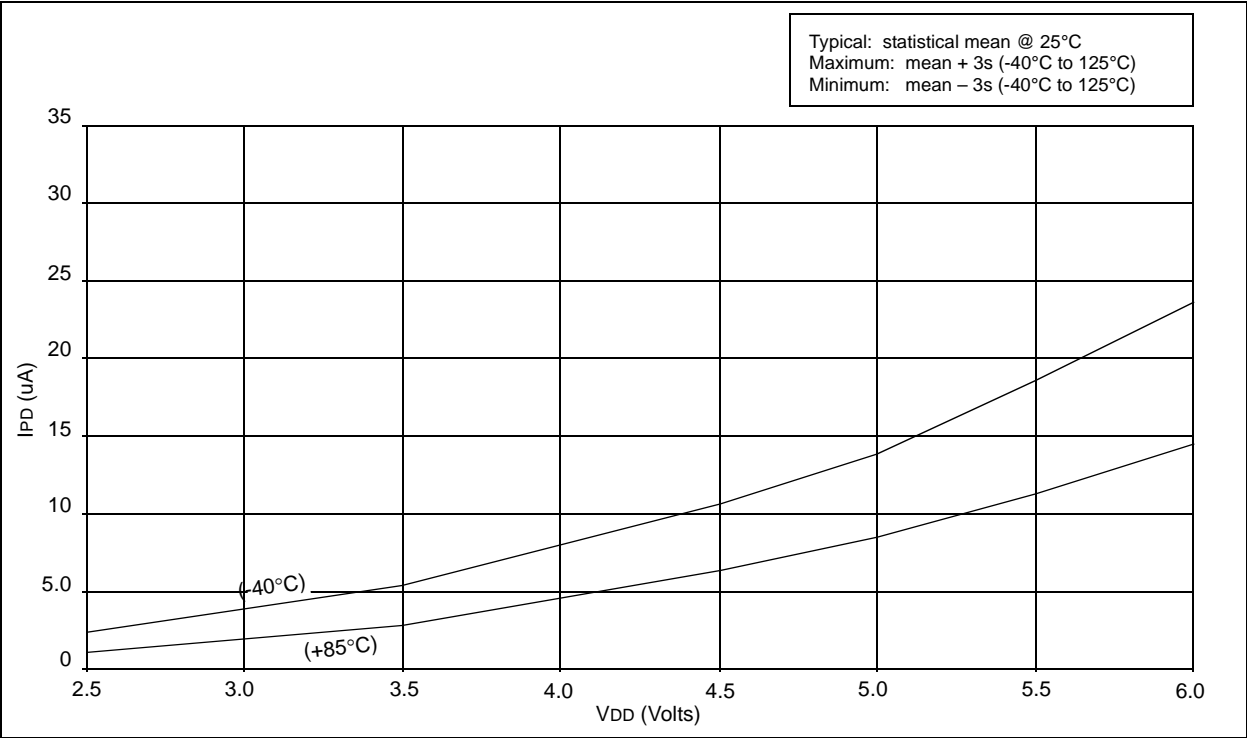


FIGURE 18-7: TYPICAL I_{PD} vs. V_{DD} , WATCHDOG ENABLED (-40°C, 85°C)

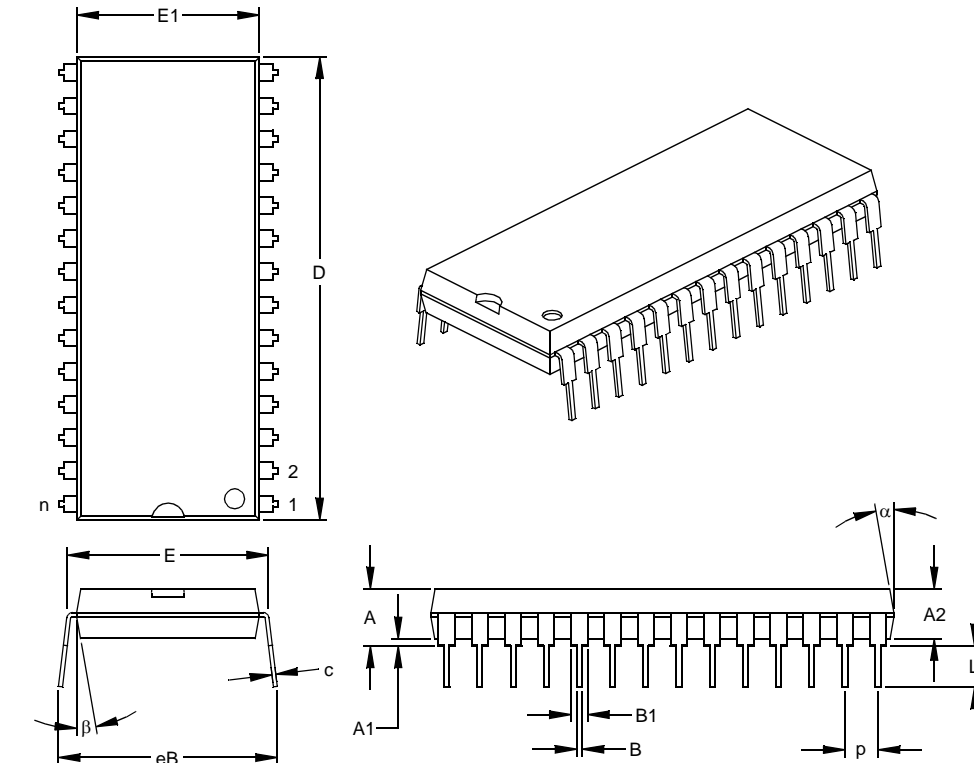


PIC16C5X

NOTES:

28-Lead Plastic Dual In-line (P) – 600 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.175	.190	4.06	4.45	4.83
Molded Package Thickness	A2	.140	.150	.160	3.56	3.81	4.06
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88
Molded Package Width	E1	.505	.545	.560	12.83	13.84	14.22
Overall Length	D	1.395	1.430	1.465	35.43	36.32	37.21
Tip to Seating Plane	L	.120	.130	.135	3.05	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.030	.050	.070	0.76	1.27	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§	.620	.650	.680	15.75	16.51	17.27
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-011

Drawing No. C04-079

APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

1. Check any `CALL`, `GOTO` or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change RESET vector to proper value for processor used.
6. Remove any use of the `ADDLW`, `RETURN` and `SUBLW` instructions.
7. Rewrite any code segments that use interrupts.

APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.