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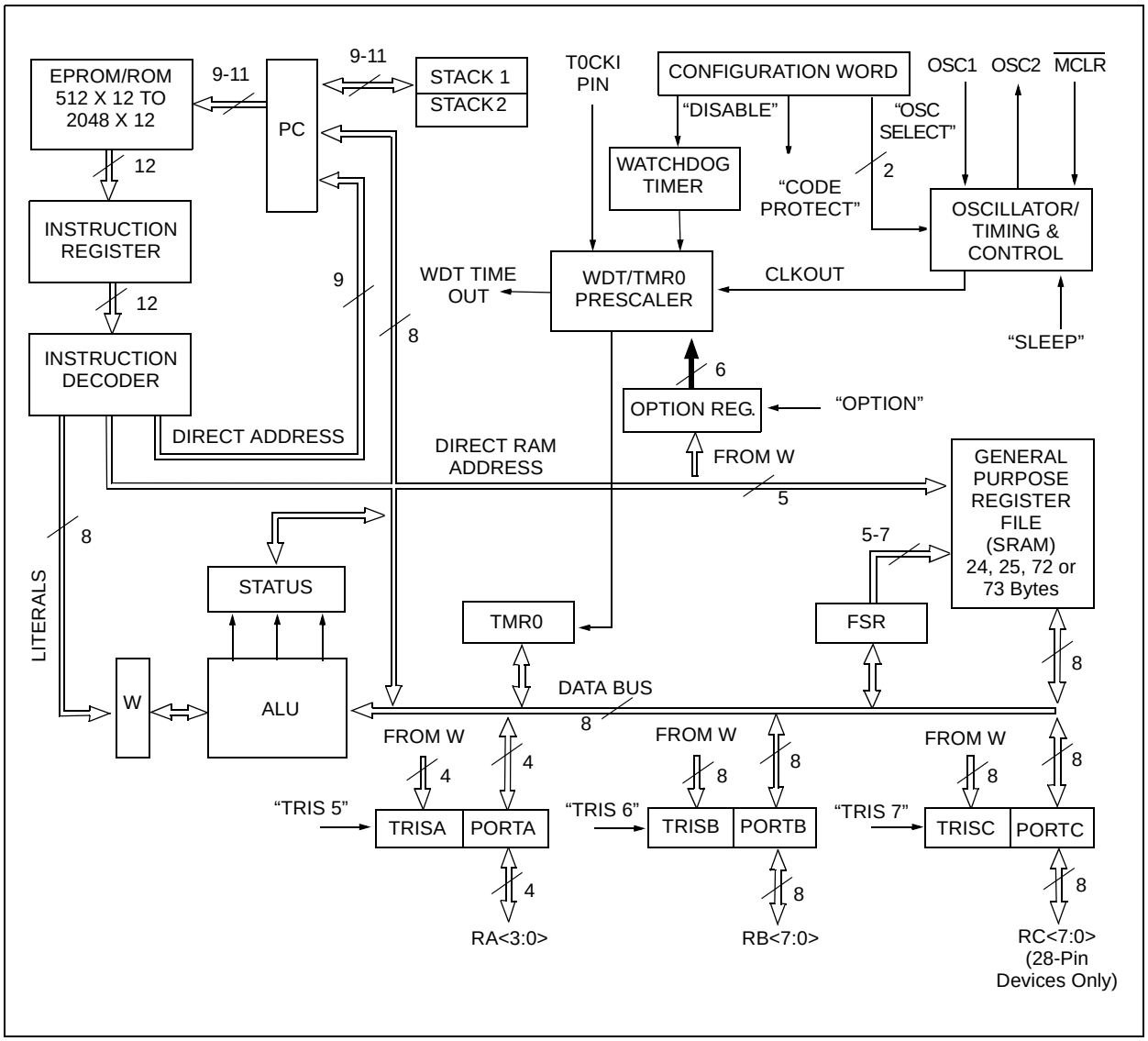
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 20 |
| Program Memory Size | 768B (512 x 12) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 24 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 6.25V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16c55-rc-ss |

**FIGURE 3-1: PIC16C5X SERIES BLOCK DIAGRAM**



### 6.5.1 PAGING CONSIDERATIONS – PIC16C56/CR56, PIC16C57/CR57 AND PIC16C58/CR58

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS Register will not be updated. Therefore, the next GOTO, CALL or modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA<1:0>).

For example, a NOP at location 1FFh (page 0) increments the PC to 200h (page 1). A GOTO xxx at 200h will return the program to address xxh on page 0 (assuming that PA<1:0> are clear).

To prevent this, the page preselect bits must be updated under program control.

### 6.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the RESET vector).

The STATUS Register page preselect bits are cleared upon a RESET, which means that page 0 is preselected.

Therefore, upon a RESET, a GOTO instruction at the RESET vector location will automatically cause the program to jump to page 0.

## 6.6 Stack

PIC16C5X devices have a 10-bit or 11-bit wide, two-level hardware push/pop stack.

A CALL instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W Register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the RETLW instruction, the PC is loaded with the Top of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC, therefore, paging is not an issue when returning from a subroutine.

## 12.1 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial)

| **PIC16C54/55/56/57-RC, XT, 10, HS, LP** (Commercial) | | | **Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | | | | | |
| | | PIC16C5X-RC | 3.0 | — | 6.25 | V | |
| | | PIC16C5X-XT | 3.0 | — | 6.25 | V | |
| | | PIC16C5X-10 | 4.5 | — | 5.5 | V | |
| | | PIC16C5X-HS | 4.5 | — | 5.5 | V | |
| | | PIC16C5X-LP | 2.5 | — | 6.25 | V | |
| D002 | VDR | **RAM Data Retention Voltage(1)** | | 1.5* | — | V | Device in SLEEP Mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | | VSS | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D010 | IDD | **Supply Current(2)** | | | | | |
| | | PIC16C5X-RC(3) | — | 1.8 | 3.3 | mA | FOSC = 4 MHz, VDD = 5.5V |
| | | PIC16C5X-XT | — | 1.8 | 3.3 | mA | FOSC = 4 MHz, VDD = 5.5V |
| | | PIC16C5X-10 | — | 4.8 | 10 | mA | FOSC = 10 MHz, VDD = 5.5V |
| | | PIC16C5X-HS | — | 4.8 | 10 | mA | FOSC = 10 MHz, VDD = 5.5V |
| | | PIC16C5X-HS | — | 9.0 | 20 | mA | FOSC = 20 MHz, VDD = 5.5V |
| | | PIC16C5X-LP | — | 15 | 32 | µA | FOSC = 32 kHz, VDD = 3.0V, WDT disabled |
| D020 | IPD | **Power-down Current(2)** | — | 4.0 | 12 | µA | VDD = 3.0V, WDT enabled |
| | | | — | 0.6 | 9 | µA | VDD = 3.0V, WDT disabled |

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

## 12.4 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial) PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D030 | VIL | **Input Low Voltage** | | | | | |
| | | I/O ports | VSS | — | 0.2 VDD | V | Pin at hi-impedance |
| | | MCLR (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | T0CKI (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | OSC1 (Schmitt Trigger) | VSS | — | 0.15 VDD | V | PIC16C5X-RC only(3) |
| | | OSC1 (Schmitt Trigger) | VSS | — | 0.3 VDD | V | PIC16C5X-XT, 10, HS, LP |
| D040 | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | 0.45 VDD | — | VDD | V | For all VDD(4) |
| | | I/O ports | 2.0 | — | VDD | V | 4.0V < VDD ≤ 5.5V(4) |
| | | I/O ports | 0.36 VDD | — | VDD | V | VDD > 5.5V |
| | | MCLR (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | T0CKI (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | OSC1 (Schmitt Trigger) | 0.85 VDD | — | VDD | V | PIC16C5X-RC only(3) |
| | | OSC1 (Schmitt Trigger) | 0.7 VDD | — | VDD | V | PIC16C5X-XT, 10, HS, LP |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current(1,2)** | | | | | **For VDD ≤ 5.5V:** |
| | | I/O ports | –1 | 0.5 | +1 | µA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| | | MCLR | –5 | — | — | µA | VPIN = VSS + 0.25V |
| | | MCLR | — | 0.5 | +5 | µA | VPIN = VDD |
| | | T0CKI | –3 | 0.5 | +3 | µA | VSS ≤ VPIN ≤ VDD |
| | | OSC1 | –3 | 0.5 | +3 | µA | VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, 10, HS, LP |
| D080 | VOL | **Output Low Voltage** | | | | | |
| | | I/O ports | — | — | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | — | — | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC |
| D090 | VOH | **Output High Voltage(2)** | | | | | |
| | | I/O ports | VDD – 0.7 | — | — | V | IOH = –5.4 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | VDD – 0.7 | — | — | V | IOH = –1.0 mA, VDD = 4.5V, PIC16C5X-RC |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

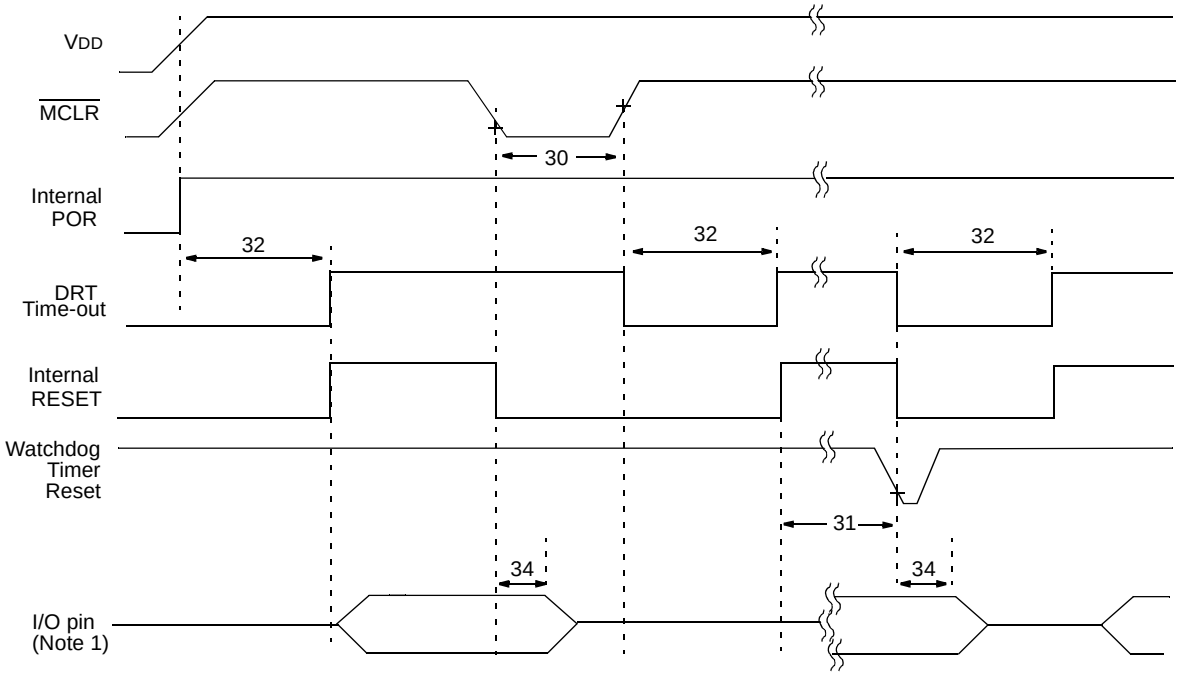
**Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

**4:** The user may use the better of the two specifications.

**FIGURE 12-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54/55/56/57**




**Note 1:** Please refer to Figure 12-1 for load conditions.

**TABLE 12-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57**

| **AC Characteristics** | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 100* | — | — | ns | VDD = 5.0V |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 32 | TDRT | Device Reset Timer Period | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 34 | Tioz | I/O Hi-impedance from $\overline{\text{MCLR}}$ Low | — | — | 100* | ns | |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**TABLE 14-2: INPUT CAPACITANCE FOR PIC16C54/56**

| Pin | Typical Capacitance (pF) | |
|---|---|---|
| | 18L PDIP | 18L SOIC |
| RA port | 5.0 | 4.3 |
| RB port | 5.0 | 4.3 |
| $\overline{MCLR}$ | 17.0 | 17.0 |
| OSC1 | 4.0 | 3.5 |
| OSC2/CLKOUT | 4.3 | 3.5 |
| T0CKI | 3.2 | 2.8 |

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

**TABLE 14-3: INPUT CAPACITANCE FOR PIC16C55/57**

| Pin | Typical Capacitance (pF) | |
|---|---|---|
| | 28L PDIP (600 mil) | 28L SOIC |
| RA port | 5.2 | 4.8 |
| RB port | 5.6 | 4.7 |
| RC port | 5.0 | 4.1 |
| $\overline{MCLR}$ | 17.0 | 17.0 |
| OSC1 | 6.6 | 3.5 |
| OSC2/CLKOUT | 4.6 | 3.5 |
| T0CKI | 4.5 | 3.5 |

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

## 15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PIC16LC54A-04**<br>**PIC16LC54A-04I**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **PIC16C54A-04, 10, 20**<br>**PIC16C54A-04I, 10I, 20I**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | VDD | **Supply Voltage** | | | | | |
| D001 | | PIC16LC54A | 3.0<br>2.5 | —<br>— | 6.25<br>6.25 | V<br>V | XT and RC modes<br>LP mode |
| D001A | | PIC16C54A | 3.0<br>4.5 | —<br>— | 6.25<br>5.5 | V<br>V | RC, XT and LP modes<br>HS mode |
| D002 | VDR | **RAM Data Retention Voltage(1)** | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D005 | IDD | **Supply Current(2)** | | | | | |
| | | PIC16LC5X | —<br>—<br>— | 0.5<br>11<br>11 | 2.5<br>27<br>35 | mA<br>µA<br>µA | FOSC = 4.0 MHz, VDD = 5.5V, RC(3) and XT modes<br>FOSC = 32 kHz, VDD = 2.5V, WDT disabled, LP mode, Commercial<br>FOSC = 32 kHz, VDD = 2.5V, WDT disabled, LP mode, Industrial |
| D005A | | PIC16C5X | —<br>—<br>—<br>—<br>— | 1.8<br>2.4<br>4.5<br>14<br>17 | 2.4<br>8.0<br>16<br>29<br>37 | mA<br>mA<br>mA<br>µA<br>µA | FOSC = 4.0 MHz, VDD = 5.5V, RC(3) and XT modes<br>FOSC = 10 MHz, VDD = 5.5V, HS mode<br>FOSC = 20 MHz, VDD = 5.5V, HS mode<br>FOSC = 32 kHz, VDD = 3.0V, WDT disabled, LP mode, Commercial<br>FOSC = 32 kHz, VDD = 3.0V, WDT disabled, LP mode, Industrial |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

## 15.3 DC Characteristics: PIC16LV54A-02 (Commercial) PIC16LV54A-02I (Industrial)

| PIC16LV54A-02<br>PIC16LV54A-02I<br>(Commercial, Industrial) | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–20°C ≤ TA ≤ +85°C for industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage**<br>RC and XT modes | 2.0 | — | 3.8 | V | |
| D002 | VDR | **RAM Data Retention Voltage(1)** | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D010 | IDD | **Supply Current(2)**<br>RC(3) and XT modes<br>LP mode, Commercial<br>LP mode, Industrial | <br>—<br>—<br>— | <br>0.5<br>11<br>14 | <br>—<br>27<br>35 | <br>mA<br>µA<br>µA | <br>FOSC = 2.0 MHz, VDD = 3.0V<br>FOSC = 32 kHz, VDD = 2.5V WDT disabled<br>FOSC = 32 kHz, VDD = 2.5V WDT disabled |
| D020 | IPD | **Power-down Current(2,4)**<br>Commercial<br>Commercial<br>Industrial<br>Industrial | <br>—<br>—<br>—<br>— | <br>2.5<br>0.25<br>3.5<br>0.3 | <br>12<br>4.0<br>14<br>5.0 | <br>µA<br>µA<br>µA<br>µA | <br>VDD = 2.5V, WDT enabled<br>VDD = 2.5V, WDT disabled<br>VDD = 2.5V, WDT enabled<br>VDD = 2.5V, WDT disabled |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

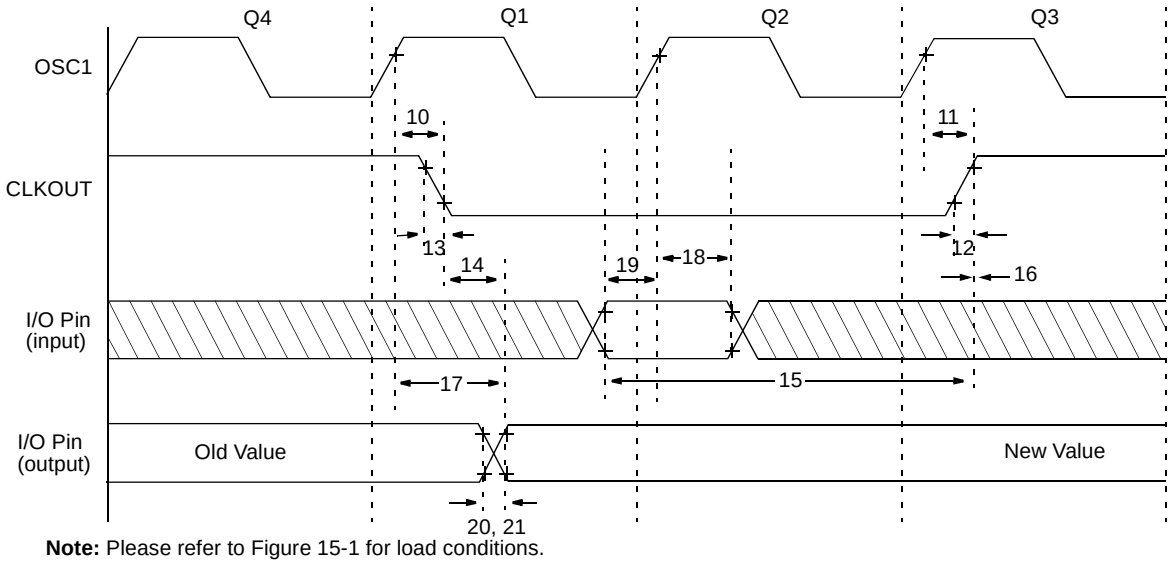
b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

**4:** The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection on wake-up from SLEEP mode or during initial power-up.

**FIGURE 15-3: CLKOUT AND I/O TIMING - PIC16C54A**




**Note:** Please refer to Figure 15-1 for load conditions.

**TABLE 15-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54A**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I<br>–40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** |
| 10 | TosH2ckL | OSC1↑ to CLKOUT↓(1) | — | 15 | 30** | ns |
| 11 | TosH2ckH | OSC1↑ to CLKOUT↑(1) | — | 15 | 30** | ns |
| 12 | TckR | CLKOUT rise time(1) | — | 5.0 | 15** | ns |
| 13 | TckF | CLKOUT fall time(1) | — | 5.0 | 15** | ns |
| 14 | TckL2ioV | CLKOUT↓ to Port out valid(1) | — | — | 40** | ns |
| 15 | TioV2ckH | Port in valid before CLKOUT↑(1) | 0.25 TCY+30* | — | — | ns |
| 16 | TckH2ioI | Port in hold after CLKOUT↑(1) | 0* | — | — | ns |
| 17 | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid(2) | — | — | 100* | ns |
| 18 | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | TBD | — | — | ns |
| 19 | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | TBD | — | — | ns |
| 20 | TioR | Port output rise time(2) | — | 10 | 25** | ns |
| 21 | TioF | Port output fall time(2) | — | 10 | 25** | ns |

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

**2:** Please refer to Figure 15-1 for load conditions.

**FIGURE 16-10: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, 25°C)**

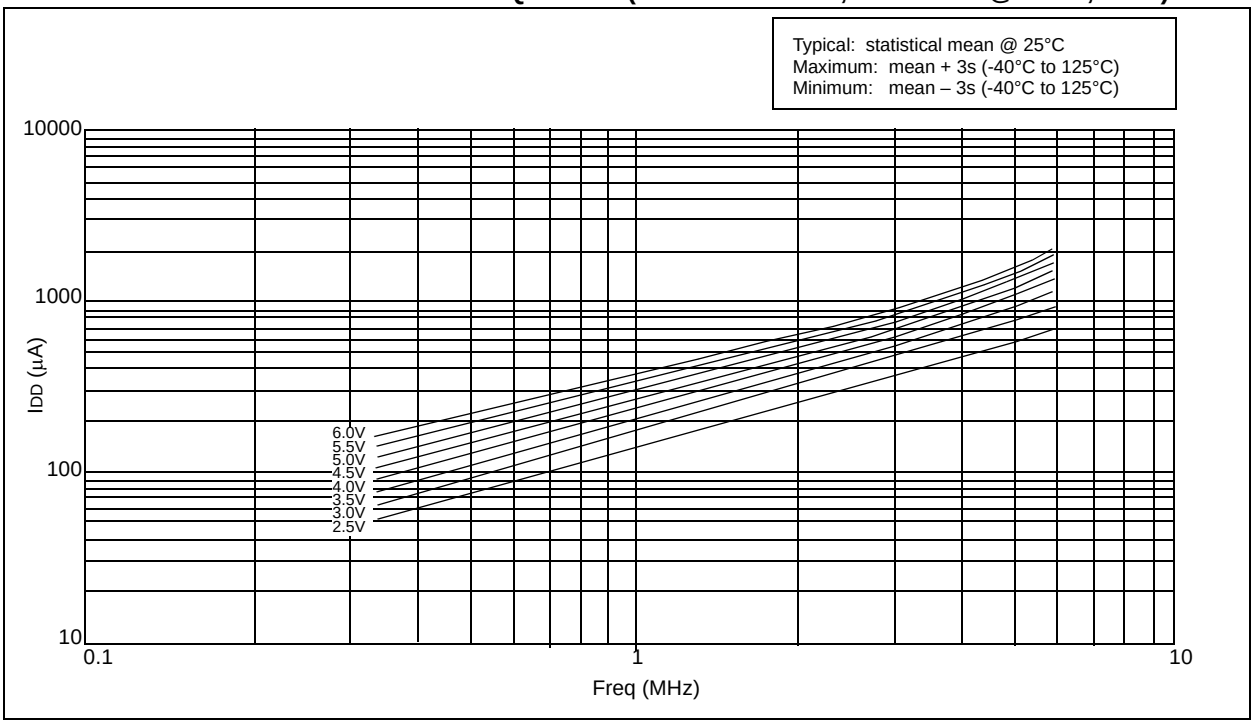



**FIGURE 16-11: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, –40°C to +85°C)**

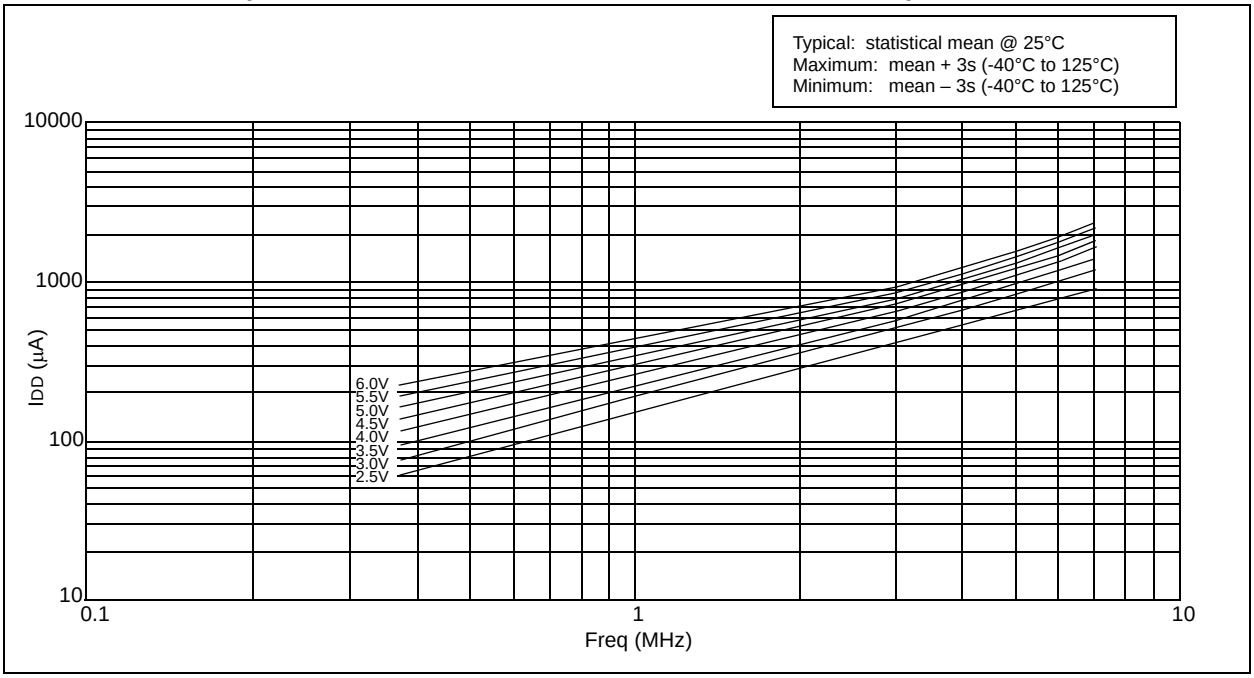


**FIGURE 16-14: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, 25°C)**

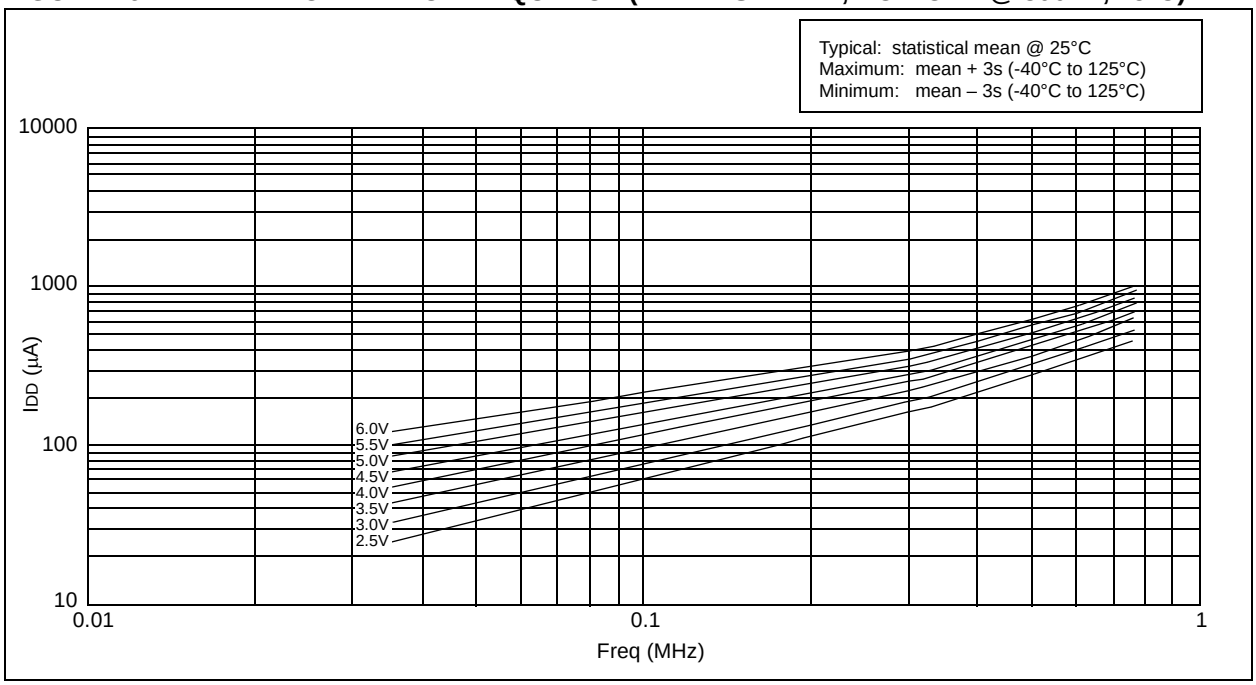



**FIGURE 16-15: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, –40°C to +85°C)**

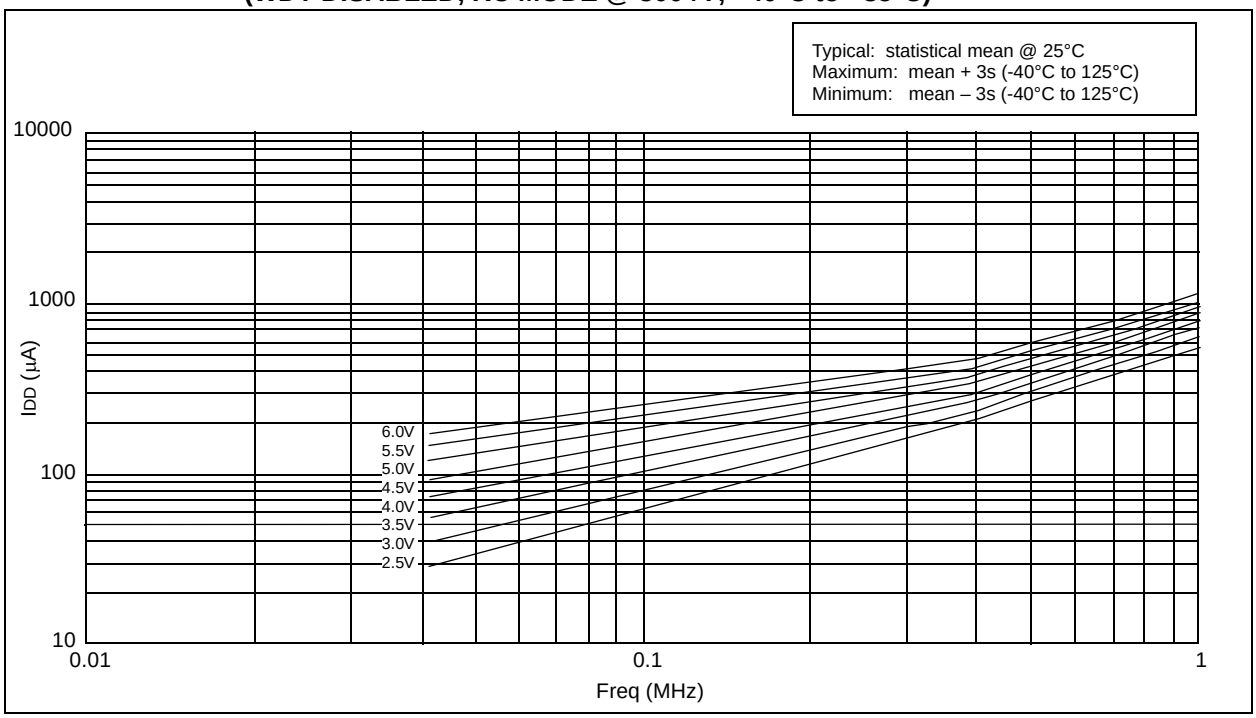


**FIGURE 16-18: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD**

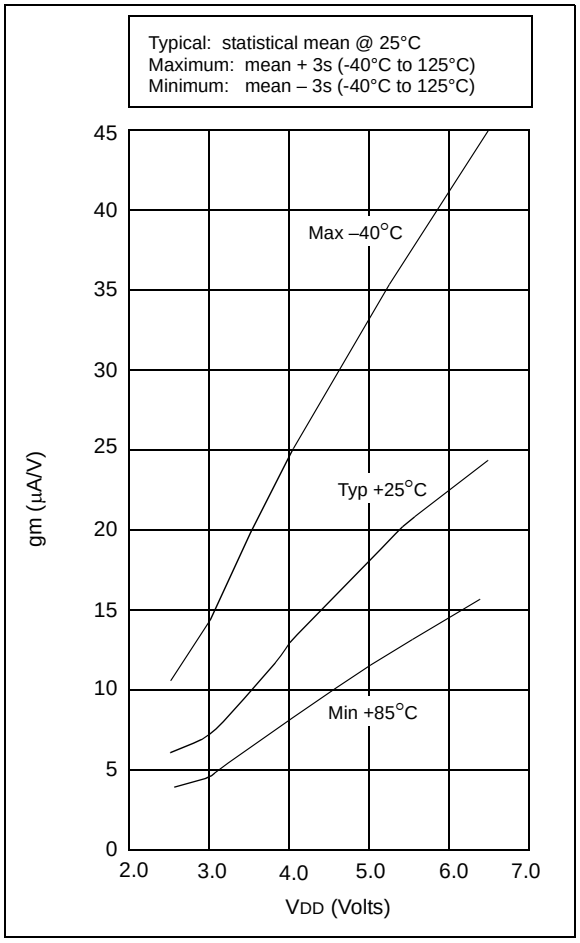
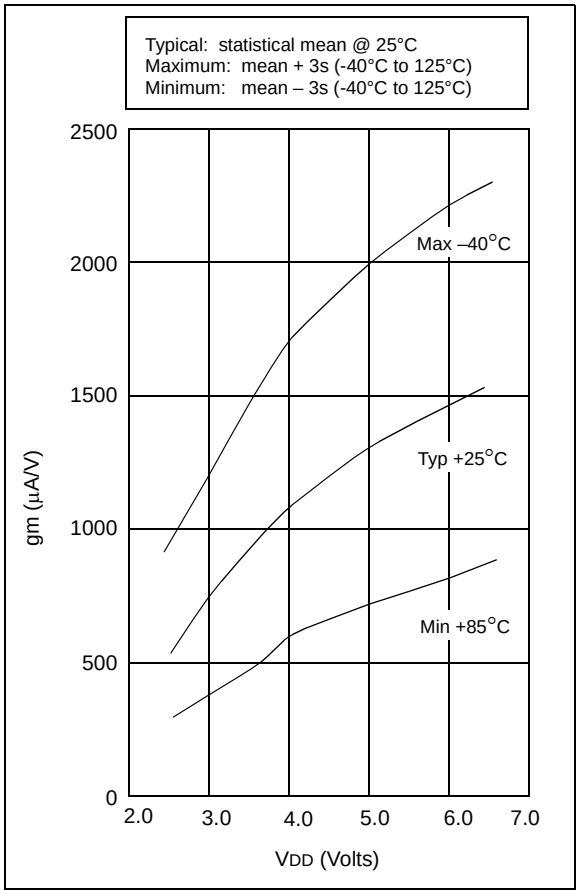


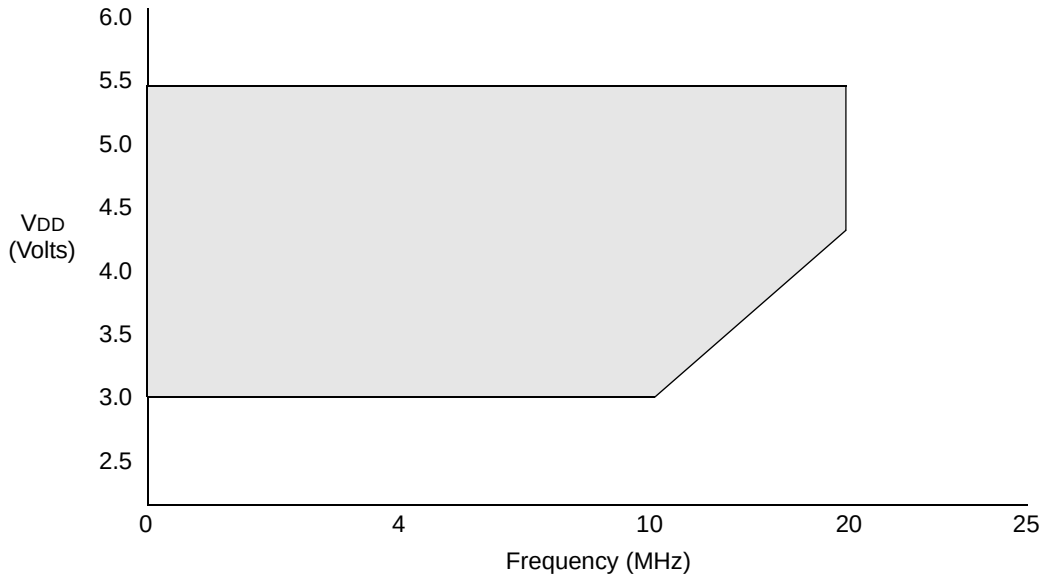

**FIGURE 16-19: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD**



**NOTES:**

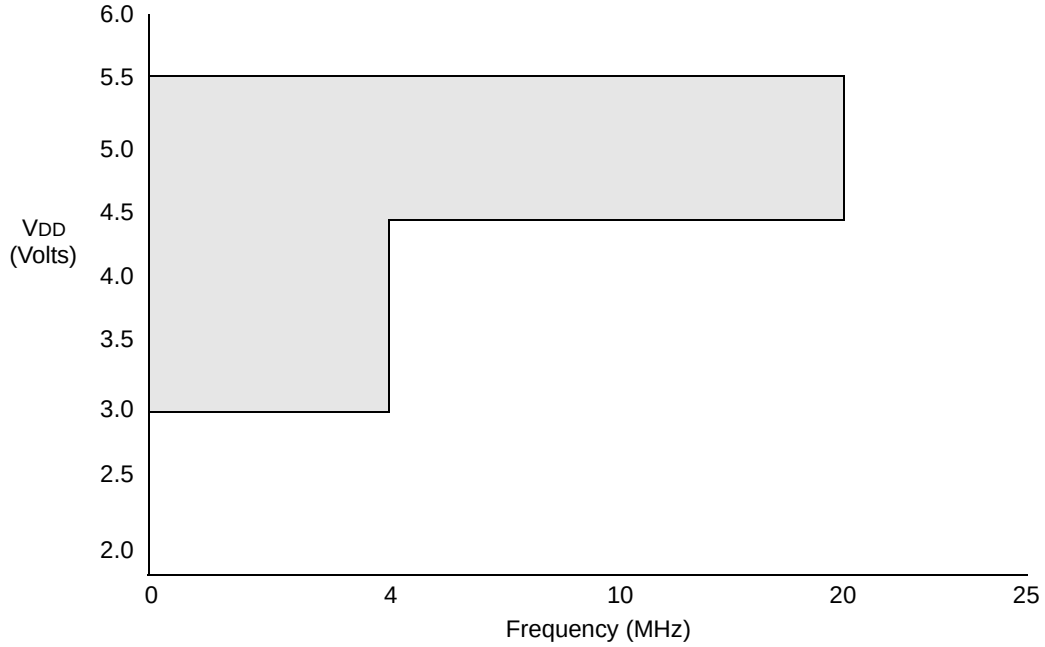
**FIGURE 17-1: PIC16C54C/55A/56A/57C/58B-04, 20 VOLTAGE-FREQUENCY GRAPH, 0°C ≤ $T_A$ ≤ +70°C (COMMERCIAL TEMPS)**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

**2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

**FIGURE 17-2: PIC16C54C/55A/56A/57C/58B-04, 20 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ $T_A$ < 0°C, +70°C < $T_A$ ≤ +125°C (OUTSIDE OF COMMERCIAL TEMPS)**

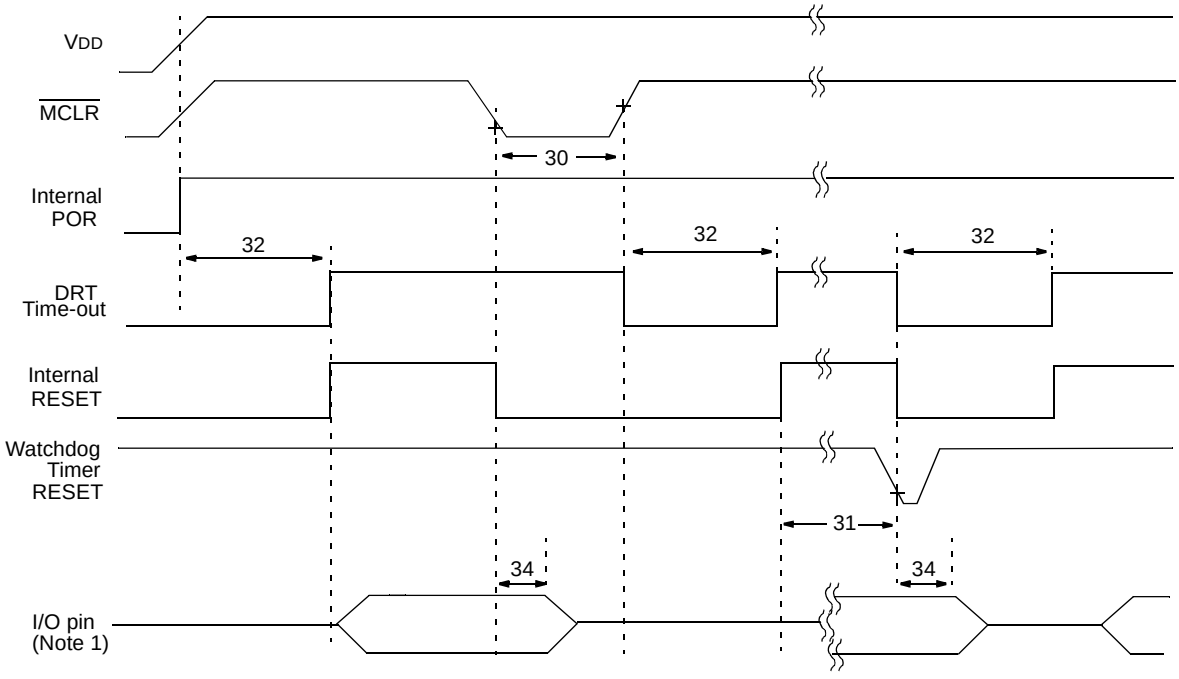



**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

**2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

**FIGURE 17-8: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X, PIC16CR5X**




**Note 1:** Please refer to Figure 17-5 for load conditions.

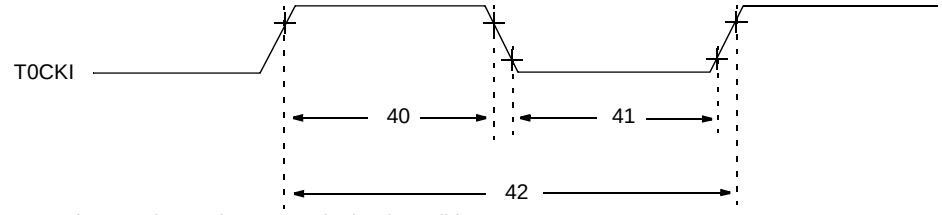
**TABLE 17-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X, PIC16CR5X**

| **AC Characteristics** | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 1000* | — | — | ns | VDD = 5.0V |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 32 | TDRT | Device Reset Timer Period | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 34 | Tioz | I/O Hi-impedance from $\overline{\text{MCLR}}$ Low | 100* | 300* | 1000* | ns | |

* These parameters are characterized but not tested.

† Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 17-9: TIMER0 CLOCK TIMINGS - PIC16C5X, PIC16CR5X**




**Note:** Please refer to Figure 17-5 for load conditions.

**TABLE 17-4: TIMER0 CLOCK REQUIREMENTS - PIC16C5X, PIC16CR5X**

| AC Characteristics | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 40 | Tt0H | T0CKI High Pulse Width<br>- No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width<br>- No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | 20 or $\frac{T_{CY} + 40}{N}$* | — | — | ns | Whichever is greater.<br>N = Prescale Value (1, 2, 4,..., 256) |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## 19.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)(1)

| PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial) | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | 4.5 | — | 5.5 | V | HS mode from 20 - 40 MHz |
| D002 | VDR | **RAM Data Retention Voltage(2)** | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D010 | IDD | **Supply Current(3)** | —<br>— | 5.2<br>6.8 | 12.3<br>16 | mA<br>mA | FOSC = 40 MHz, VDD = 4.5V, HS mode<br>FOSC = 40 MHz, VDD = 5.5V, HS mode |
| D020 | IPD | **Power-down Current(3)** | —<br>— | 1.8<br>9.8 | 7.0<br>27* | µA<br>µA | VDD = 5.5V, WDT disabled, Commercial<br>VDD = 5.5V, WDT enabled, Commercial |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected, HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 19.1.

**2:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**FIGURE 20-2: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (25°C)**

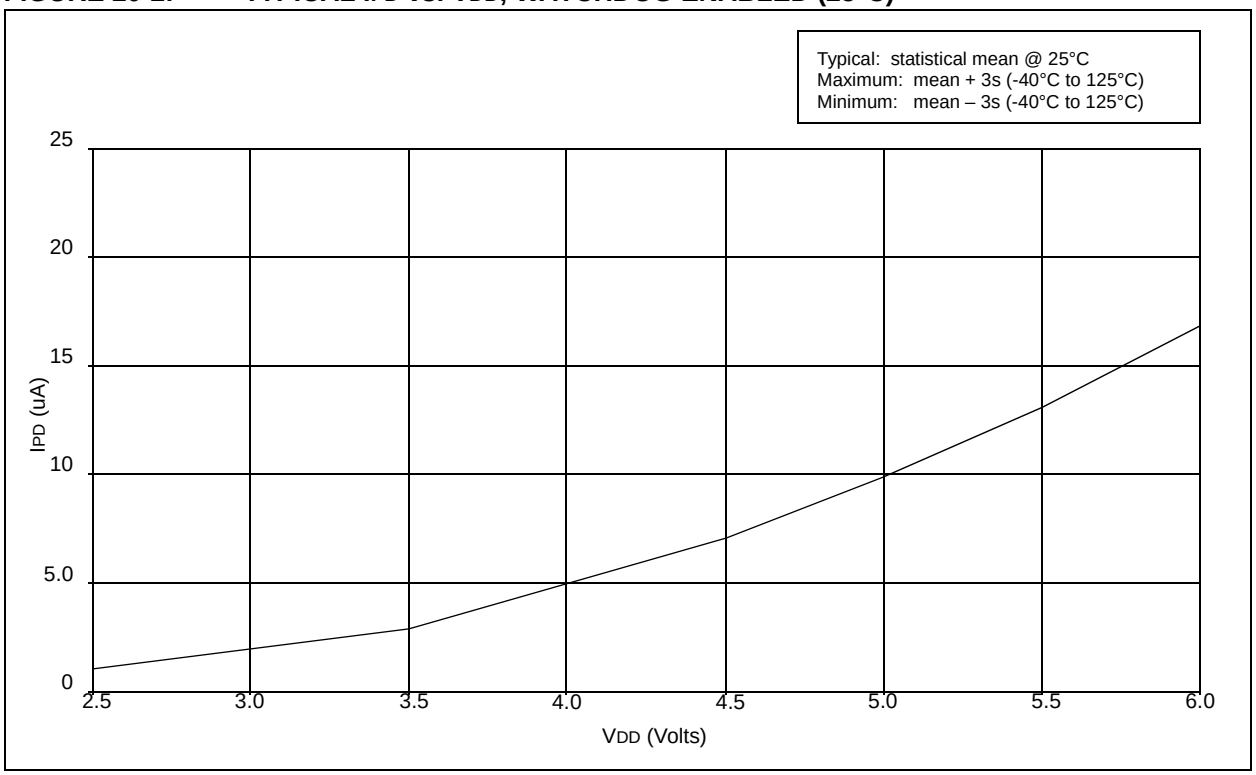
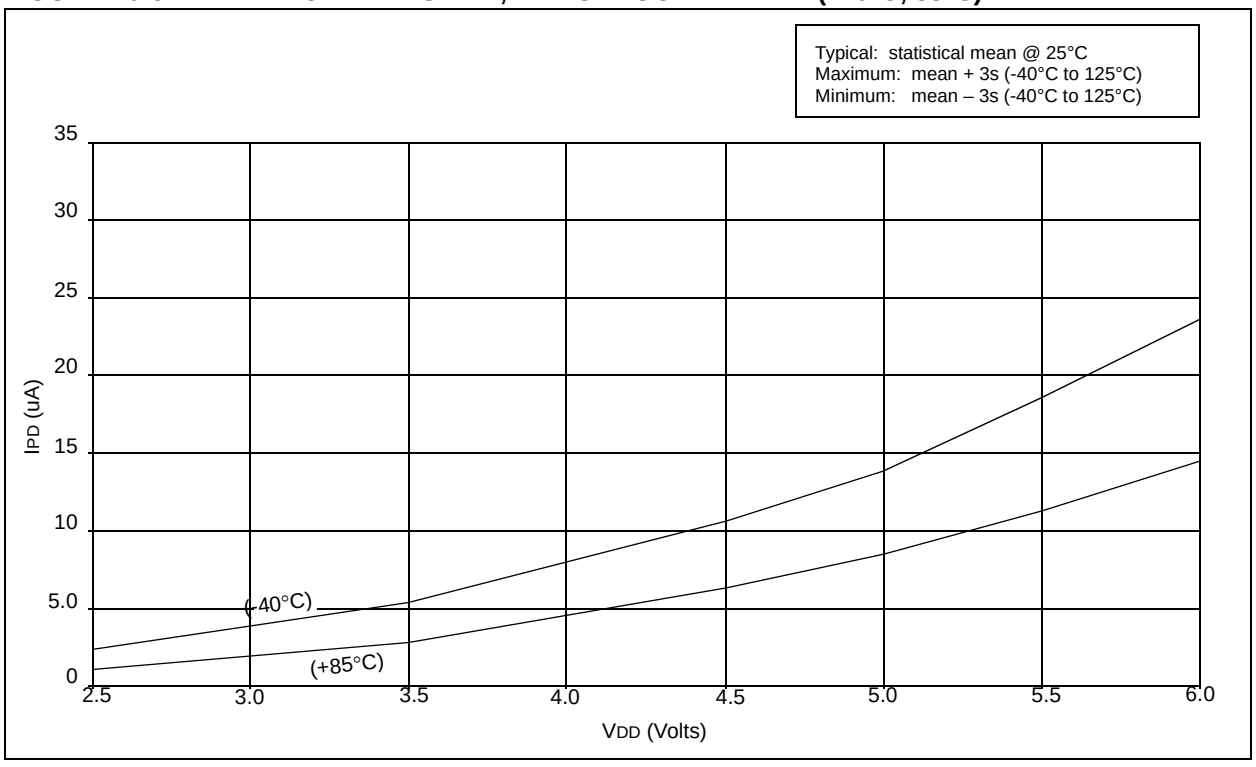



**FIGURE 20-3: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (–40°C, 85°C)**

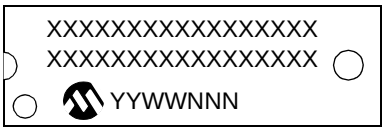


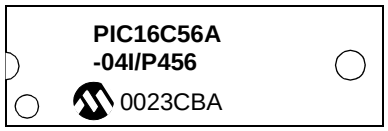
## 21.0 PACKAGING INFORMATION

### 21.1 Package Marketing Information

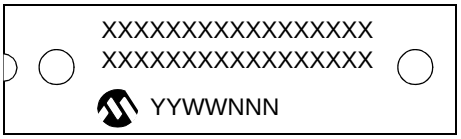
18-Lead PDIP



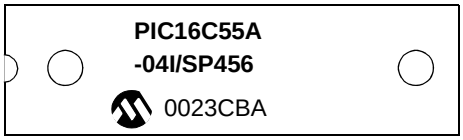

Example



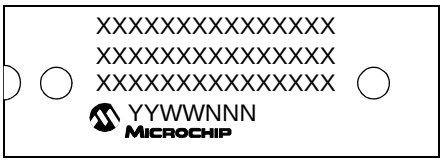

28-Lead Skinny PDIP (.300")



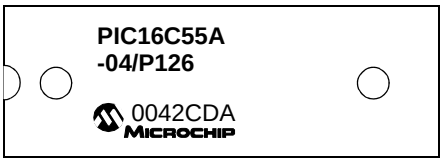

Example




28-Lead PDIP (.600")



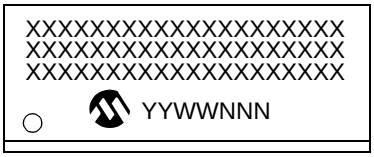

Example




18-Lead SOIC

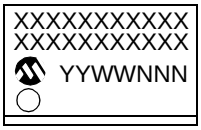

Example


28-Lead SOIC




Example


20-Lead SSOP



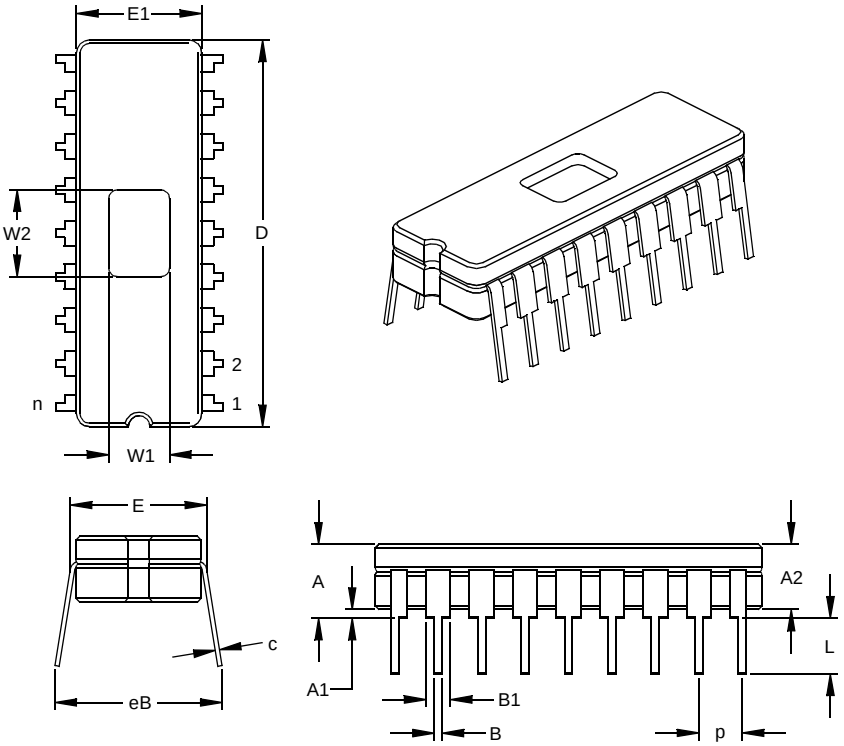

Example


28-Lead SSOP


Example

### 18-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 18 | | | 18 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .170 | .183 | .195 | 4.32 | 4.64 | 4.95 |
| Ceramic Package Height | A2 | .155 | .160 | .165 | 3.94 | 4.06 | 4.19 |
| Standoff | A1 | .015 | .023 | .030 | 0.38 | 0.57 | 0.76 |
| Shoulder to Shoulder Width | E | .300 | .313 | .325 | 7.62 | 7.94 | 8.26 |
| Ceramic Pkg. Width | E1 | .285 | .290 | .295 | 7.24 | 7.37 | 7.49 |
| Overall Length | D | .880 | .900 | .920 | 22.35 | 22.86 | 23.37 |
| Tip to Seating Plane | L | .125 | .138 | .150 | 3.18 | 3.49 | 3.81 |
| Lead Thickness | c | .008 | .010 | .012 | 0.20 | 0.25 | 0.30 |
| Upper Lead Width | B1 | .050 | .055 | .060 | 1.27 | 1.40 | 1.52 |
| Lower Lead Width | B | .016 | .019 | .021 | 0.41 | 0.47 | 0.53 |
| Overall Row Spacing § | eB | .345 | .385 | .425 | 8.76 | 9.78 | 10.80 |
| Window Width | W1 | .130 | .140 | .150 | 3.30 | 3.56 | 3.81 |
| Window Length | W2 | .190 | .200 | .210 | 4.83 | 5.08 | 5.33 |

* Controlling Parameter
§ Significant Characteristic
JEDEC Equivalent: MO-036
Drawing No. C04-010