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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	24 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c55-xt-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A twostage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle except for program branches.

The PIC16C54/CR54 and PIC16C55 address 512 x 12 of program memory, the PIC16C56/CR56 address 1K x 12 of program memory, and the PIC16C57/CR57 and PIC16C58/CR58 address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly. The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 (for PIC16C54/56/58) and Table 3-2 (for PIC16C55/57).

4.4 RC Oscillator

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 4-5 shows how the R/C combination is connected to the PIC16C5X. For REXT values below 2.2 k Ω , the oscillator operation may become unstable, or stop completely. For very high REXT values (e.g., 1 M Ω) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping REXT between 3 k Ω and 100 k Ω .

Although the oscillator will operate with no external capacitor (CEXT = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications sections for variation of oscillator frequency due to VDD for given REXT/ CEXT values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic.



Note: If you change from this device to another device, please verify oscillator characteristics in your application.

6.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not

writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as $000u \ u1uu$ (where u = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 10.0, Instruction Set Summary.

REGISTER 6-1: STATUS REGISTER (ADDRESS: 03h)

	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x	
	PA2	PA1	PA0	TO	PD	Z	DC	С	
	bit 7							bit 0	
bit 7:	PA2: This bit	unused at th	is time.						
		A2 bit as a ge with future pr		e read/write	bit is not recor	mmended, sir	nce this may a	affect upward	
bit 6-5:				-	CR56)(PIC16			58)	
					16C57/CR57, 16C57/CR57,				
		(400h - 5FFh				FIC 10C30/C	N00		
	11 = Page 3	(600h - 7FFh							
	Each page is		deperal pur	ose read/wr	ite bits in devi	ices which do	not use them	for program	
					affect upward				
bit 4:	TO: Time-ou			,	•				
		ver-up, CLRWI ime-out occur		, or sleep i	nstruction				
bit 3:	PD: Power-d	lown bit							
	•	ver-up or by tl ution of the SI							
bit 2:	Z: Zero bit								
		lt of an arithm It of an arithm							
bit 1:	DC: Digit car	ry/borrow bit	(for ADDWF a	nd SUBWF in	structions)				
	ADDWF								
		rom the 4th la rom the 4th la							
	SUBWF								
					did not occur				
	 0 = A borrow from the 4th low order bit of the result occurred Carry/borrow bit (for ADDWF, SUBWF and RRF, RLF instructions) 								
bit 0:	•	row bit (for AI			F instructions		_		
	ADDWF 1 = A carry o	ocurred		orrow did n	ot occur	RRF or RLI		, respectively	
	$\pm = \pi \operatorname{carry} 0$	locurrou	/ · ·						

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

9.1 Configuration Bits

Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. Nine bits are code protection bits for the PIC16C54A, PIC16CR54A, PIC16C55A, PIC16C56A, PIC16CR56A, PIC16CR57C, PIC16CR57C, PIC16CR57C,

PIC16C58B, and PIC16CR58B devices (Register 9-1). One bit is for code protection for the PIC16C54, PIC16C55, PIC16C56 and PIC16C57 devices (Register 9-2).

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" diagrams in the back of this data sheet).

REGISTER 9-1: CONFIGURATION WORD FOR PIC16C54A/CR54A/C54C/CR54C/C55A/C56A/ CR56A/C57C/CR57C/C58B/CR58B

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0
bit 11											bit 0

bit 11-3: CP: Code Protection Bit

- 1 = Code protection off
 - 0 =Code protection on
- bit 2: WDTE: Watchdog timer enable bit
 - 1 = WDT enabled
 - 0 = WDT disabled

bit 1-0: FOSC1:FOSC0: Oscillator Selection Bit

- 00 = LP oscillator
- 01 = XT oscillator
- 10 = HS oscillator
- 11 = RC oscillator

Note 1: Refer to the PIC16C5X Programming Specification (Literature Number DS30190) to determine how to access the configuration word.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

		Standard Operating Condition	•			-				
AC Chara	cteristics	Operating Temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial $-40^{\circ}C \leq TA \leq +85^{\circ}C$ for industrial								
				TA ≤ +125						
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions			
1	Tosc	External CLKIN Period ⁽¹⁾	250	—	_	ns	XT OSC mode			
			100	—	—	ns	10 MHz mode			
			50	—	—	ns	HS osc mode (Comm/Ind)			
			62.5	—	—	ns	HS osc mode (Ext)			
			25	—	_	μS	LP OSC mode			
		Oscillator Period ⁽¹⁾	250	—	—	ns	RC OSC mode			
			250	—	10,000	ns	XT OSC mode			
			100	—	250	ns	10 MHz mode			
			50	—	250	ns	HS OSC mode (Comm/Ind)			
			62.5	—	250	ns	HS osc mode (Ext)			
			25	—	_	μS	LP OSC mode			
2	Тсу	Instruction Cycle Time ⁽²⁾	—	4/Fosc		—				
3	TosL,	Clock in (OSC1) Low or High	85*	—	—	ns	XT oscillator			
	TosH	Time	20*	—	—	ns	HS oscillator			
			2.0*	—		μS	LP oscillator			
4	TosR,	Clock in (OSC1) Rise or Fall	—	—	25*	ns	XT oscillator			
	TosF	Time	—	—	25*	ns	HS oscillator			
			—	—	50*	ns	LP oscillator			

TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 PIC16LCR54A-04I (Commercial, Industrial)				$ \begin{array}{ l l l l l l l l l l l l l l l l l l l$						
PIC16CR	254A-04, 10 254A-04I, 10 ercial, Indus) i , 20i		ard Oper ting Temp		0°	s (unless otherwise specified) C \leq TA \leq +70°C for commercial C \leq TA \leq +85°C for industrial			
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions			
	IPD	Power-down Current ⁽²⁾								
D006		PIC16LCR54A-Commercial		1.0 2.0 3.0 5.0	6.0 8.0* 15 25	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled			
D006A		PIC16CR54A-Commercial		1.0 2.0 3.0 5.0	6.0 8.0* 15 25	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled			
D007		PIC16LCR54A-Industrial		1.0 2.0 3.0 3.0 5.0	8.0 10* 20* 18 45	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 4.0V, WDT enabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled			
D007A		PIC16CR54A-Industrial		1.0 2.0 3.0 3.0 5.0	8.0 10* 20* 18 45	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 4.0V, WDT enabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled			

Legend: Rows with standard voltage device data only are shaded for improved readability.

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.
- **Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .



FIGURE 13-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR54A

TABLE 13-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR54A

$\label{eq:AC Characteristics} \begin{tabular}{lllllllllllllllllllllllllllllllllll$							
Param No.	Symbol	Characteristic Min Typ† Max Units Conditions					Conditions
30	TmcL	MCLR Pulse Width (low)	1.0*			μS	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7.0*	18*	40*	ms	VDD = 5.0V (Comm)
32	Tdrt	Device Reset Timer Period	7.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	_	_	1.0*	μS	

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C5X









15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04 PIC16LC54A-04I (Commercial, Industrial)				$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$				
PIC16C5	54A-04, 10 5 4A-04I, 1 0 ercial, Ind	01, 201	$\begin{array}{l} Standard Operating Conditions (unless otherwise species of the speci$					
Param No.	Symbol	Characteristic/Device	Characteristic/Device Min Typ† Max Units Conditions				Conditions	
	IPD	Power-down Current ⁽²⁾						
D006		PIC16LC5X		2.5 0.25 2.5 0.25	12 4.0 14 5.0	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT enabled, Commercial VDD = 2.5V, WDT disabled, Commercial VDD = 2.5V, WDT enabled, Industrial VDD = 2.5V, WDT disabled, Industrial	
D006A		PIC16C5X		4.0 0.25 5.0 0.3	12 4.0 14 5.0	μΑ μΑ μΑ μΑ	VDD = 3.0V, WDT enabled, Commercial VDD = 3.0V, WDT disabled, Commercial VDD = 3.0V, WDT enabled, Industrial VDD = 3.0V, WDT disabled, Industrial	

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

NOTES:

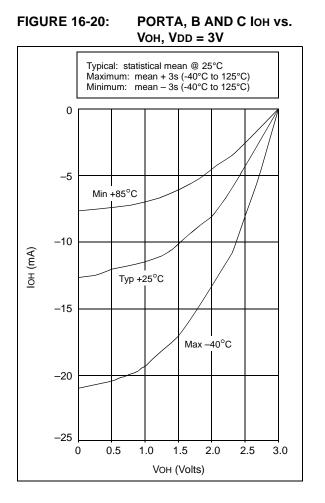
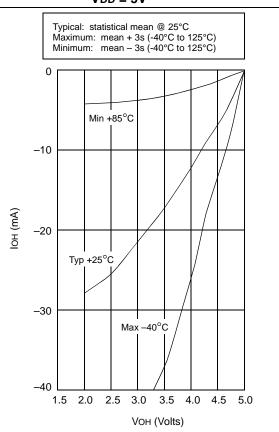
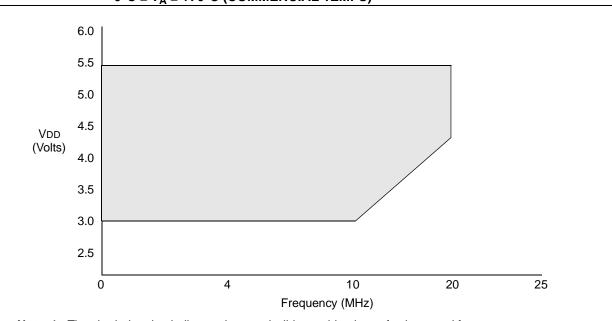


FIGURE 16-21: PORTA, B AND C IOH vs. VOH, VDD = 5V



PIC16C5X

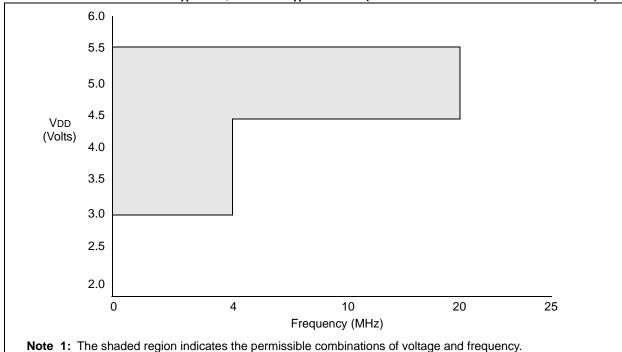






2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.





2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency.

Please reference the Product Identification System section for the maximum rated speed of the parts.

17.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC						ions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial	
PIC16C5 PIC16CF (Comm		ustrial)					ions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial
Param No.	Symbol	Characteristic/Device	Min Typ† Max Units Conditions			Conditions	
	IDD	Supply Current ^(2,3)					
D010		PIC16LC5X		0.5	2.4	mA	Fosc = 4.0 MHz, VDD = 5.5V, XT and
			—	11	27	μA	RC modes
							FOSC = 32 kHz, VDD = 2.5 V, LP mode,
			_	14	35	μA	Commercial Fosc = 32 kHz, VDD = 2.5V, LP mode,
							Industrial
D010A		PIC16C5X	_	1.8	2.4	mA	Fosc = 4 MHz, VDD = 5.5V, XT and RC
				2.6 4.5	3.6* 16	mA mA	modes Fosc = 10 MHz, VDD = 3.0V, HS mode
				4.5	32	μA	FOSC = 20 MHz, VDD = 3.00, HS mode FOSC = 20 MHz, VDD = 5.5V, HS mode
				14	52	μΛ	FOSC = 32 kHz, VDD = 3.3 V, HS mode
			_	17	40	μA	Commercial
							Fosc = 32 kHz, VDD = 3.0V, LP mode, Industrial

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

17.4 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

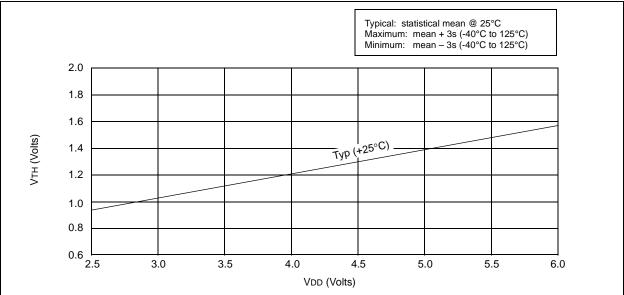
1. TppS2ppS

2. Tp	pS	
Т		
F	Frequency	T Time
Lowe	ercase letters (pp) and their meanings:	
рр		
2	to	mc MCLR
ck	CLKOUT	osc oscillator
су	cycle time	os OSC1
drt	device reset timer	t0 T0CKI
io	I/O port	wdt watchdog timer
Uppe	ercase letters and their meanings:	
S		
F	Fall	P Period
н	High	R Rise
T	Invalid (Hi-impedance)	V Valid
L	Low	Z Hi-impedance

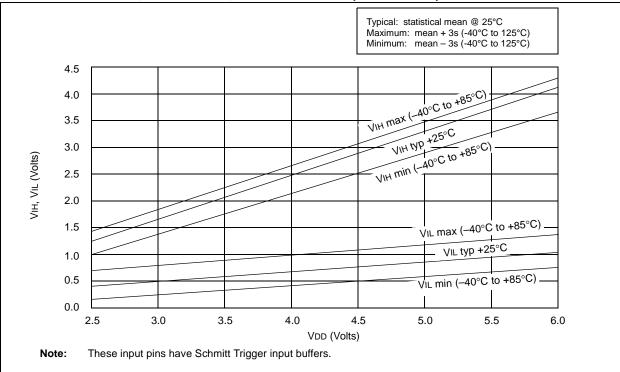
FIGURE 17-5: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS -PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B-04, 20











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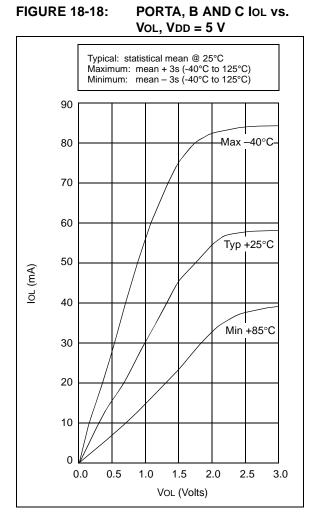


TABLE 18-2:INPUT CAPACITANCE

Pin	Typical Capacitance (pF)				
Pin	18L PDIP	18L SOIC			
RA port	5.0	4.3			
RB port	5.0	4.3			
MCLR	17.0	17.0			
OSC1	4.0	3.5			
OSC2/CLKOUT	4.3	3.5			
тоскі	3.2	2.8			

All capacitance values are typical at 25° C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.



TABLE 20-1: INPUT CAPACITANCE

Pin	Typical Capacitance (pF)			
	18L PDIP	18L SOIC		
RA port	5.0	4.3		
RB port	5.0	4.3		
MCLR	17.0	17.0		
OSC1	4.0	3.5		
OSC2/CLKOUT	4.3	3.5		
тоскі	3.2	2.8		

All capacitance values are typical at 25° C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.



28-Lead Skinny Plastic Dual In-line (SP) - 300 mil (PDIP)





в

	Units		INCHES*		Μ	IILLIMETERS	
Dimensi	on Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.100			2.54	
Top to Seating Plane	А	.140	.150	.160	3.56	3.81	4.06
Molded Package Thickness	A2	.125	.130	.135	3.18	3.30	3.43
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.310	.325	7.62	7.87	8.26
Molded Package Width	E1	.275	.285	.295	6.99	7.24	7.49
Overall Length	D	1.345	1.365	1.385	34.16	34.67	35.18
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.040	.053	.065	1.02	1.33	1.65
Lower Lead Width	В	.016	.019	.022	0.41	0.48	0.56
Overall Row Spacing	èB	.320	.350	.430	8.13	8.89	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter § Significant Characteristic

eВ

Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side.

JEDEC Equivalent: MO-095

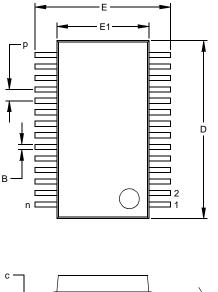
Drawing No. C04-070

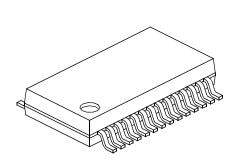
- p -

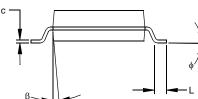
Notes:

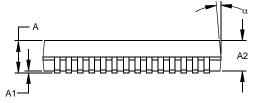
28-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









	Units	INCHES		MILLIMETERS*			
Dimensio	n Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.026			0.65	
Overall Height	А	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	Е	.299	.309	.319	7.59	7.85	8.10
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.396	.402	.407	10.06	10.20	10.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25
Foot Angle	¢	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-150 Drawing No. C04-073

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