What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	24 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c55-xti-so

NOTES:

Preliminary

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2 and Example 3-1.
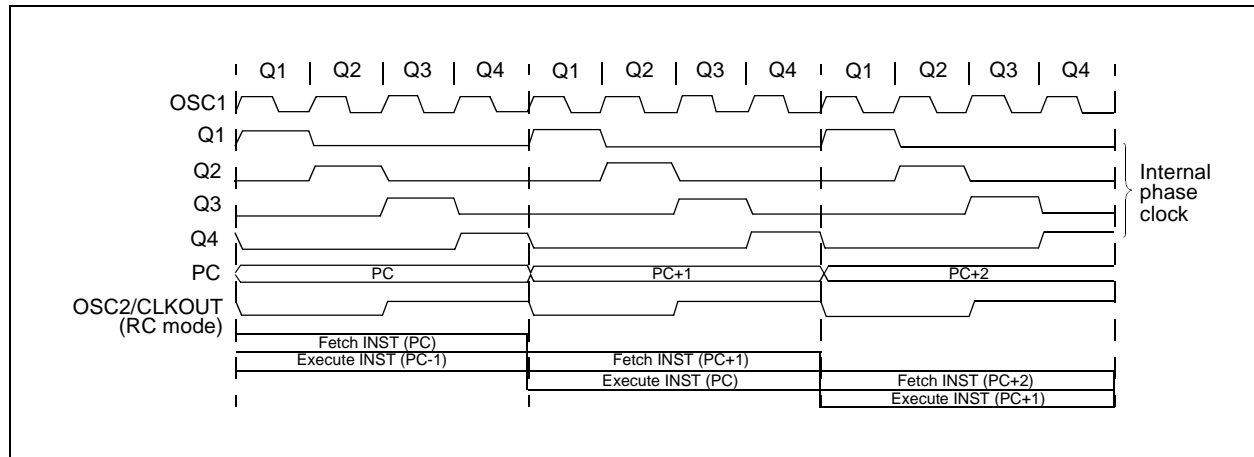
3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).
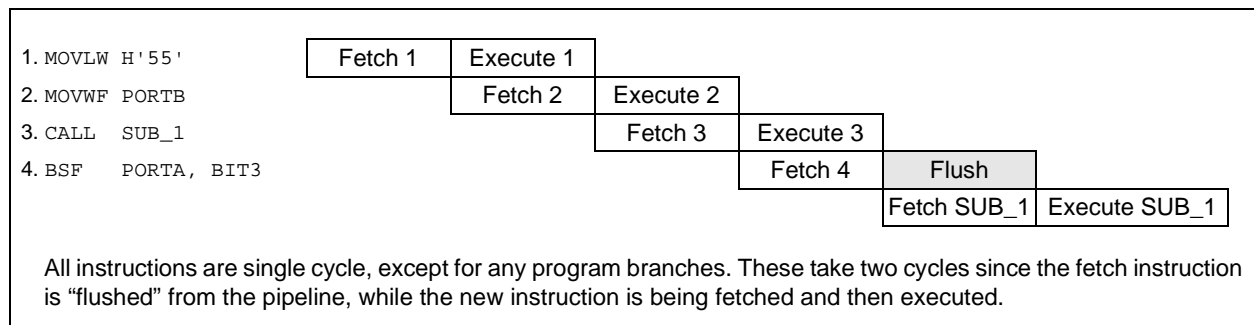
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2:   CLOCK/INSTRUCTION CYCLE

EXAMPLE 3-1:   INSTRUCTION PIPELINE FLOW

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline, while the new instruction is being fetched and then executed.

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4.3 External Crystal Oscillator Circuit

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 4-3 shows an implementation example of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 4-3: EXAMPLE OF EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)
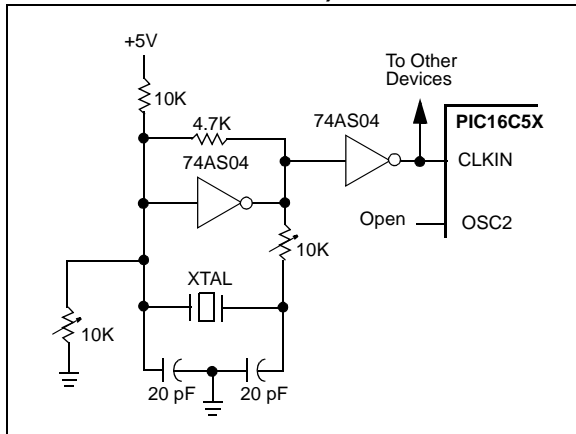

Figure 4-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 4-4: EXAMPLE OF EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)

Preliminary
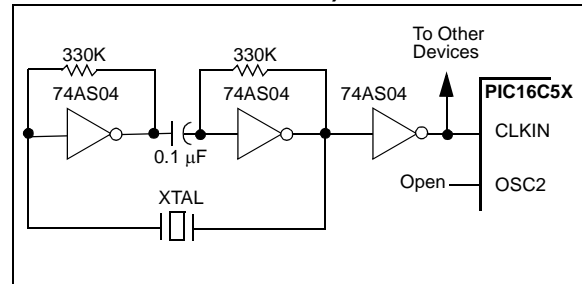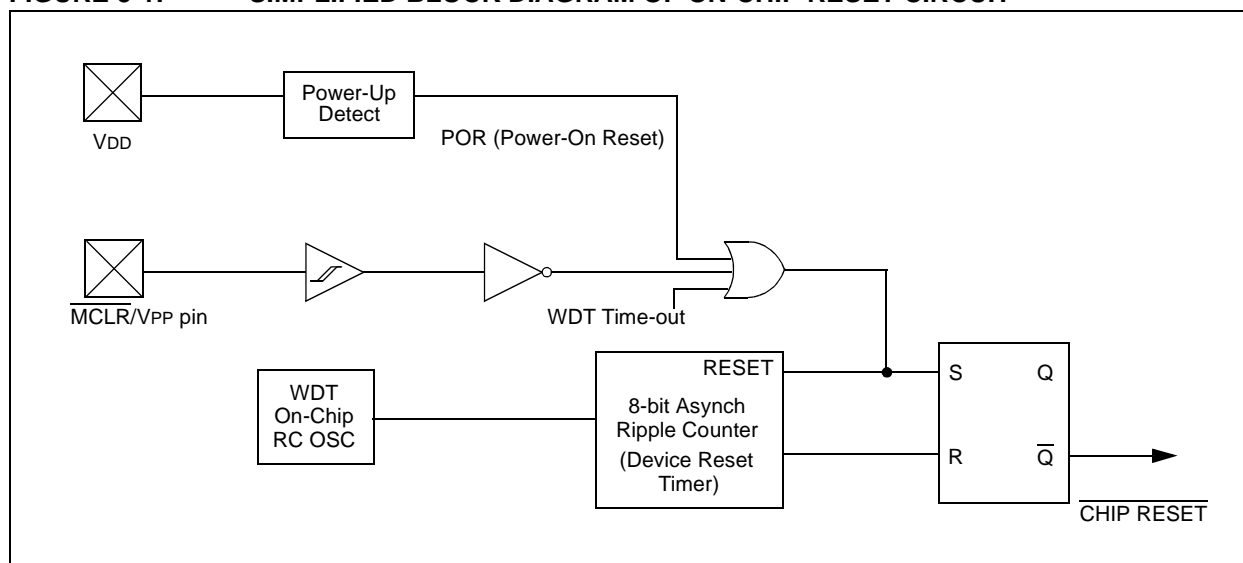
PIC16C5X

TABLE 5-3: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-On Reset	$\overline{\text{MCLR}}$ or WDT Reset
W	N/A	xxxx xxxx	uuuu uuuu
TRIS	N/A	1111 1111	1111 1111
OPTION	N/A	--11 1111	--11 1111
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000q quuu
FSR[1]	04h	1xxx xxxx	1uuu uuuu
PORTA	05h	---- xxxx	---- uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu
PORTC[2]	07h	xxxx xxxx	uuuu uuuu
General Purpose Register Files	07-7Fh	xxxx xxxx	uuuu uuuu

Legend: x = unknown u = unchanged - = unimplemented, read as '0'
q = see tables in Table 5-1 for possible values.

Note 1: These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for $\overline{\text{MCLR}}$ and WDT Reset, the value is 111u uuuu.

   2: General purpose register file on PIC16C54/CR54/C56/CR56/C58/CR58.

FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

6.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by
the CPU and peripheral functions to control the opera-
tion of the device (Table 6-1).

The Special Registers can be classified into two sets.
The Special Function Registers associated with the
"core" functions are described in this section. Those
related to the operation of the peripheral features are
described in the section for each peripheral feature.

TABLE 6-1:   SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Details on Page
N/A	TRIS	I/O Control Registers (TRISA, TRISB, TRISC)								1111 1111	35
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								--11 1111	30
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32
01h	TMR0	Timer0 Module Register								xxxx xxxx	38
02h[1]	PCL	Low order 8 bits of PC								1111 1111	31
03h	STATUS	PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	29
04h	FSR	Indirect data memory address pointer								1xxx xxxx[3]	32
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	35
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	35
07h[2]	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	35

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused
Note 1: The upper byte of the Program Counter is not directly accessible. See Section 6.5 for an explanation of how to access these bits.
  2: File address 07h is a General Purpose Register on the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58 and PIC16CR58.
  3: These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for $\overline{MCLR}$ and WDT Reset, the value is 111u uuuu.

6.5   Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.

For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0> (Figure 6-7, Figure 6-8 and Figure 6-9).

For the PIC16C56, PIC16CR56, PIC16C57, PIC16CR57, PIC16C58 and PIC16CR58, a page number must be supplied as well. Bit5 and bit6 of the STATUS Register provide page information to bit9 and bit10 of the PC (Figure 6-8 and Figure 6-9).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 6-7 and Figure 6-8).

Instructions where the PCL is the destination, or modify PCL instructions, include MOVWF PCL, ADDWF PCL, and BSF PCL,5.

For the PIC16C56, PIC16CR56, PIC16C57, PIC16CR57, PIC16C58 and PIC16CR58, a page number again must be supplied. Bit5 and bit6 of the STATUS Register provide page information to bit9 and bit10 of the PC (Figure 6-8 and Figure 6-9).

> **Note:** Because PC<8> is cleared in the CALL instruction, or any modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 6-7:   LOADING OF PC BRANCH INSTRUCTIONS - PIC16C54, PIC16CR54, PIC16C55
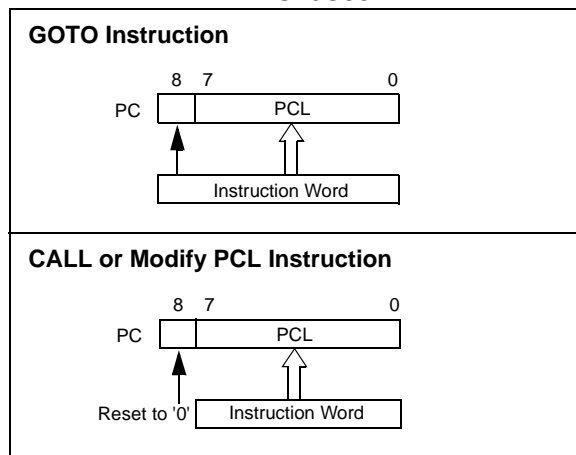

FIGURE 6-8:   LOADING OF PC BRANCH INSTRUCTIONS - PIC16C56/PIC16CR56
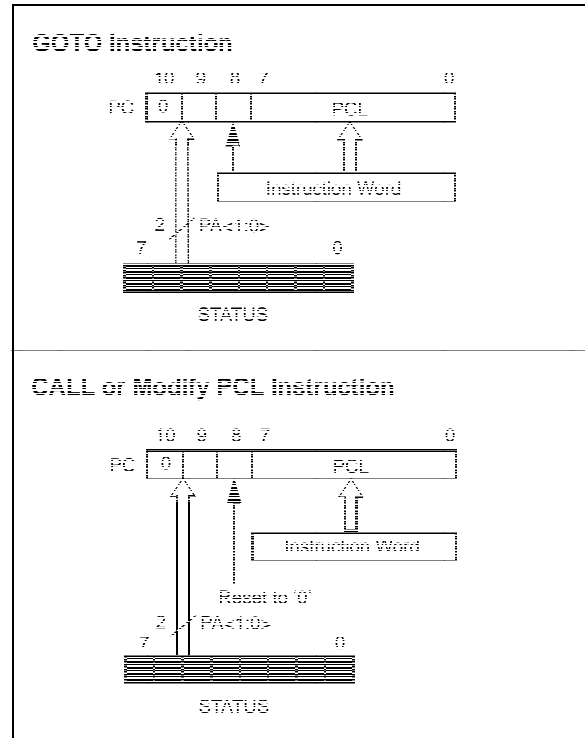

FIGURE 6-9:   LOADING OF PC BRANCH INSTRUCTIONS - PIC16C57/PIC16CR57, AND PIC16C58/PIC16CR58
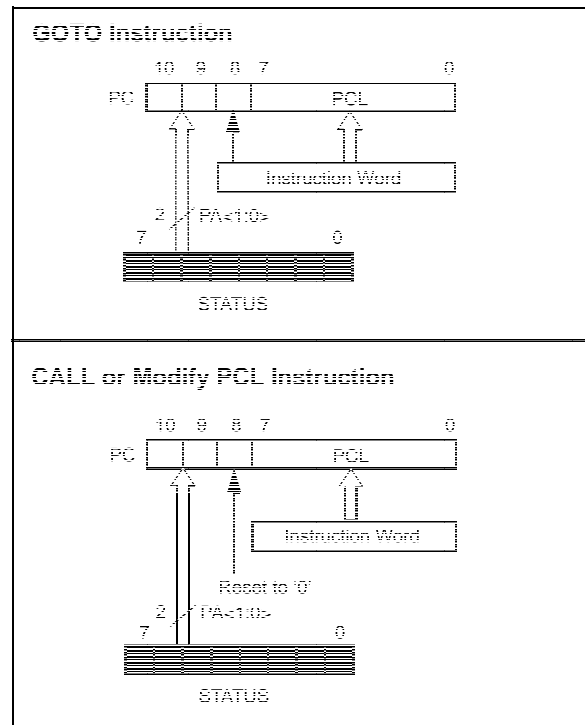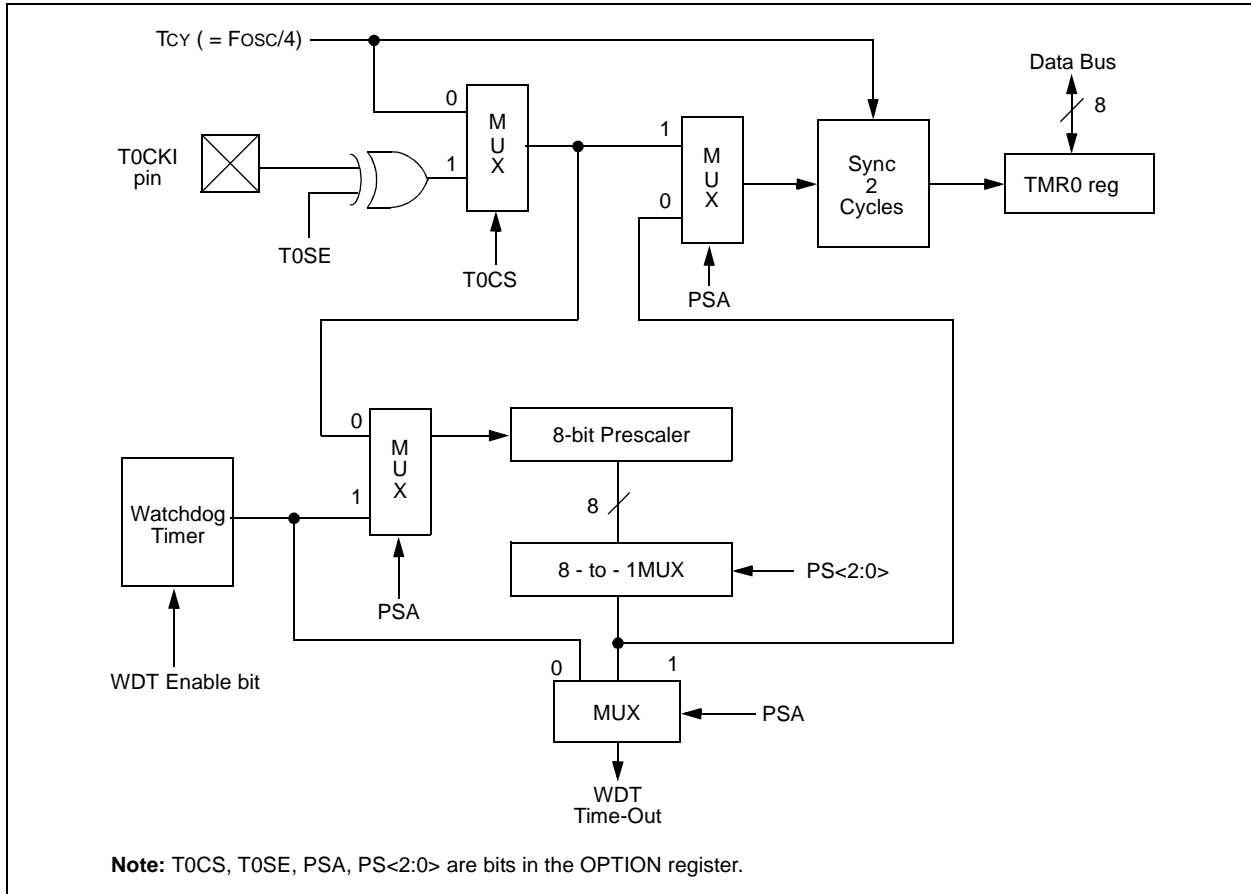
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FIGURE 8-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

Note: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

ADDWF	**Add W and f**
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	(W) + (f) $\rightarrow$ (dest)
Status Affected:	C, DC, Z
Encoding:	0001 | 11df | ffff
Description:	Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	ADDWF TEMP_REG, 0

    Before Instruction
       W   = 0x17
       TEMP_REG = 0xC2
    After Instruction
       W   = 0xD9
       TEMP_REG = 0xC2

ANDWF	**AND W with f**
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	(W) .AND. (f) $\rightarrow$ (dest)
Status Affected:	Z
Encoding:	0001 | 01df | ffff
Description:	The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	ANDWF TEMP_REG, 1

    Before Instruction
       W   = 0x17
       TEMP_REG = 0xC2
    After Instruction
       W   = 0x17
       TEMP_REG = 0x02

ANDLW	**AND literal with W**
Syntax:	[*label*] ANDLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W).AND. (k) $\rightarrow$ (W)
Status Affected:	Z
Encoding:	1110 | kkkk | kkkk
Description:	The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1
Example:	ANDLW H'5F'

    Before Instruction
       W   = 0xA3
    After Instruction
       W   = 0x03

BCF	**Bit Clear f**
Syntax:	[*label*] BCF f,b
Operands:	$0 \leq f \leq 31$ $0 \leq b \leq 7$
Operation:	0 $\rightarrow$ (f<b>)
Status Affected:	None
Encoding:	0100 | bbbf | ffff
Description:	Bit 'b' in register 'f' is cleared.
Words:	1
Cycles:	1
Example:	BCF FLAG_REG, 7

    Before Instruction
       FLAG_REG = 0xC7
    After Instruction
       FLAG_REG = 0x47

MOVWF	Move W to f

Syntax:	[*label*] MOVWF f
Operands:	$0 \leq f \leq 31$
Operation:	$(W) \rightarrow (f)$
Status Affected:	None
Encoding:	`0000` `001f` `ffff`
Description:	Move data from the W register to register 'f'.
Words:	1
Cycles:	1
Example:	MOVWF TEMP_REG

    Before Instruction
        TEMP_REG =   0xFF
        W   =   0x4F
    After Instruction
        TEMP_REG =   0x4F
        W   =   0x4F

NOP	No Operation

Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Encoding:	`0000` `0000` `0000`
Description:	No operation.
Words:	1
Cycles:	1
Example:	NOP

OPTION	Load OPTION Register

Syntax:	[*label*] OPTION
Operands:	None
Operation:	$(W) \rightarrow OPTION$
Status Affected:	None
Encoding:	`0000` `0000` `0010`
Description:	The content of the W register is loaded into the OPTION register.
Words:	1
Cycles:	1
Example	OPTION

    Before Instruction
        W   =   0x07
    After Instruction
        OPTION   =   0x07

RETLW	Return with Literal in W

Syntax:	[*label*] RETLW k
Operands:	$0 \leq k \leq 255$
Operation:	$k \rightarrow (W)$; $TOS \rightarrow PC$
Status Affected:	None
Encoding:	`1000` `kkkk` `kkkk`
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Words:	1
Cycles:	2
Example:	CALL TABLE ;W contains

```
                   ;table offset
                   ;value.
      •            ;W now has table
      •            ;value.
TABLE •
      ADDWF PC  ;W = offset
      RETLW k1  ;Begin table
      RETLW k2  ;
      •
      •
      •
      RETLW kn  ; End of table
```

    Before Instruction
        W   =   0x07
    After Instruction
        W   =   value of k8

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RLF	**Rotate Left f through Carry**		**RRF**	**Rotate Right f through Carry**

<table>
<tr><td>Syntax:</td><td>[label]   RLF   f,d</td><td>Syntax:</td><td>[label]   RRF   f,d</td></tr>
<tr><td>Operands:</td><td>$0 \leq f \leq 31$
$d \in [0,1]$</td><td>Operands:</td><td>$0 \leq f \leq 31$
$d \in [0,1]$</td></tr>
<tr><td>Operation:</td><td>See description below</td><td>Operation:</td><td>See description below</td></tr>
<tr><td>Status Affected:</td><td>C</td><td>Status Affected:</td><td>C</td></tr>
</table>

Encoding:

0011	01df	ffff

Encoding:

0011	00df	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
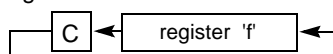
Words: 1

Cycles: 1

Example: `RLF    REG1,0`

Before Instruction
  REG1 = 1110 0110
  C   = 0
After Instruction
  REG1 = 1110 0110
  W   = 1100 1100
  C   = 1
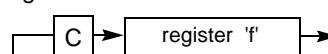
Words: 1

Cycles: 1

Example: `RRF    REG1,0`

Before Instruction
  REG1 = 1110 0110
  C   = 0
After Instruction
  REG1 = 1110 0110
  W   = 0111 0011
  C   = 0

SLEEP	**Enter SLEEP Mode**

Syntax: [*label*]   SLEEP

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler; if assigned
1 → $\overline{TO}$;
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

0000	0000	0011

Description: Time-out status bit ($\overline{TO}$) is set. The power-down status bit ($\overline{PD}$) is cleared. The WDT and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example: `SLEEP`

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11.0   DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/
    MPLIB™ Object Librarian
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM 2 Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - KEELOQ® Demonstration Board

11.1   MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows®-based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

11.2   MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

11.3   MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

12.6   Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 12-1:   LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54/55/56/57

C_L =   50 pF   for all pins and OSC2 for RC mode
0 - 15 pF   for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1
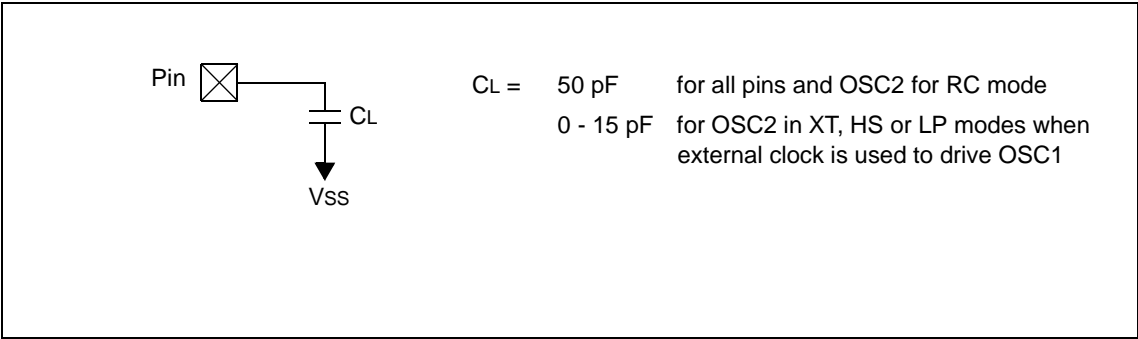
15.0   ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings[†]

Ambient temperature under bias .... −55°C to +125°C

Storage temperature .... −65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} .... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} .... 0 to +14V

Voltage on all other pins with respect to V_{SS} .... −0.6V to (V_{DD} + 0.6V)

Total power dissipation[1] .... 800 mW

Max. current out of V_{SS} pin .... 150 mA

Max. current into V_{DD} pin .... 100 mA

Max. current into an input pin (T0CKI only) .... ±500 μA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) .... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) .... ±20 mA

Max. output current sunk by any I/O pin .... 25 mA

Max. output current sourced by any I/O pin .... 20 mA

Max. output current sourced by a single I/O port (PORTA or B) .... 50 mA

Max. output current sunk by a single I/O port (PORTA or B) .... 50 mA

Note 1: Power dissipation is calculated as follows: $Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

---

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

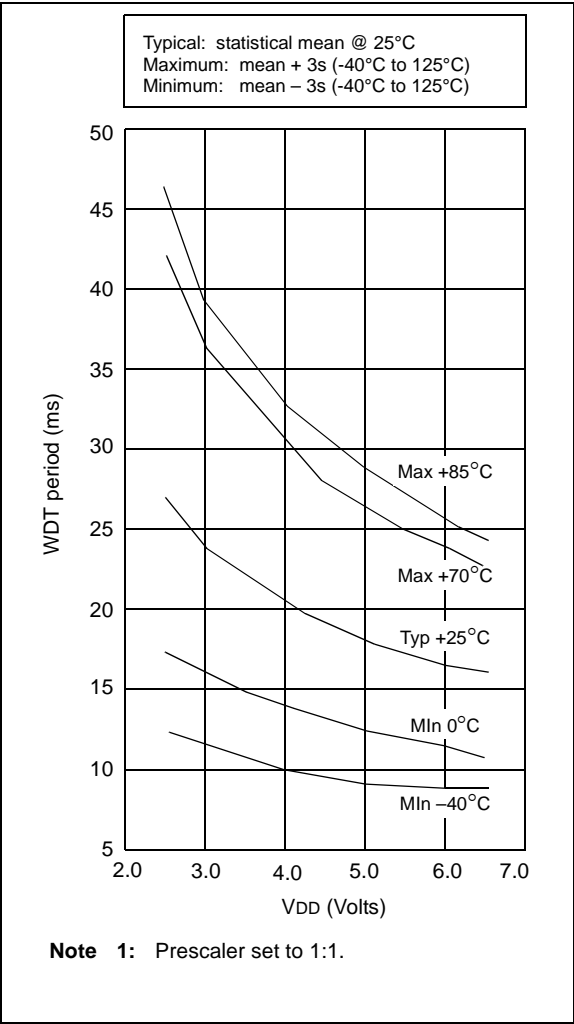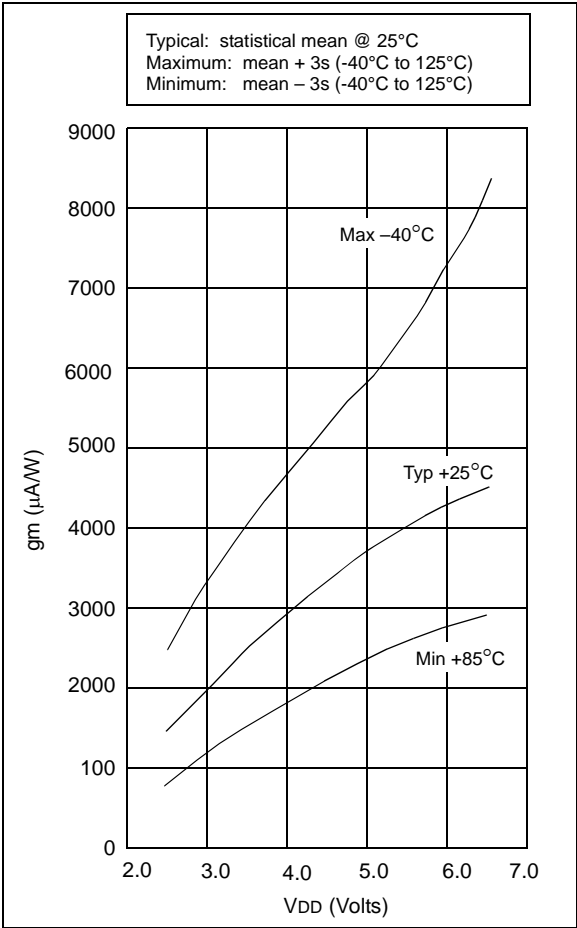# PIC16C5X

FIGURE 16-16: **WDT TIMER TIME-OUT PERIOD vs. V$_{DD}$**[1]

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Note   1: Prescaler set to 1:1.

FIGURE 16-17: **TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. V$_{DD}$**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
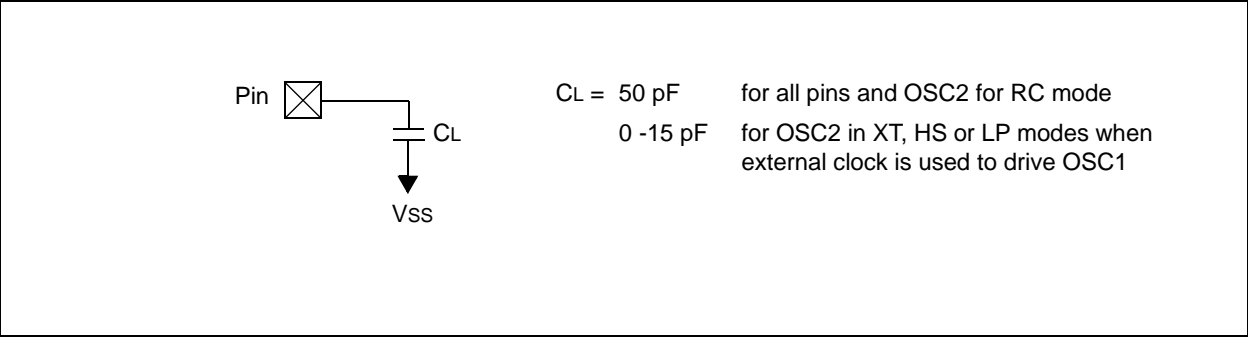Minimum: mean – 3s (-40°C to 125°C)

Preliminary

17.4   Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 17-5:   **LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B-04, 20**

Pin

C_L

Vss

$C_L =$ 50 pF   for all pins and OSC2 for RC mode

0 -15 pF   for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

PIC16C5X

FIGURE 17-9: TIMER0 CLOCK TIMINGS - PIC16C5X, PIC16CR5X

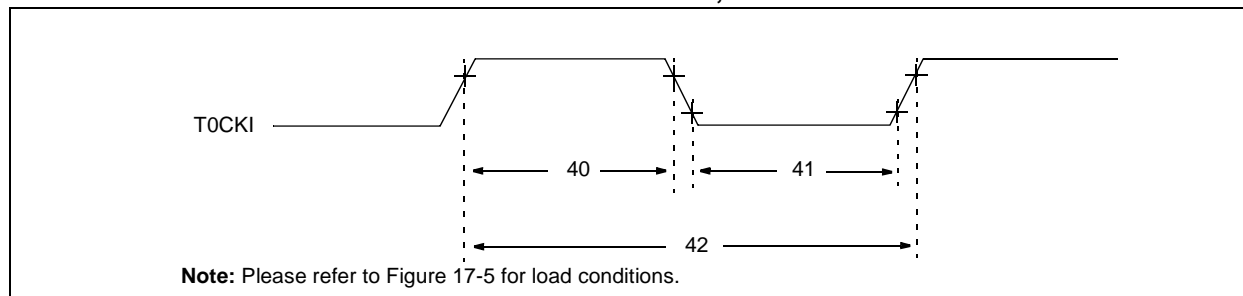**Note:** Please refer to Figure 17-5 for load conditions.

TABLE 17-4: TIMER0 CLOCK REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C $\leq$ TA $\leq$ +70°C for commercial −40°C $\leq$ TA $\leq$ +85°C for industrial −40°C $\leq$ TA $\leq$ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	$\frac{20 \text{ or } \underline{T_{CY} + 40}^*}{N}$	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

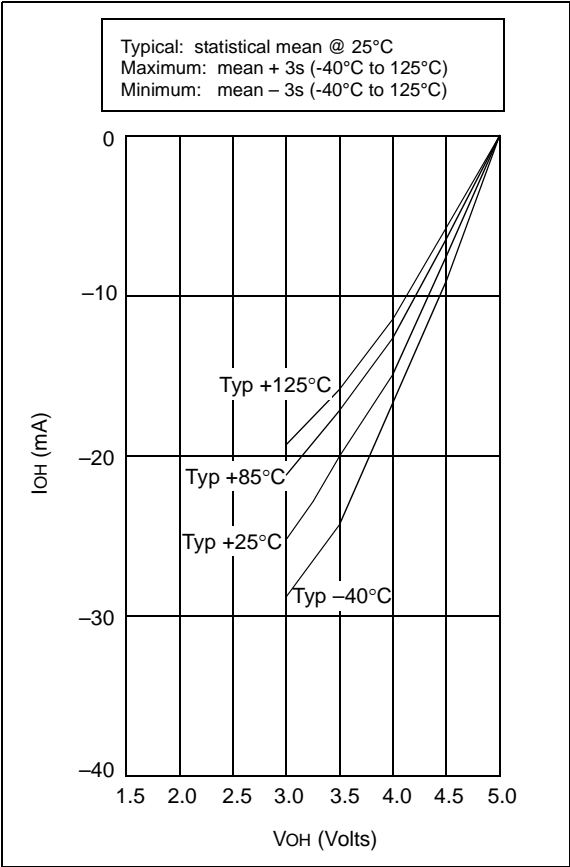**Preliminary**
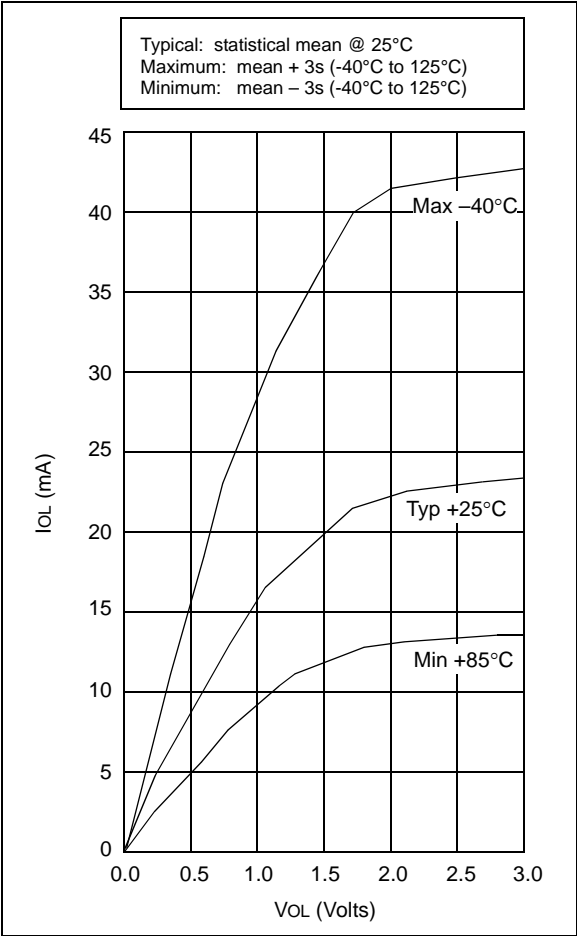
FIGURE 18-16: PORTA, B AND C I$_{OH}$ vs. V$_{OH}$, V$_{DD}$ = 5 V

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Typ +125°C
Typ +85°C
Typ +25°C
Typ –40°C

I$_{OH}$ (mA)
V$_{OH}$ (Volts)

FIGURE 18-17: PORTA, B AND C I$_{OL}$ vs. V$_{OL}$, V$_{DD}$ = 3 V

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Max –40°C
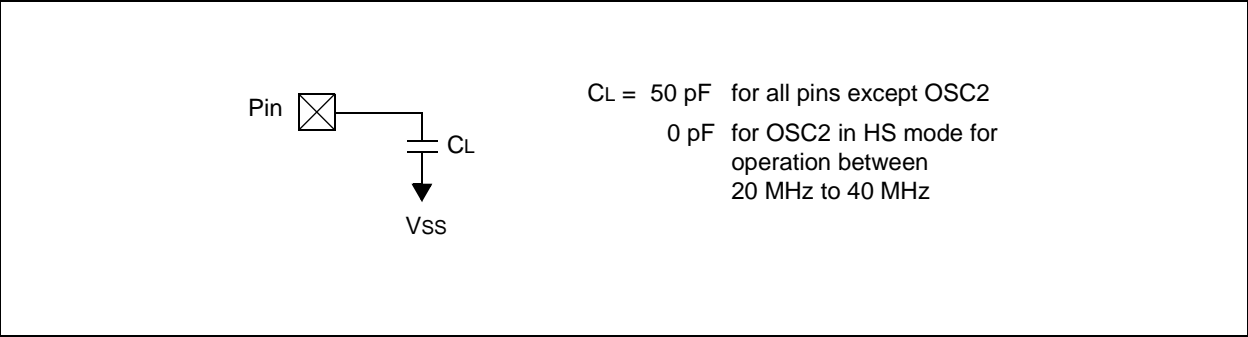Typ +25°C
Min +85°C

I$_{OL}$ (mA)
V$_{OL}$ (Volts)

19.3   Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 19-2:   LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54C/C55A/C56A/C57C/C58B-40

Pin ⊠ — C_L — Vss

C_L = 50 pF   for all pins except OSC2

0 pF   for OSC2 in HS mode for operation between 20 MHz to 40 MHz

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-	XX	X	/XX	XXX
Device		Frequency Range/OSC Type	Temperature Range	Package	Pattern

Device	PIC16C54 PIC16C54A PIC16CR54A PIC16C54C PIC16CR54C PIC16C55 PIC16C55A PIC16C56 PIC16C56A PIC16CR56A PIC16C57 PIC16C57C PIC16CR57C PIC16C58B PIC16CR58B	PIC16C54T[2] PIC16C54AT[2] PIC16CR54AT[2] PIC16C54CT[2] PIC16CR54CT[2] PIC16C55T[2] PIC16C55AT[2] PIC16C56T[2] PIC16C56AT[2] PIC16CR56AT[2] PIC16C57T[2] PIC16C57CT[2] PIC16CR57CT[2] PIC16C58BT[2] PIC16CR58BT[2]
Frequency Range/ Oscillator Type	RC Resistor Capacitor LP Low Power Crystal XT Standard Crystal/Resonator HS High Speed Crystal 02 200 KHz (LP) or 2 MHz (XT and RC) 04 200 KHz (LP) or 4 MHz (XT and RC) 10 10 MHz (HS only) 20 20 MHz (HS only) 40 40 MHz (HS only) b[4] No oscillator type for JW packages[3] *RC/LP/XT/HS are for 16C54/55/56/57 devices only -02 is available for 16LV54A only -04/10/20 options are available for all other devices -40 is available for 16C54C/55A/56A/57C/58B devices only	
Temperature Range	b[4] = 0°C to +70°C I = -40°C to +85°C E = -40°C to +125°C	
Package	S = Die in Waffle Pack JW = 28-pin 600 mil/18-pin 300 mil windowed CER-DIP[3] P = 28-pin 600 mil/18-pin 300 mil PDIP SO = 300 mil SOIC SS = 209 mil SSOP SP = 28-pin 300 mil Skinny PDIP *See Section 21 for additional package information.	
Pattern	QTP, SQTP, ROM code (factory specified) or Special Requirements. Blank for OTP and Windowed devices.	

Examples:

a) PIC16C55A - 04/P 301 = Commercial Temp., PDIP package, 4 MHz, standard V_{DD} limits, QTP pattern #301

b) PIC16LC54C - 04I/SO Industrial Temp., SOIC package, 200 kHz, extended V_{DD} limits

c) PIC16C57 - RC/SP = RC Oscillator, commercial temp, skinny PDIP package, 4 MHz, standard V_{DD} limits

d) PIC16C58BT -40/SS 123 = commercial temp, SSOP package in tape and reel, 4 MHz, extended V_{DD} limits, ROM pattern #123

Note 1: C = normal voltage range
LC = extended

2: T = in tape and reel - SOIC and SSOP packages only

3: JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirements of each oscillator type, including LC devices.

4: b = Blank

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Worldwide Site (www.microchip.com)

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