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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	24 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c55-xti-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

PIC16C5X



FIGURE 5-4: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME



FIGURE 5-5: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): SLOW VDD RISE TIME



9.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT Reset or Wake-up Reset generates a device RESET.

The $\overline{\text{TO}}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset (Section 6.3).

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 9.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

9.2.1 WDT PERIOD

An 8-bit counter is available as a prescaler for the Timer0 module (Section 8.2), or as a postscaler for the Watchdog Timer (WDT), respectively. For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not

both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio (Section 6.4).

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see Device Characterization).

Under worst case conditions (VDD = Min., Temperature = Max., WDT prescaler = 1:128), it may take several seconds before a WDT time-out occurs.

9.2.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction RESETS the WDT and the prescaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.



TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	<u>Value</u> on MCLR and WDT Reset
N/A	OPTION	—	—	Tosc	Tose	PSA	PS2	PS1	PS0	11 1111	11 1111

Legend: u = unchanged, - = unimplemented, read as '0'. Shaded cells not used by Watchdog Timer.

9.3 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

9.3.1 SLEEP

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the TO bit (STATUS<4>) is set, the PD bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the MCLR/VPP pin low.

For lowest current consumption while powered down, the T0CKI input should be at VDD or Vss and the $\overline{\text{MCLR}}/\text{VPP}$ pin must be at a logic high level ($\overline{\text{MCLR}} = \text{VIH}$).

9.3.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

- 1. An external RESET input on MCLR/VPP pin.
- 2. A Watchdog Timer Time-out Reset (if WDT was enabled).

Both of these events cause a device RESET. The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits can be used to determine the cause of device RESET. The $\overline{\text{TO}}$ bit is cleared if a WDT timeout occurred (and caused wake-up). The $\overline{\text{PD}}$ bit, which is set on power-up, is cleared when SLEEP is invoked.

The WDT is cleared when the device wakes from SLEEP, regardless of the wake-up source.

9.4 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip does not recommend code pro-
	tecting windowed devices.

9.5 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

Note: Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

NOTES:

12.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings^(†)

Ambient Temperature under bias	–55°C to +125°C
Storage Temperature	65°C to +150°C
Voltage on VDD with respect to VSS	0V to +7.5V
Voltage on MCLR with respect to Vss ⁽¹⁾	0V to +14V
Voltage on all other pins with respect to Vss	0.6V to (VDD + 0.6V)
Total power dissipation ⁽²⁾	800 mW
Max. current out of Vss pin	150 mA
Max. current into VDD pin	100 mA
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, Iik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)	±20 mA
Max. output current sunk by any I/O pin	
Max. output current sourced by any I/O pin	
Max. output current sourced by a single I/O port (PORTA, B or C)	40 mA
Max. output current sunk by a single I/O port (PORTA, B or C)	50 mA

- **Note 1:** Voltage spikes below Vss at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a "low" level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to Vss.
 - **2:** Power Dissipation is calculated as follows: Pdis = VDD x {IDD $-\Sigma$ IOH} + Σ {(VDD VOH) x IOH} + Σ (VOL x IOL)

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

12.3 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions	
D001	Vdd	Supply Voltage PIC16C5X-RCE PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-LPE	3.25 3.25 4.5 4.5 2.5		6.0 6.0 5.5 5.5 6.0	V V V V V		
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	_	V	Device in SLEEP mode	
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset	
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset	
D010	IDD	Supply Current ⁽²⁾ PIC16C5X-RCE ⁽³⁾ PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-HSE PIC16C5X-LPE		1.8 1.8 4.8 9.0 19	3.3 3.3 10 10 20 55	mA mA mA mA μA	Fosc = 4 MHz, VDD = $5.5V$ Fosc = 4 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 16 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $3.25V$, WDT disabled	
D020	IPD	Power-down Current ⁽²⁾	_	5.0 0.8	22 18	μΑ μΑ	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled	

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

13.3 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

DC CHARACTERISTICS			$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$					
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
D030	VIL	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD	> > > > >	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes	
D040	Viн	Input High Voltage I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	2.0 0.6 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD		VDD VDD VDD VDD VDD VDD	V V V V V	VDD = 3.0V to 5.5V ⁽⁴⁾ Full VDD range ⁽⁴⁾ RC mode only ⁽³⁾ XT, HS and LP modes	
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	_	_	V		
D060	lı∟	Input Leakage Current ^(1,2) I/O ports	-1.0	_	+1.0	μA	For VDD \leq 5.5V: VSS \leq VPIN \leq VDD, pin at hi-impedance	
		MCLR MCLR TOCKI OSC1	-5.0 -3.0 -3.0	 0.5 0.5 0.5		μΑ μΑ μΑ μΑ	$VPIN = VSS + 0.25V$ $VPIN = VDD$ $VSS \le VPIN \le VDD$ $VSS \le VPIN \le VDD,$ $XT, HS and LP modes$	
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.5 0.5	V V	IOL = 10 mA, VDD = 6.0 V IOL = 1.9 mA, VDD = 6.0 V, RC mode only	
D090	Vон	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	Vdd – 0.5 Vdd – 0.5	_		V V	IOH = -4.0 mA, VDD = 6.0 V IOH = -0.8 mA, VDD = 6.0 V, RC mode only	

* These parameters are characterized but not tested.

- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- **Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
 - 2: Negative current is defined as coming out of the pin.
 - **3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
 - 4: The user may use the better of the two specifications.

PIC16C5X

FIGURE 14-2: TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 20 PF Typical: statistical mean @ 25°C Maximum: mean + 3s (-40°C to 125°C) Minimum: mean – 3s (-40°C to 125°C) 5.5 R = 3.3K5.0 4.5 R = 5K 4.0 3.5 Fosc (MHz) 3.0 R = 10K 2.5 2.0 Measured on DIP Packages, $T = 25^{\circ}C$ 1.5 1.0 R = 100K 0.5 0.0 3.0 3.5 4.0 4.5 5.0 5.5 6.0 VDD (Volts)

FIGURE 14-3:

TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 100 PF



15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04 PIC16LC54A-04I (Commercial, Industrial)				ard Ope ting Tem	perating	J Condi ure 	tions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $40^{\circ}C \le TA \le +85^{\circ}C$ for industrial
$ \begin{array}{ c c c c c } \mbox{PIC16C54A-04, 10, 20} \\ \mbox{PIC16C54A-04I, 10I, 20I} \\ \mbox{(Commercial, Industrial)} \end{array} & \begin{array}{ c c c c c c } \mbox{Standard Operating Conditions (unless otherwide)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C for index of the second secon$				tions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $40^{\circ}C \le TA \le +85^{\circ}C$ for industrial			
Param No.	Symbol	Characteristic/Device	Min Typ† Max Units Conditions				
	IPD	Power-down Current ⁽²⁾					
D006		PIC16LC5X	—	2.5	12	μΑ	VDD = 2.5V, WDT enabled, Commercial
			—	0.25	4.0	μΑ	VDD = 2.5V, WDT disabled, Commercial
			_	0.25	5.0	μΑ μΑ	VDD = 2.5V, WDT enabled, industrial $VDD = 2.5V$, WDT disabled, Industrial
D006A		PIC16C5X	_	4.0	12	μΑ	VDD = 3.0V, WDT enabled, Commercial
			—	0.25	4.0	μA	VDD = 3.0V, WDT disabled, Commercial
			—	5.0	14	μΑ	VDD = 3.0V, WDT enabled, Industrial
				0.3	5.0	μA	$v \Box U = 3.0v, v U T uisabled, industrial$

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .



FIGURE 16-10: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 PF, 25°C)

FIGURE 16-11: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 PF, -40°C to +85°C)





TABLE 16-2:INPUT CAPACITANCE FOR
PIC16C54A/C58A

Pin	Typical Capacitance (pF)				
FIII	18L PDIP	18L SOIC			
RA port	5.0	4.3			
RB port	5.0	4.3			
MCLR	17.0	17.0			
OSC1	4.0	3.5			
OSC2/CLKOUT	4.3	3.5			
TOCKI	3.2	2.8			

All capacitance values are typical at 25°C. A part-to-part variation of $\pm 25\%$ (three standard deviations) should be taken into account.

FIGURE 16-23: PORTA, B AND C IOL vs. VoL, VDD = 5V



17.3 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial, Extended) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial, Extended) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

DC CH	ARACTE	RISTICS	$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
D030	VIL	Input Low Voltage I/O Ports I/O Ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss Vss Vss	 	0.8 V 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V V	4.5V <v<sub>DD ≤ 5.5V Otherwise RC mode only⁽³⁾ XT, HS and LP modes</v<sub>	
D040	Vih	Input High Voltage I/O ports I/O ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	2.0 0.25 Vdd+0.8 0.85 Vdd 0.85 Vdd 0.85 Vdd 0.85 Vdd 0.7 Vdd	 	Vdd Vdd Vdd Vdd Vdd Vdd Vdd	V V V V V	4.5V < V _{DD} ≤ 5.5V Otherwise RC mode only ⁽³⁾ XT, HS and LP modes	
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	—	_	V		
D060	lı∟	Input Leakage Current ^(1,2) I/O ports	-1.0	0.5	+1.0	μA	For VDD \leq 5.5V: VSS \leq VPIN \leq VDD, pin at hi-impedance	
		MCLR MCLR T0CKI OSC1	-5.0 -3.0 -3.0	— 0.5 0.5 0.5	+5.0 +3.0 +3.0 —	μΑ μΑ μΑ μΑ	$VPIN = VSS +0.25V$ $VPIN = VDD$ $VSS \le VPIN \le VDD$ $VSS \le VPIN \le VDD,$ $XT, HS and LP modes$	
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5 V IOL = 1.6 mA, VDD = 4.5 V, RC mode only	
D090	Vон	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	Vdd - 0.7 Vdd - 0.7			V V	IOH = -5.4 mA, VDD = 4.5 V IOH = -1.0 mA, VDD = 4.5 V, RC mode only	

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
 - **2:** Negative current is defined as coming out of the pin.
 - 3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.



TABLE 18-2:INPUT CAPACITANCE

Bin	Typical Capacitance (pF)				
FIII	18L PDIP	18L SOIC			
RA port	5.0	4.3			
RB port	5.0	4.3			
MCLR	17.0	17.0			
OSC1	4.0	3.5			
OSC2/CLKOUT	4.3	3.5			
TOCKI	3.2	2.8			

All capacitance values are typical at 25° C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.



	ALVAUT AND VA TIMINA DEALIDEMENTA DIA AASY (A
IABLE 19-2:	CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X-40

AC Chara	acteristics	Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units			
10	TosH2ckL	OSC1↑ to CLKOUT↓ ^(1,2)		15	30**	ns			
11	TosH2ckH	OSC1↑ to CLKOUT↑ ^(1,2)	—	15	30**	ns			
12	TckR	CLKOUT rise time ^(1,2)	—	5.0	15**	ns			
13	TckF	CLKOUT fall time ^(1,2)	—	5.0	15**	ns			
14	TckL2ioV	CLKOUT↓ to Port out valid ^(1,2)	—		40**	ns			
15	TioV2ckH	Port in valid before CLKOUT ^(1,2)	0.25 TCY+30*	—	—	ns			
16	TckH2iol	Port in hold after CLKOUT ^(1,2)	0*	—	—	ns			
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽²⁾	—	—	100	ns			
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns			
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns			
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns			
21	TioF	Port output fall time ⁽²⁾		10	25**	ns			

* These parameters are characterized but not tested.

- ** These parameters are design targets and are not tested. No characterization data available at this time.
- † Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Refer to Figure 19-2 for load conditions.

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21.0 PACKAGING INFORMATION

21.1 Package Marketing Information

18-Lead PDIP



28-Lead Skinny PDIP (.300")



28-Lead PDIP (.600")



18-Lead SOIC



28-Lead SOIC



20-Lead SSOP



28-Lead SSOP





Example



Example



Example



Example



Example



Example



28-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









	Units	INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.026			0.65	
Overall Height	Α	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.319	7.59	7.85	8.10
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.396	.402	.407	10.06	10.20	10.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25
Foot Angle	¢	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-150 Drawing No. C04-073

APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

- 1. Check any CALL, GOTO or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
- 2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change RESET vector to proper value for processor used.
- 6. Remove any use of the ADDLW, RETURN and SUBLW instructions.
- 7. Rewrite any code segments that use interrupts.

APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.

w

W Register	
Value on reset	20
Wake-up from SLEEP	19, 47
Watchdog Timer (WDT)	43, 46
Period	
Programming Considerations	
Register values on reset	
WWW, On-Line Support	3
X	
XORLW	60
XORWF	60
Z	
Zero (Z) bit	9, 29