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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16c55a-04i-p">https://www.e-xfl.com/product-detail/microchip-technology/pic16c55a-04i-p</a>



# PIC16C5X

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## 8-Bit EPROM/ROM-Based CMOS Microcontrollers

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### 1.0 GENERAL DESCRIPTION

The PIC16C5X from Microchip Technology is a family of low cost, high performance, 8-bit fully static, EPROM/ROM-based CMOS microcontrollers. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle except for program branches which take two cycles. The PIC16C5X delivers performance in an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C5X products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external RESET circuitry. There are four oscillator configurations to choose from, including the power saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and Code Protection features improve system cost, power and reliability.

The UV erasable Cerdip packaged versions are ideal for code development, while the cost effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers, while benefiting from the OTP's flexibility.

The PIC16C5X products are supported by a full featured macro assembler, a software simulator, an in-circuit emulator, a low cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

### 1.1 Applications

The PIC16C5X series fits perfectly in applications ranging from high speed automotive and appliance motor control to low power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customizing application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low cost, low power, high performance ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, co-processor applications).

## 6.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the  $\overline{TO}$  and  $\overline{PD}$  bits are not

writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS Register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 10.0, Instruction Set Summary.

### REGISTER 6-1: STATUS REGISTER (ADDRESS: 03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7			bit 0				

bit 7: **PA2:** This bit unused at this time.

Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

bit 6-5: **PA<1:0>:** Program page preselect bits (PIC16C56/CR56)(PIC16C57/CR57)(PIC16C58/CR58)

00 = Page 0 (000h - 1FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58

01 = Page 1 (200h - 3FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58

10 = Page 2 (400h - 5FFh) - PIC16C57/CR57, PIC16C58/CR58

11 = Page 3 (600h - 7FFh) - PIC16C57/CR57, PIC16C58/CR58

Each page is 512 words.

Using the PA<1:0> bits as general purpose read/write bits in devices which do not use them for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4:  **$\overline{TO}$ :** Time-out bit

1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction

0 = A WDT time-out occurred

bit 3:  **$\overline{PD}$ :** Power-down bit

1 = After power-up or by the `CLRWDT` instruction

0 = By execution of the `SLEEP` instruction

bit 2: **Z:** Zero bit

1 = The result of an arithmetic or logic operation is zero

0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC:** Digit carry/borrow bit (for `ADDWF` and `SUBWF` instructions)

**ADDWF**

1 = A carry from the 4th low order bit of the result occurred

0 = A carry from the 4th low order bit of the result did not occur

**SUBWF**

1 = A borrow from the 4th low order bit of the result did not occur

0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C:** Carry/borrow bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

**ADDWF**

1 = A carry occurred

0 = A carry did not occur

**SUBWF**

1 = A borrow did not occur

0 = A borrow occurred

**RRF or RLF**

Loaded with LSb or MSb, respectively

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

1 = bit is set

0 = bit is cleared

x = bit is unknown

## 8.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

### 8.1.1 EXTERNAL CLOCK SYNCHRONIZATION

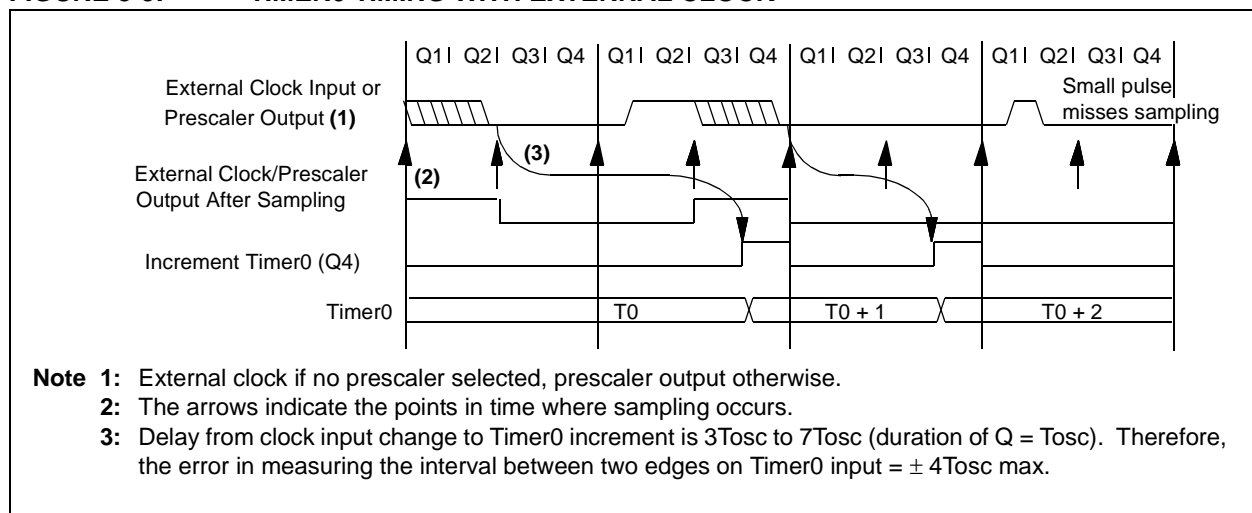
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 8-5). Therefore, it is necessary for T0CKI to be high for at least  $2T_{osc}$  (and a small RC delay of 20 ns) and low for at least  $2T_{osc}$  (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least  $4T_{osc}$  (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

### 8.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 8-5 shows the delay from the external clock edge to the timer incrementing.

**FIGURE 8-5: TIMER0 TIMING WITH EXTERNAL CLOCK**



# PIC16C5X

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NOTES:

## 10.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 10-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers in that bank is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

**TABLE 10-1: OPCODE FIELD DESCRIPTIONS**

Field	Description
f	Register file address (0x00 to 0x1F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
TO	Time-out bit
PD	Power-down bit
dest	Destination, either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
<i>italics</i>	User defined term (font is courier)

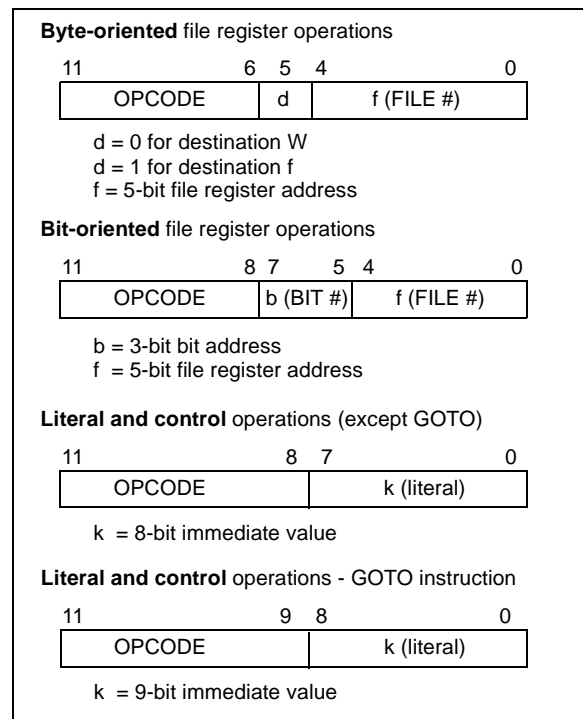
All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time would be 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time would be 2 μs.

Figure 10-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

**FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS**



## ADDWF Add W and f

Syntax: [ *label* ] ADDWF f,d

Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$

Operation:  $(W) + (f) \rightarrow (\text{dest})$

Status Affected: C, DC, Z

Encoding: 

0001	11df	ffff
------	------	------

Description: Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: ADDWF TEMP\_REG, 0

Before Instruction

W = 0x17  
TEMP\_REG = 0xC2

After Instruction

W = 0xD9  
TEMP\_REG = 0xC2

## ANDWF AND W with f

Syntax: [ *label* ] ANDWF f,d

Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$

Operation:  $(W) .\text{AND}. (f) \rightarrow (\text{dest})$

Status Affected: Z

Encoding: 

0001	01df	ffff
------	------	------

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: ANDWF TEMP\_REG, 1

Before Instruction

W = 0x17  
TEMP\_REG = 0xC2

After Instruction

W = 0x17  
TEMP\_REG = 0x02

## ANDLW AND literal with W

Syntax: [ *label* ] ANDLW k

Operands:  $0 \leq k \leq 255$

Operation:  $(W) .\text{AND}. (k) \rightarrow (W)$

Status Affected: Z

Encoding: 

1110	kkkk	kkkk
------	------	------

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: ANDLW H'5F'

Before Instruction

W = 0xA3

After Instruction

W = 0x03

## BCF Bit Clear f

Syntax: [ *label* ] BCF f,b

Operands:  $0 \leq f \leq 31$   
 $0 \leq b \leq 7$

Operation:  $0 \rightarrow (f<b>)$

Status Affected: None

Encoding: 

0100	bbbf	ffff
------	------	------

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example: BCF FLAG\_REG, 7

Before Instruction

FLAG\_REG = 0xC7

After Instruction

FLAG\_REG = 0x47

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## **XORLW**      **Exclusive OR literal with W**

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Syntax:      `[label] XORLW k`

Operands:     $0 \leq k \leq 255$

Operation:     $(W) .XOR. k \rightarrow (W)$

Status Affected: Z

Encoding:    

1111	kkkk	kkkk
------	------	------

Description:    The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words:        1

Cycles:        1

Example:      `XORLW 0xAF`

Before Instruction

W      =    0xB5

After Instruction

W      =    0x1A

## **XORWF**      **Exclusive OR W with f**

---

Syntax:      `[label] XORWF f,d`

Operands:     $0 \leq f \leq 31$   
               $d \in [0,1]$

Operation:     $(W) .XOR. (f) \rightarrow (dest)$

Status Affected: Z

Encoding:    

0001	10df	ffff
------	------	------

Description:    Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words:        1

Cycles:        1

Example      `XORWF REG,1`

Before Instruction

REG      =    0xAF

W        =    0xB5

After Instruction

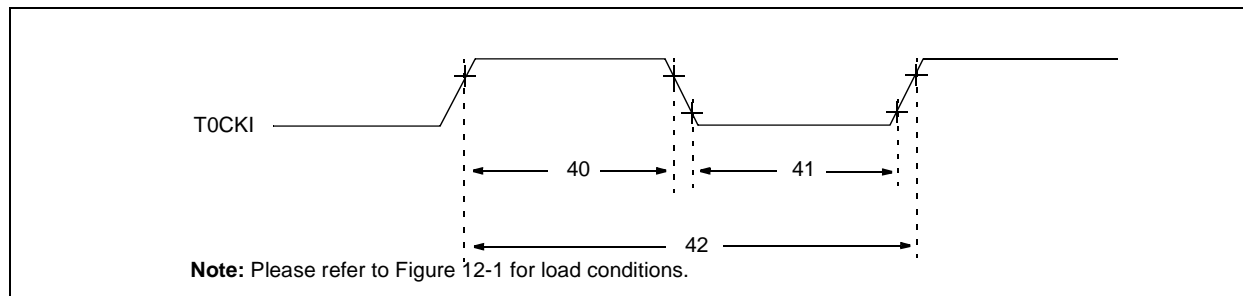
REG      =    0x1A

W        =    0xB5



# PIC16C5X

**FIGURE 12-5: TIMER0 CLOCK TIMINGS - PIC16C54/55/56/57**



**TABLE 12-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54/55/56/57**

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
		- With Prescaler	$10^*$	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
		- With Prescaler	$10^*$	—	—	ns	
42	Tt0P	T0CKI Period	$20$ or $\frac{T_{CY} + 40^*}{N}$	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

\* These parameters are characterized but not tested.

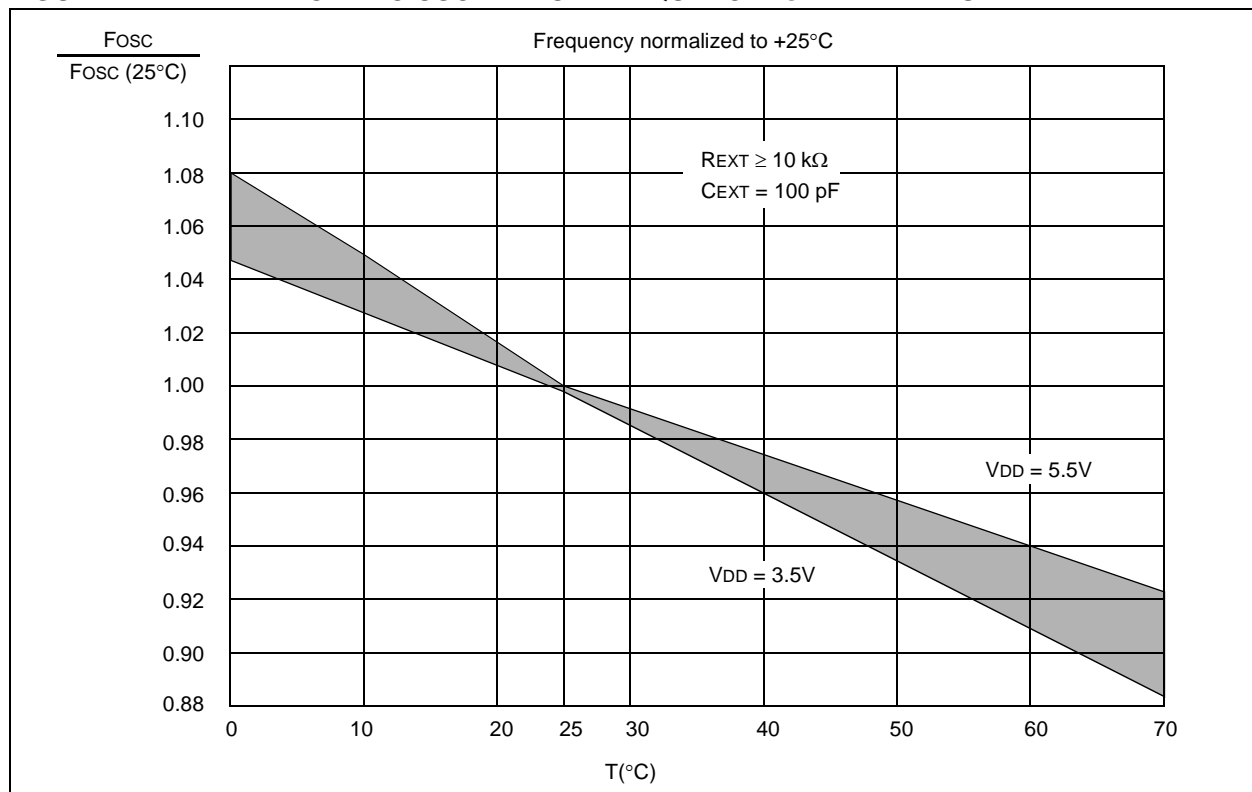
† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## 14.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum” or “minimum” represents (mean + 3 $\sigma$ ) or (mean – 3 $\sigma$ ) respectively, where  $\sigma$  is a standard deviation, over the whole temperature range.

**FIGURE 14-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE**



**TABLE 14-1: RC OSCILLATOR FREQUENCIES**

$C_{EXT}$	$R_{EXT}$	Average $F_{osc}$ @ 5 V, 25°C	
20 pF	3.3K	5 MHz	± 27%
	5K	3.8 MHz	± 21%
	10K	2.2 MHz	± 21%
	100K	262 kHz	± 31%
100 pF	3.3K	1.6 MHz	± 13%
	5K	1.2 MHz	± 13%
	10K	684 kHz	± 18%
	100K	71 kHz	± 25%
300 pF	3.3K	660 kHz	± 10%
	5.0K	484 kHz	± 14%
	10K	267 kHz	± 15%
	100K	29 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is  $\pm 3$  standard deviations from the average value for  $V_{DD} = 5\text{V}$ .

FIGURE 14-2: TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 20 PF

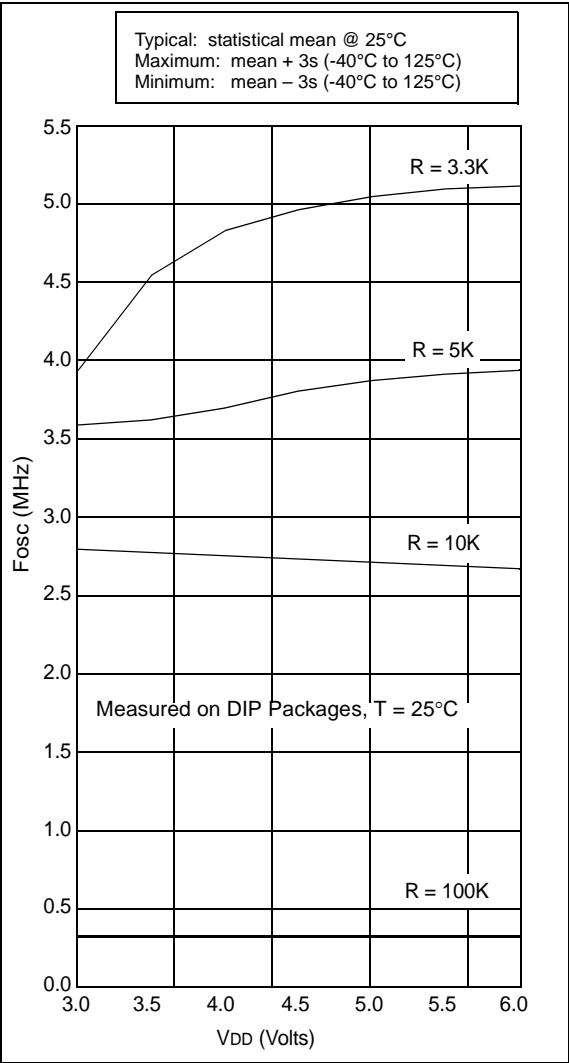
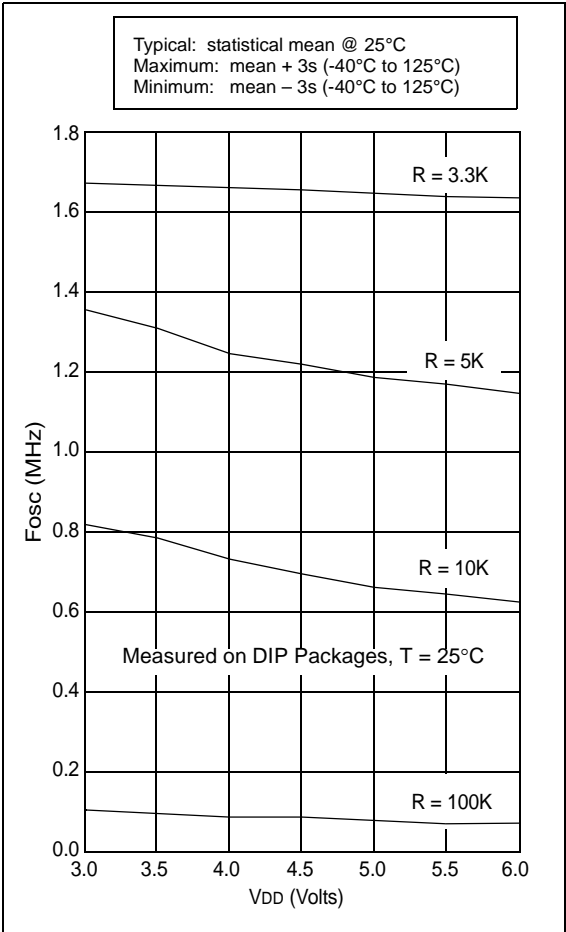
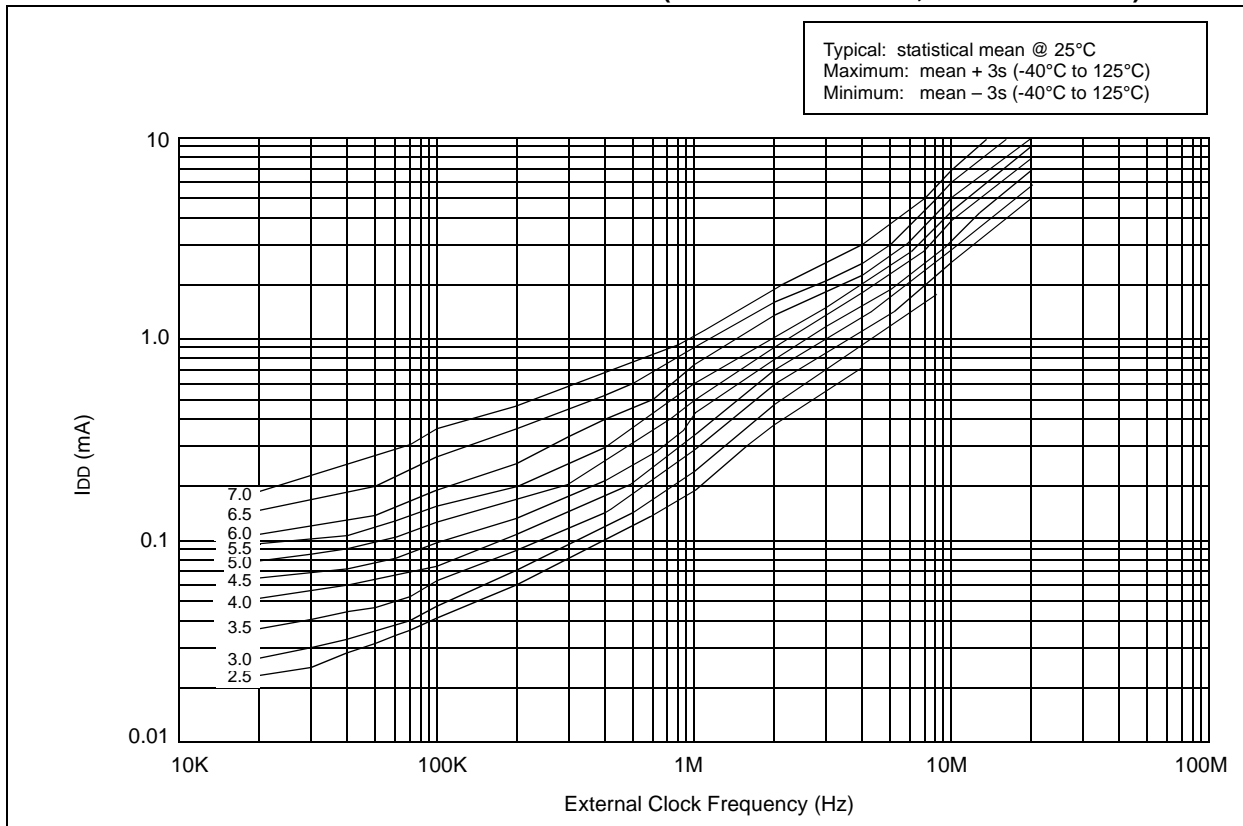


FIGURE 14-3: TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 100 PF



**FIGURE 14-13: MAXIMUM IDD VS. FREQUENCY (EXTERNAL CLOCK, -40°C TO +85°C)**



**FIGURE 14-14: MAXIMUM  $I_{DD}$  vs. FREQUENCY (EXTERNAL CLOCK -55°C TO +125°C)**

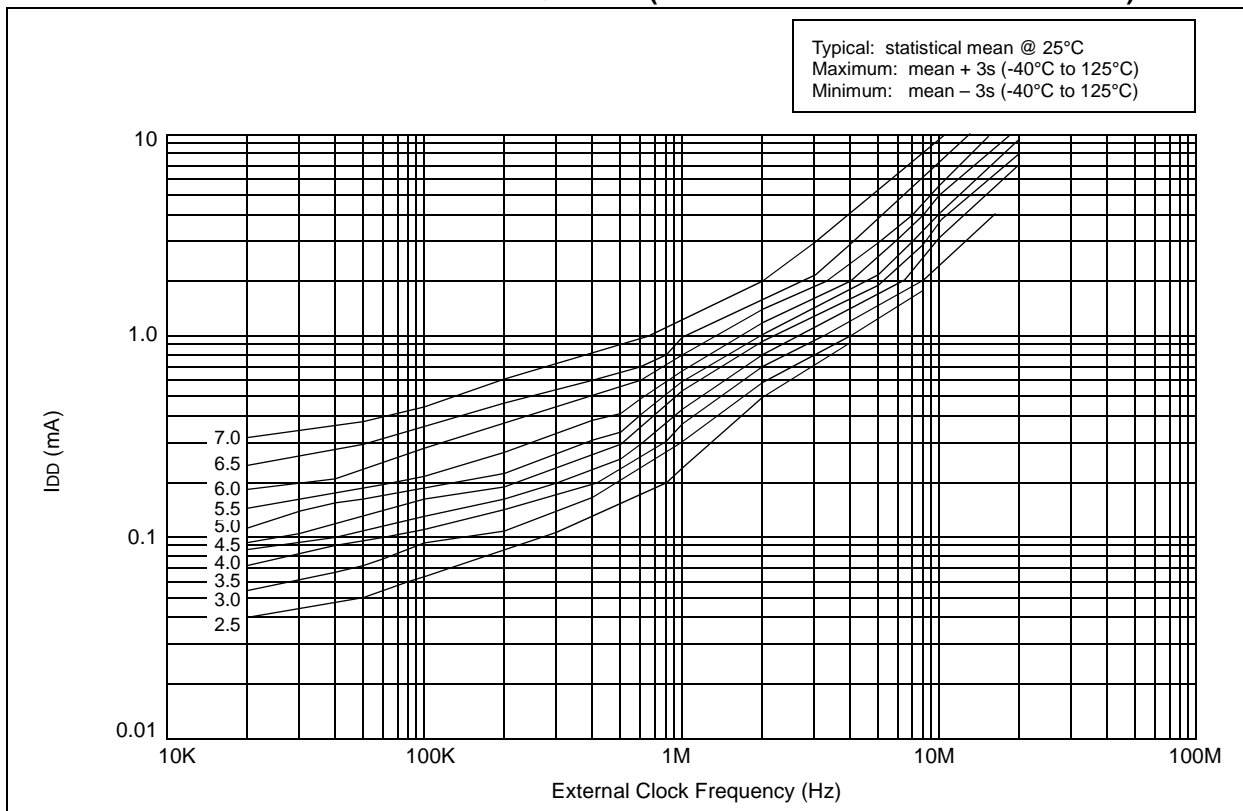


FIGURE 14-19: PORTA, B AND C I<sub>OH</sub> vs. V<sub>OH</sub>, V<sub>DD</sub> = 3 V

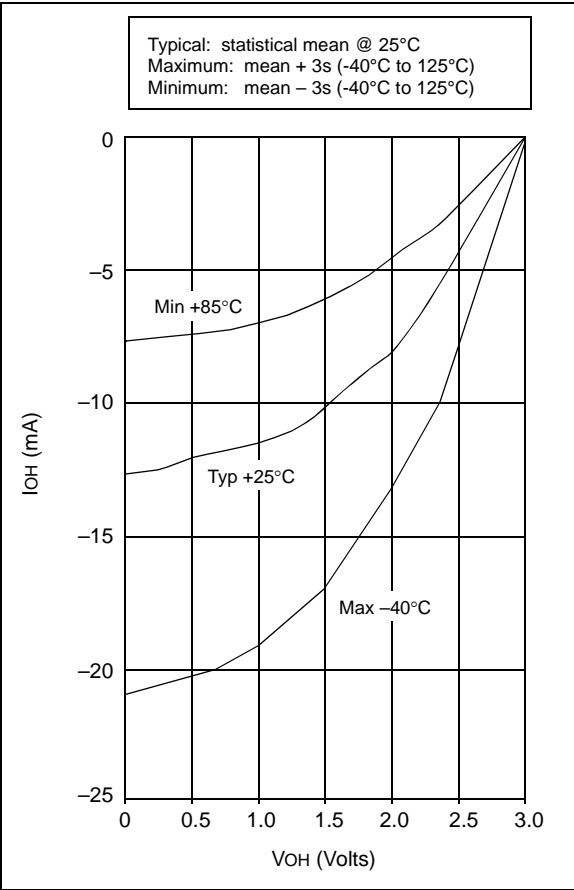
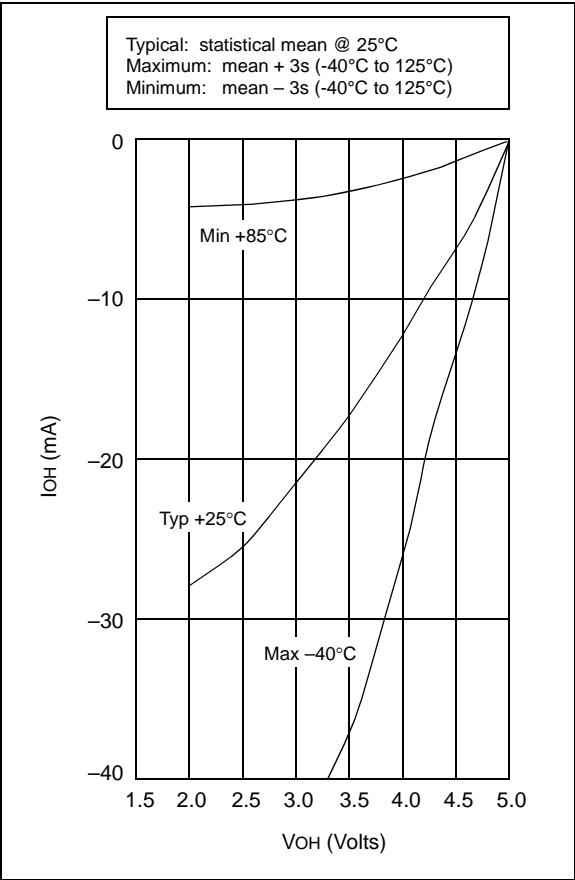
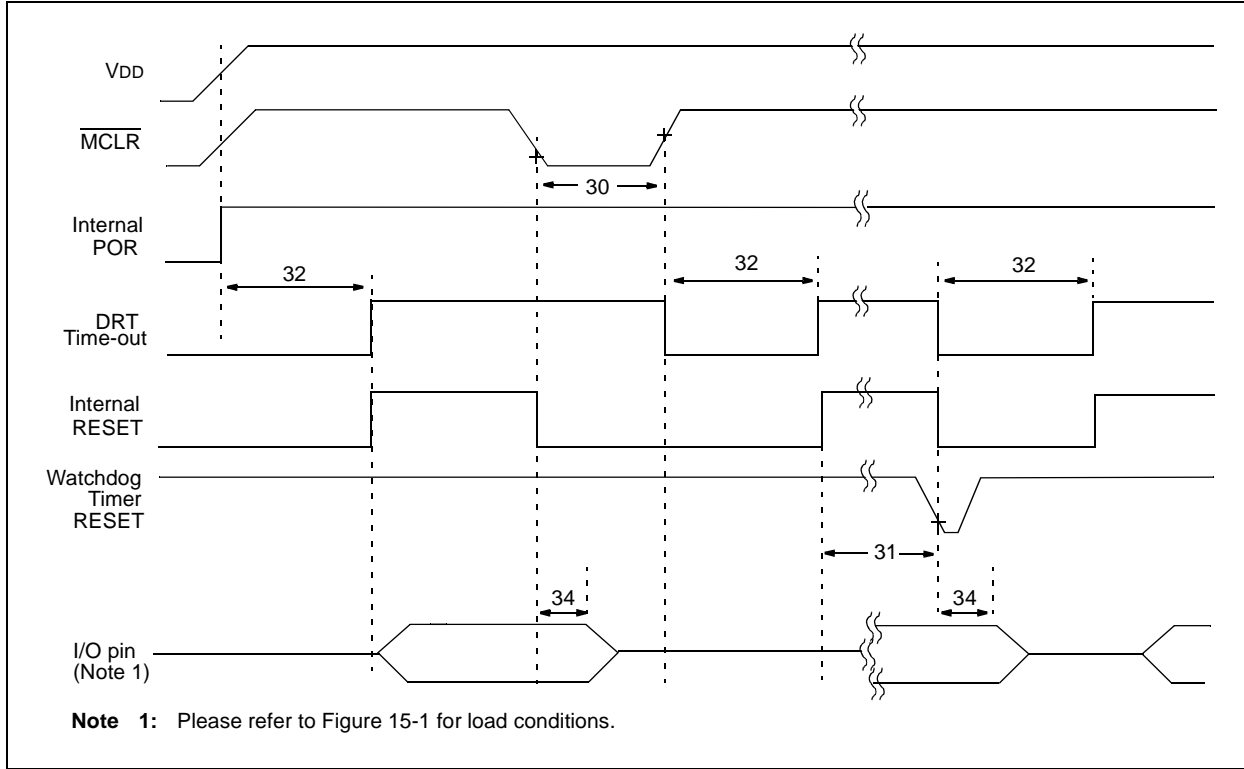


FIGURE 14-20: PORTA, B AND C I<sub>OH</sub> vs. V<sub>OH</sub>, V<sub>DD</sub> = 5 V



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**FIGURE 15-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A**



**TABLE 15-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A**

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics							
		Operating Temperature					
		0°C ≤ TA ≤ +70°C for commercial					
		-40°C ≤ TA ≤ +85°C for industrial					
		-20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I					
		-40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	100* 1	— —	— —	ns μs	VDD = 5.0V VDD = 5.0V (PIC16LV54A only)
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	TioZ	I/O Hi-impedance from MCLR Low	— —	— —	100* 1μs	ns —	(PIC16LV54A only)

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 16-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF, 25°C

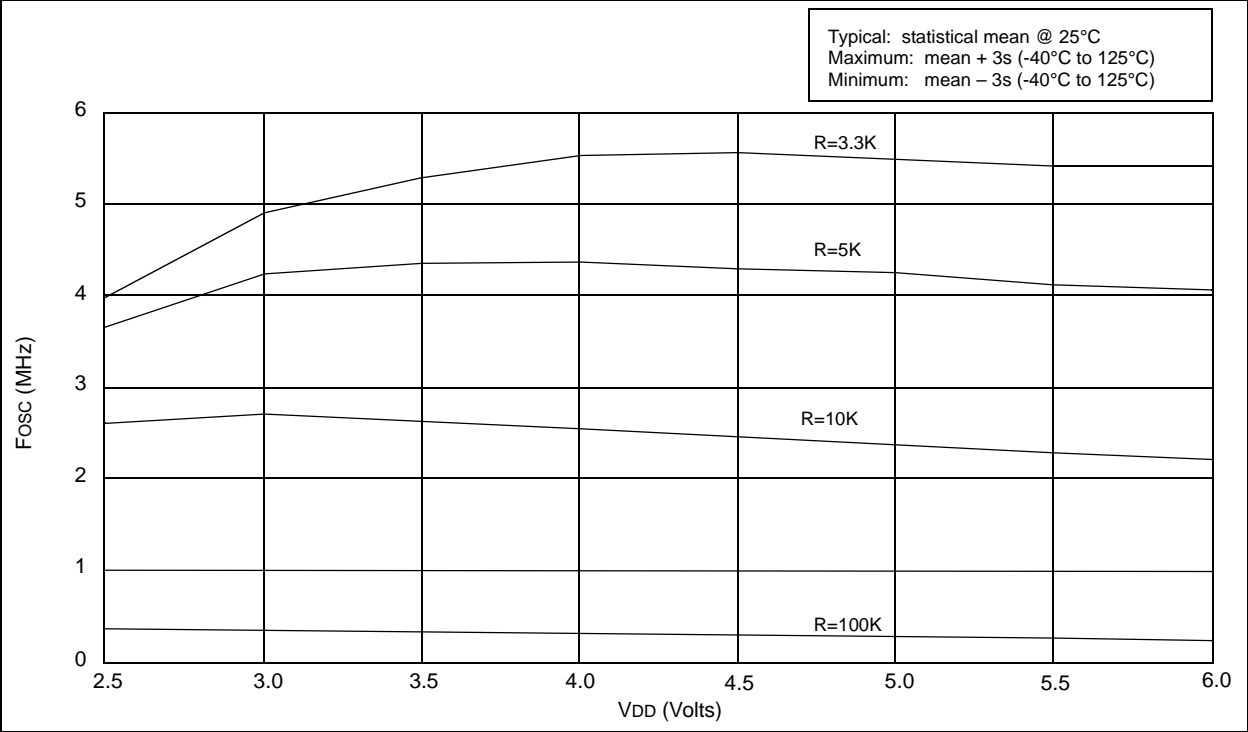


FIGURE 16-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF, 25°C

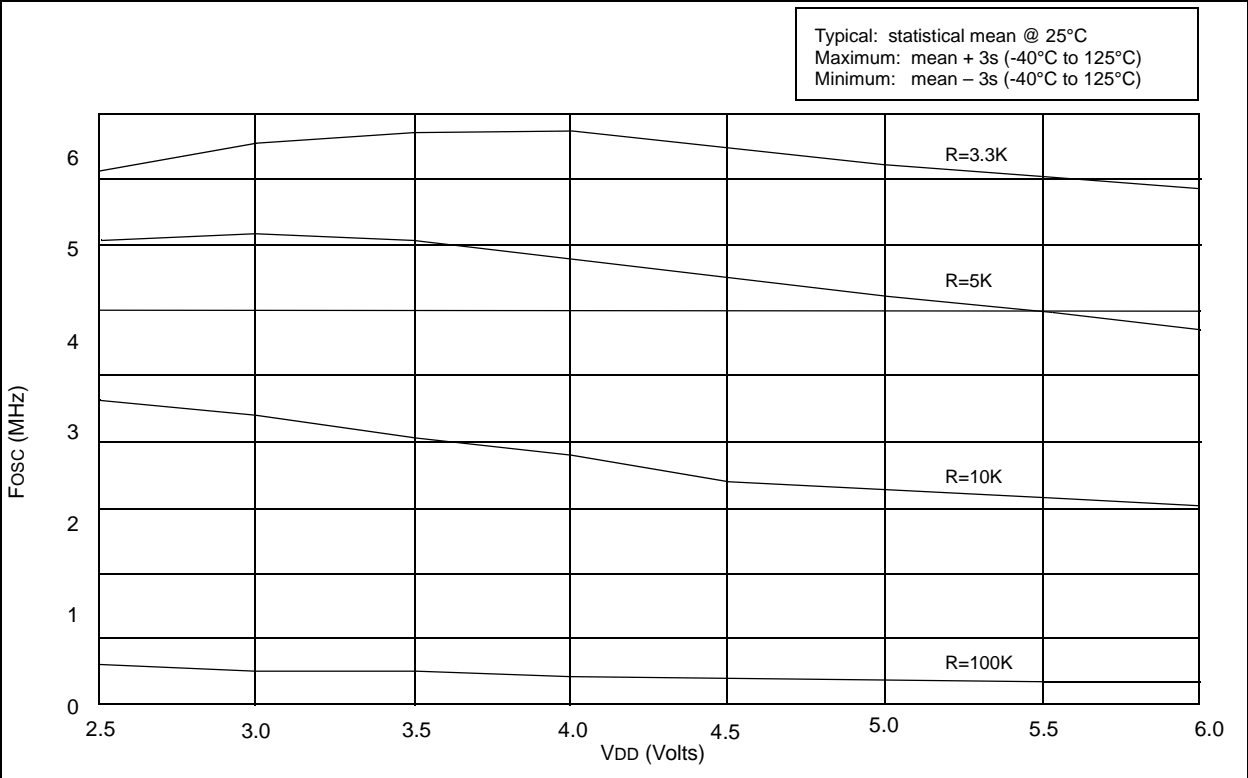


FIGURE 16-16: WDT TIMER TIME-OUT PERIOD vs. VDD<sup>(1)</sup>

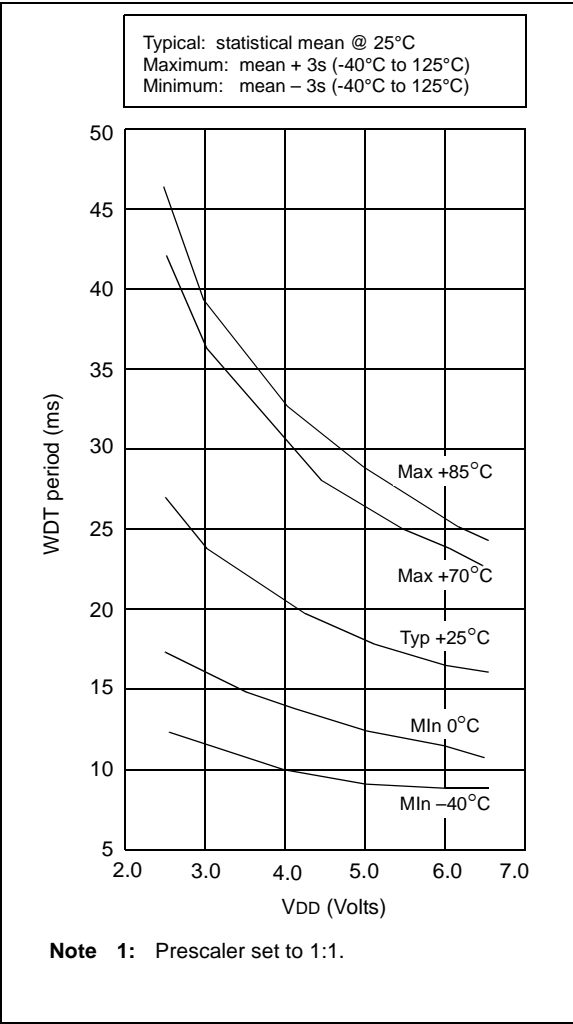
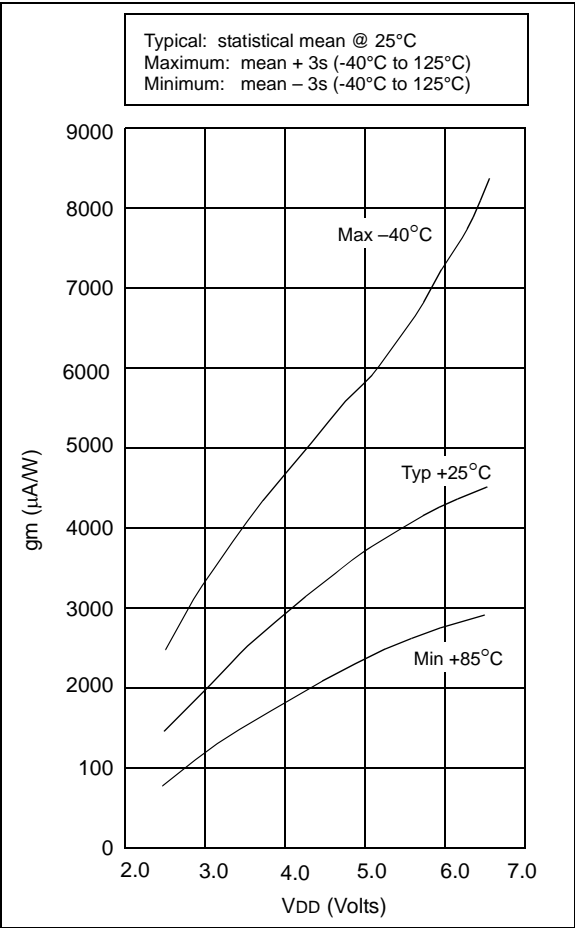


FIGURE 16-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD





## 17.0 ELECTRICAL CHARACTERISTICS - PIC16LC54A

### Absolute Maximum Ratings<sup>(†)</sup>

Ambient temperature under bias .....	–55°C to +125°C
Storage temperature .....	–65°C to +150°C
Voltage on VDD with respect to VSS .....	0 to +7.5V
Voltage on MCLR with respect to VSS.....	0 to +14V
Voltage on all other pins with respect to VSS .....	–0.6V to (VDD + 0.6V)
Total power dissipation <sup>(1)</sup> .....	800 mW
Max. current out of VSS pin .....	150 mA
Max. current into VDD pin .....	100 mA
Max. current into an input pin (T0CKI only) .....	±500 µA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > VDD).....	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > VDD) .....	±20 mA
Max. output current sunk by any I/O pin .....	25 mA
Max. output current sourced by any I/O pin .....	20 mA
Max. output current sourced by a single I/O (Port A, B or C) .....	50 mA
Max. output current sunk by a single I/O (Port A, B or C).....	50 mA

**Note 1:** Power dissipation is calculated as follows:  $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# PIC16C5X

## 17.3 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial, Extended) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial, Extended) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	V <sub>IL</sub>	<b>Input Low Voltage</b> I/O Ports I/O Ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	V <sub>SS</sub> V <sub>SS</sub> V <sub>SS</sub> V <sub>SS</sub> V <sub>SS</sub> V <sub>SS</sub>	— — — — — —	0.8 V 0.15 V <sub>DD</sub> 0.15 V <sub>DD</sub> 0.15 V <sub>DD</sub> 0.15 V <sub>DD</sub> 0.3 V <sub>DD</sub>	V V V V V V	4.5V < V <sub>DD</sub> ≤ 5.5V Otherwise  RC mode only <sup>(3)</sup> XT, HS and LP modes
D040	V <sub>IH</sub>	<b>Input High Voltage</b> I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	2.0 0.25 V <sub>DD</sub> +0.8 0.85 V <sub>DD</sub> 0.85 V <sub>DD</sub> 0.85 V <sub>DD</sub> 0.7 V <sub>DD</sub>	— — — — — —	V <sub>DD</sub> V <sub>DD</sub> V <sub>DD</sub> V <sub>DD</sub> V <sub>DD</sub> V <sub>DD</sub>	V V V V V V	4.5V < V <sub>DD</sub> ≤ 5.5V Otherwise  RC mode only <sup>(3)</sup> XT, HS and LP modes
D050	V <sub>HYS</sub>	<b>Hysteresis of Schmitt Trigger inputs</b>	0.15 V <sub>DD</sub> *	—	—	V	
D060	I <sub>IL</sub>	<b>Input Leakage Current<sup>(1,2)</sup></b> I/O ports  MCLR MCLR T0CKI OSC1	-1.0  -5.0  -3.0 -3.0	0.5  — 0.5 0.5 0.5	+1.0  +5.0 +3.0 +3.0 —	μA  μA μA μA μA	<b>For V<sub>DD</sub> ≤ 5.5V:</b> V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , pin at hi-impedance V <sub>PIN</sub> = V <sub>SS</sub> +0.25V V <sub>PIN</sub> = V <sub>DD</sub> V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , XT, HS and LP modes
D080	V <sub>OL</sub>	<b>Output Low Voltage</b> I/O ports OSC2/CLKOUT	— —	— —	0.6 0.6	V V	I <sub>OL</sub> = 8.7 mA, V <sub>DD</sub> = 4.5V I <sub>OL</sub> = 1.6 mA, V <sub>DD</sub> = 4.5V, RC mode only
D090	V <sub>OH</sub>	<b>Output High Voltage<sup>(2)</sup></b> I/O ports OSC2/CLKOUT	V <sub>DD</sub> - 0.7 V <sub>DD</sub> - 0.7	— —	— —	V V	I <sub>OH</sub> = -5.4 mA, V <sub>DD</sub> = 4.5V I <sub>OH</sub> = -1.0 mA, V <sub>DD</sub> = 4.5V, RC mode only

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

# PIC16C5X

FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF, 25°C

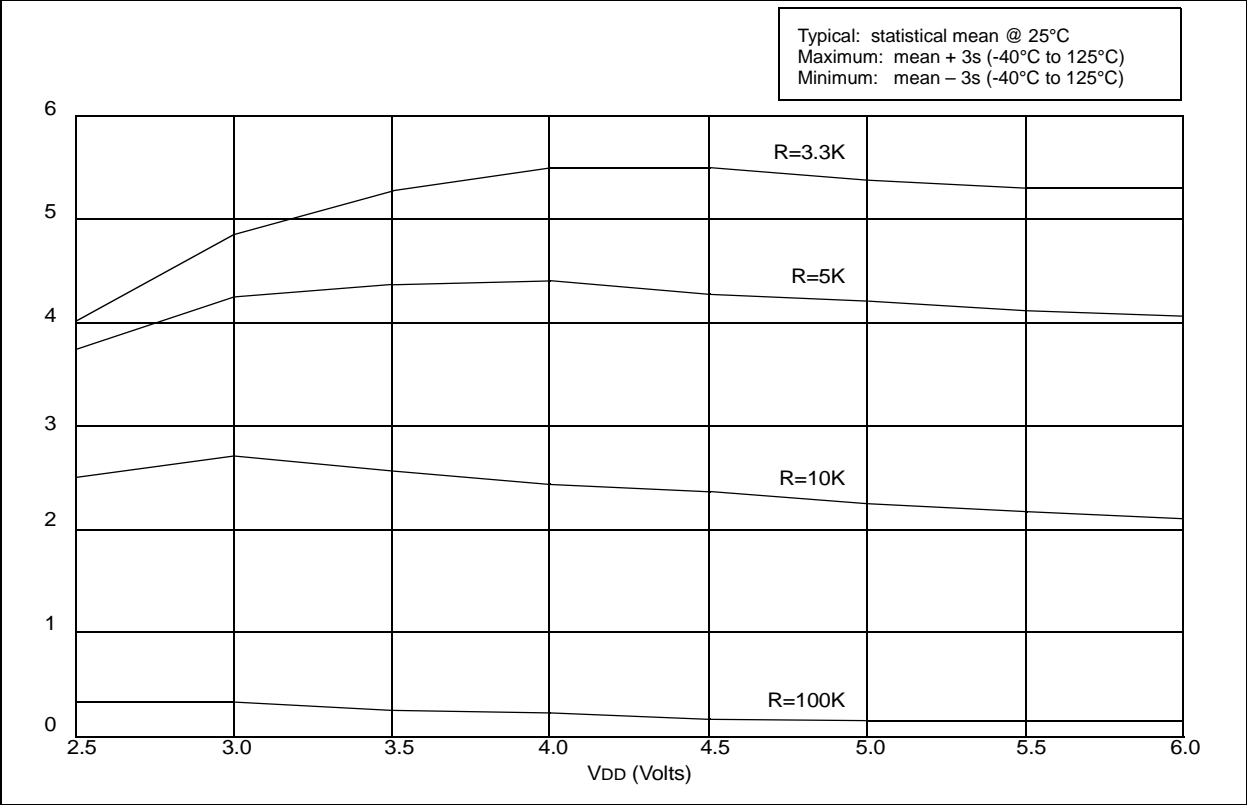
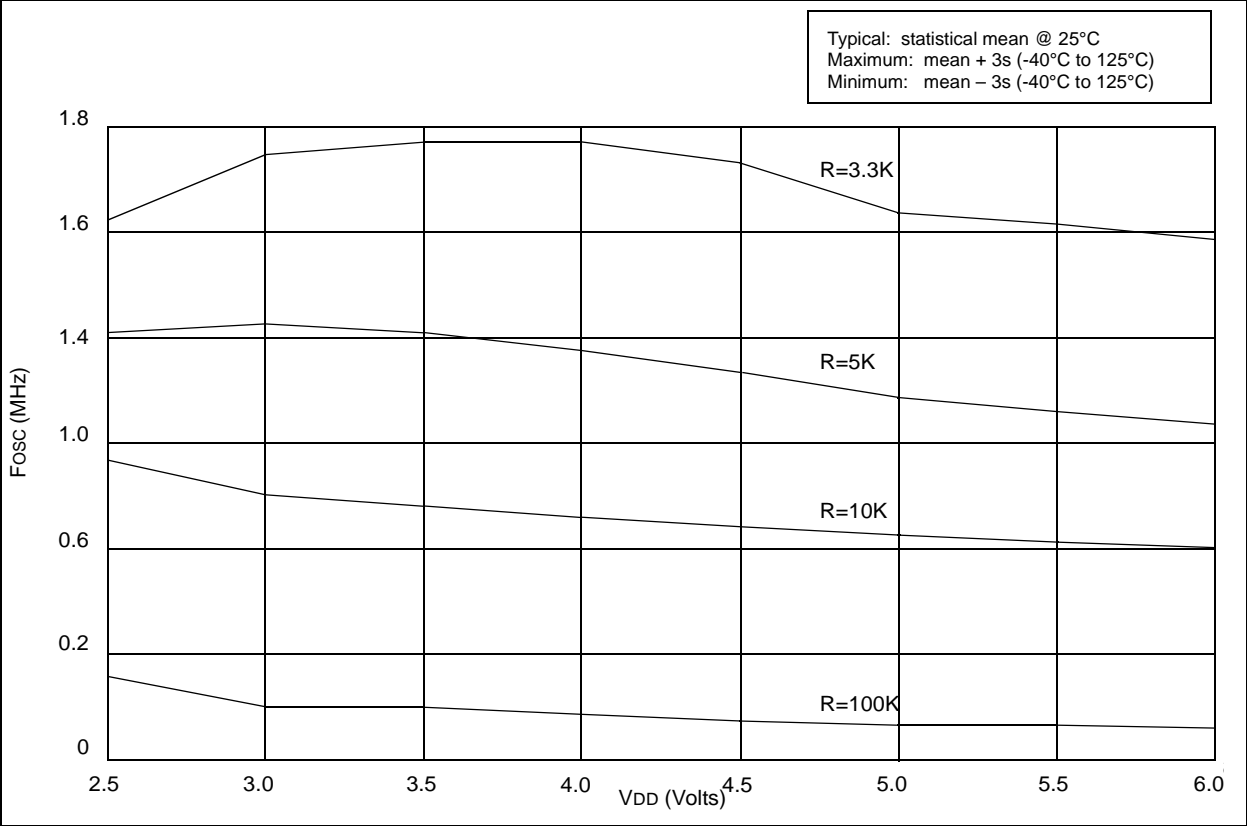
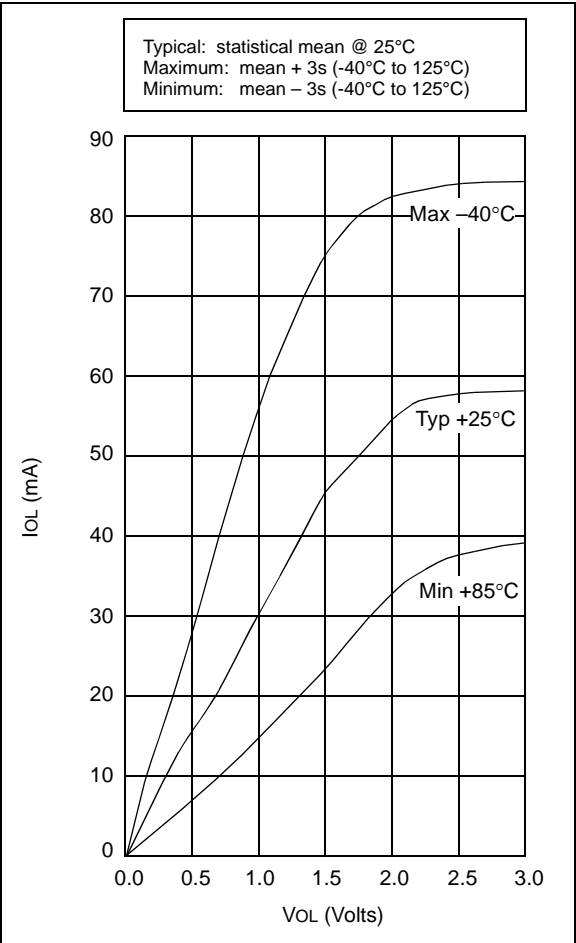


FIGURE 18-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF, 25°C



# PIC16C5X

**FIGURE 18-18:    PORTA, B AND C IoL vs.  
VOL, VDD = 5 V**

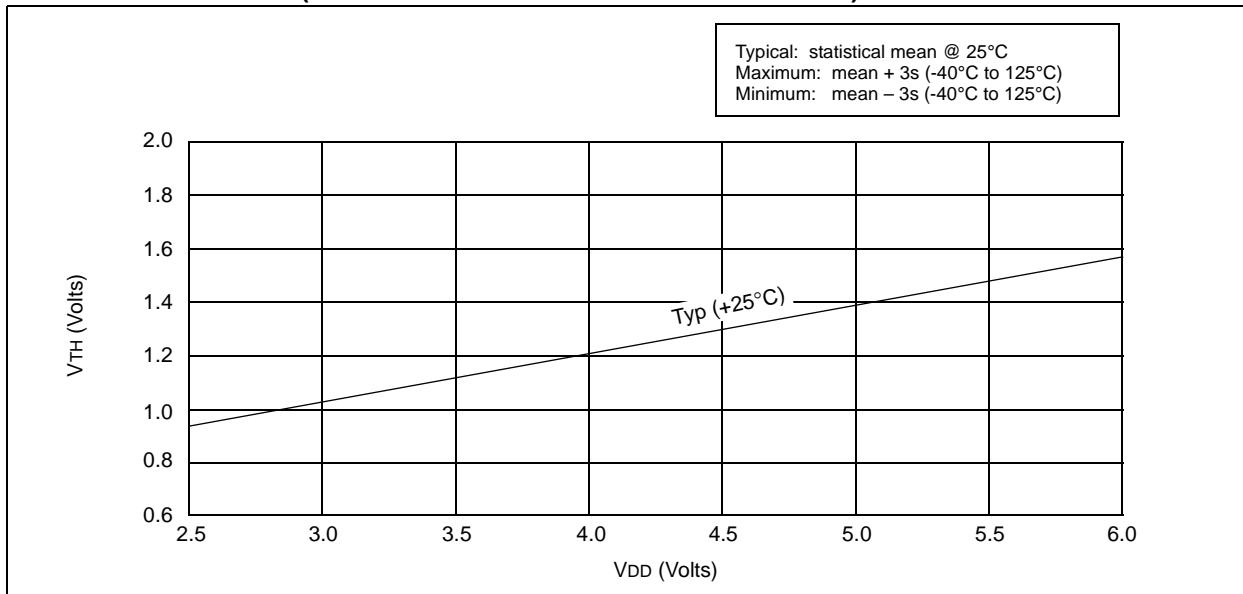


**TABLE 18-2:    INPUT CAPACITANCE**

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
MCLR	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

**FIGURE 20-4:  $V_{TH}$  (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs.  $V_{DD}$**



**FIGURE 20-5:  $V_{TH}$  (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (HS MODE) vs.  $V_{DD}$**

