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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c55a-20i-so

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### 7.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., MOVF PORTB, W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

### 7.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used (RA<3:0>). Bits 7-4 are unimplemented and read as '0's.

### 7.2 PORTB

PORTB is an 8-bit I/O Register (PORTB<7:0>).

### 7.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16CR56, PIC16CR56, PIC16CS8 and PIC16CR58.

### 7.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the TRIS f instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

Note:	A read of the ports reads the pins, not the						
	output data latches. That is, if an output						
	driver on a pin is enabled and driven high,						
	but the external system is holding it low, a						
	read of the port will indicate that the pin is						
	low.						

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

TABLE 7-1:	SUMMARY O	F PORT	REGISTERS
			LOIOI LIVO

#### Value on Value on Bit 4 Bit 3 Bit 1 Bit 0 MCLR and Address Name Bit 7 Bit 6 Bit 5 Bit 2 Power-On Reset WDT Reset TRIS N/A I/O Control Registers (TRISA, TRISB, TRISC) 1111 1111 1111 1111 05h PORTA RA3 RA2 RA1 RA0 \_ \_ \_ \_ xxxx \_ \_ \_ \_ uuuu PORTB 06h RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0 XXXX XXXX uuuu uuuu 07h PORTC RC7 RC6 RC5 RC4 RC3 RC2 RC1 RC0 XXXX XXXX uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'

### 7.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 7-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

#### FIGURE 7-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



### 7.6 I/O Programming Considerations

#### 7.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 7-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

### EXAMPLE 7-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;

;				PORT	latch	PORT	pins
;							
	BCF	PORTB,	7	;01pp	pppp	11pp	pppp
	BCF	PORTB,	6	;10pp	pppp	11pp	pppp
	MOVLW	H'3F'		;			
	TRIS	PORTB		;10pp	pppp	10pp	pppp
;							

;Note that the user may have expected the pin ;values to be 00pp pppp. The 2nd BCF caused ;RB7 to be latched as the pin value (High).

## 7.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 7-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.



### FIGURE 7-2: SUCCESSIVE I/O OPERATION

### 9.1 Configuration Bits

Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. Nine bits are code protection bits for the PIC16C54A, PIC16CR54A, PIC16CF54A, PIC16C55A, PIC16CF56A, PIC16CF56A, PIC16CF57C, PIC16CR57C,

PIC16C58B, and PIC16CR58B devices (Register 9-1). One bit is for code protection for the PIC16C54, PIC16C55, PIC16C56 and PIC16C57 devices (Register 9-2).

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" diagrams in the back of this data sheet).

### REGISTER 9-1: CONFIGURATION WORD FOR PIC16C54A/CR54A/C54C/CR54C/C55A/C56A/ CR56A/C57C/CR57C/C58B/CR58B

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0
bit 11											bit 0

bit 11-3: CP: Code Protection Bit

- 1 = Code protection off
  - 0 =Code protection on
- bit 2: WDTE: Watchdog timer enable bit
  - 1 = WDT enabled
  - 0 = WDT disabled

#### bit 1-0: FOSC1:FOSC0: Oscillator Selection Bit

- 00 = LP oscillator
- 01 = XT oscillator
- 10 = HS oscillator
- 11 = RC oscillator

## **Note 1:** Refer to the PIC16C5X Programming Specification (Literature Number DS30190) to determine how to access the configuration word.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

# PIC16C5X

RLF	Rotate Left f through Carry								
Syntax:	[label] RLF f,d								
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$								
Operation:	See description below								
Status Affected:	С								
Encoding:	0011	. 01	df	ffff					
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.								
Words:	1								
Cycles:	1								
Example:	RLF	REG	£1,0						
Before Instru REG1 C After Instruct	ction = = ion	1110 0	0110	0					
REG1	=	1110	0110	C					
W	=	1100	1100	C					
С	=	1							

RRF	Rotate Right f through Carry								
Syntax:	[label] RRF f,d								
Operands:	$\begin{array}{l} 0\leq f\leq 31\\ d\in [0,1] \end{array}$								
Operation:	See description below								
Status Affected:	С								
Encoding:	0011 00df ffff								
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.								
Words:	1								
Cycles:	1								
Example:	RRF REG1,0								
Before Instru REG1 C	uction = 1110 0110 = 0								
REG1	= 1110 0110								
W C	= 0111 0011 = 0								

SLEEP	Enter SLEEP Mode						
Syntax:	[label]	SLEEP					
Operands:	None						
Operation:	$\begin{array}{l} 00h \rightarrow WDT; \\ 0 \rightarrow WDT \ prescaler; \ if \ assigned \\ 1 \rightarrow \overline{TO}; \\ 0 \rightarrow \overline{PD} \end{array}$						
Status Affected:	TO, PD						
Encoding:	0000 0000 0011						
Description:	Time-out status bit (TO) is set. The power-down status bit (PD) is cleared. The WDT and its pres- caler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more						
Words:	1						
Cycles:	1						
Example:	SLEEP						

NOTES:



### TABLE 12-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54/55/56/57

AC Char	acteristics	$\begin{array}{ll} Standard Operating Conditions (unless of the conditions of the conditions (unless of the conditions of the conditions (unless of the conditions of the condition$	ndard Operating Conditions (unless otherwise specified)						
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units			
10	TosH2ckL	OSC1↑ to CLKOUT↓ <sup>(1)</sup>	—	15	30**	ns			
11	TosH2ckH	OSC1↑ to CLKOUT↑ <sup>(1)</sup>	—	15	30**	ns			
12	TckR	CLKOUT rise time <sup>(1)</sup>	—	5.0	15**	ns			
13	TckF	CLKOUT fall time <sup>(1)</sup>	—	5.0	15**	ns			
14	TckL2ioV	CLKOUT↓ to Port out valid <sup>(1)</sup>	—	_	40**	ns			
15	TioV2ckH	Port in valid before CLKOUT <sup>(1)</sup>	0.25 TCY+30*	_	—	ns			
16	TckH2iol	Port in hold after CLKOUT <sup>(1)</sup>	0*	_	—	ns			
17	TosH2ioV	OSC1 <sup>↑</sup> (Q1 cycle) to Port out valid <sup>(2)</sup>	—	_	100*	ns			
18	TosH2iol	OSC1 <sup>↑</sup> (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns			
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns			
20	TioR	Port output rise time <sup>(2)</sup>	—	10	25**	ns			
21	TioF	Port output fall time <sup>(2)</sup>	_	10	25**	ns			

\* These parameters are characterized but not tested.

\*\* These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Please refer to Figure 12-1 for load conditions.

### 13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 PIC16LCR54A-04I (Commercial, Industrial)				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
PIC16CR54A-04, 10, 20 PIC16CR54A-04I, 10I, 20I (Commercial, Industrial)			Standa Operat	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$					
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions		
	Vdd	Supply Voltage							
D001		PIC16LCR54A	2.0		6.25	V			
D001 D001A		PIC16CR54A	2.5 4.5		6.25 5.5	V V	RC and XT modes HS mode		
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>		1.5*	_	V	Device in SLEEP mode		
D003	Vpor	VDD Start Voltage to ensure Power-on Reset	_	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	Svdd	VDD Rise Rate to ensure Power-on Reset	0.05*		—	V/ms	See Section 5.1 for details on Power-on Reset		
	IDD	Supply Current <sup>(2)</sup>							
D005		PICLCR54A	—	10	20 70	μA μA	Fosc = 32 kHz, VDD = 2.0V Fosc = 32 kHz, VDD = 6.0V		
D005A		PIC16CR54A		2.0 0.8 90 4.8	3.6 1.8 350 10	mA mA μA	RC <sup>(3)</sup> and XT modes: Fosc = 4.0 MHz, VDD = 6.0V Fosc = 4.0 MHz, VDD = 3.0V Fosc = 200 kHz, VDD = 2.5V HS mode: Fosc = 10 MHz, VDD = 5.5V		
			—	9.0	20	mA	FOSC = 20  MHz,  VDD = 5.5  V		

Legend: Rows with standard voltage device data only are shaded for improved readability.

- \* These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

- 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
  - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
  - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k $\Omega$ .

#### FIGURE 14-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED



## FIGURE 14-7: TYPICA

#### TYPICAL IPD vs. VDD, WATCHDOG ENABLED



#### FIGURE 14-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED



IPD, with WDT enabled, has two components: The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At  $-40^{\circ}$ C, the latter dominates explaining the apparently anomalous behavior.

### 15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04 PIC16LC54A-04I (Commercial, Industrial)				$\begin{array}{ l l l l l l l l l l l l l l l l l l l$					
PIC16C54A-04, 10, 20 PIC16C54A-04I, 10I, 20I (Commercial, Industrial)			<b>Stand</b> Opera	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^\circ C \leq T A \leq +70^\circ C \mbox{ for commercial} \\ -40^\circ C \leq T A \leq +85^\circ C \mbox{ for industrial} \end{array}$					
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions		
	Vdd	Supply Voltage							
D001		PIC16LC54A	3.0 2.5	_	6.25 6.25	V V	XT and RC modes LP mode		
D001A		PIC16C54A	3.0 4.5	_	6.25 5.5	V V	RC, XT and LP modes HS mode		
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	—	1.5*	—	V	Device in SLEEP mode		
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	-	V/ms	See Section 5.1 for details on Power-on Reset		
	IDD	Supply Current <sup>(2)</sup>							
D005		PIC16LC5X	_	0.5	2.5	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC <sup>(3)</sup> and XT modes		
				11	27	μΑ	Fosc = 32 kHz, VDD = 2.5V, WDT disabled, LP mode, Commercial		
			_	11	35	μΑ	Fosc = 32 kHz, VDD = 2.5V, WDT disabled, LP mode, Industrial		
D005A		PIC16C5X	—	1.8	2.4	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC <sup>(3)</sup> and XT modes		
			—	2.4	8.0	mA	FOSC = 10 MHz, VDD = 5.5V, HS mode		
			—	4.5	16	mA	FOSC = 20  MHz,  VDD = 5.5V, HS mode		
				14	29	μA	HOSC = 32 kHz, VDD = 3.0V,		
			-	17	37	μΑ	Fosc = 32 kHz, VDD = 3.0V, WDT disabled, LP mode, Industrial		

Legend: Rows with standard voltage device data only are shaded for improved readability.

These parameters are characterized but not tested.

- † Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- **Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
  - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
    - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
    - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
  - 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k $\Omega$ .



### TABLE 15-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54A

	Standard Operating Conditions (unless otherwise specified)									
		Operating Temperat	ture $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial							
	AC Chara	acteristics	-40°C ≤	$TA \le +8$	85°C fo	or indus	trial			
			–20°C ≤	$TA \leq +8$	85°C fo	or indus	trial - PIC16LV54A-02I			
			-40°C ≤	TA ≤ +1	25°C	for exte	nded			
Param No.	Symbol	Characteristic	Тур†	Max	Units	Conditions				
40	Tt0H	T0CKI High Pulse Width								
		- No Prescaler	0.5 TCY + 20*	—	—	ns				
		- With Prescaler	10*			ns				
41	Tt0L	T0CKI Low Pulse Width								
		- No Prescaler	0.5 TCY + 20*	—	—	ns				
		- With Prescaler	10*			ns				
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> *	_	_	ns	Whichever is greater.			
			N				N = Prescale Value			
							(1, 2, 4,, 256)			

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.







### TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Chara	cteristics	$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for extended} \\ \end{array} $							
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions		
2	Тсу	Instruction Cycle Time <sup>(2)</sup>	—	4/Fosc					
3	TosL, TosH	Clock in (OSC1) Low or High			_	ns	XT oscillator		
		Time	20*	—	_	ns	HS oscillator		
			2.0*	—	_	μS	LP oscillator		
4	TosR, TosF Clock in (OSC1) Rise or Fall		-		25*	ns	XT oscillator		
		Time		—	25*	ns	HS oscillator		
			—	—	50*	ns	LP oscillator		

- \* These parameters are characterized but not tested.
- † Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- **Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

### 18.0 DEVICE CHARACTERIZATION - PIC16LC54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean +  $3\sigma$ ) or (mean -  $3\sigma$ ) respectively, where  $\sigma$  is a standard deviation, over the whole temperature range.



FIGURE 18-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

### TABLE 18-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Average Fosc @ 5V, 25°C		
20 pF	3.3K	5 MHz	± 27%	
	5K	3.8 MHz	± 21%	
	10K	2.2 MHz	± 21%	
	100K	262 kHz	± 31%	
100 pF	3.3K	1.63 MHz	± 13%	
	5K	1.2 MHz	± 13%	
	10K	684 kHz	± 18%	
	100K	71 kHz	± 25%	
300 pF	3.3K	660 kHz	± 10%	
	5.0K	484 kHz	± 14%	
	10K	267 kHz	± 15%	
	100K	29 kHz	± 19%	

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is  $\pm 3$  standard deviation from average value for VDD = 5V.









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### 19.0 ELECTRICAL CHARACTERISTICS - PIC16LC54C 40MHz

### Absolute Maximum Ratings<sup>(†)</sup>

Ambient temperature under bias	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	–0.6V to (VDD + 0.6V)
Total power dissipation <sup>(1)</sup>	
Max. current out of Vss pin	
Max. current into Vod pin	
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, IIK (VI < 0 or VI > VDD)	±20 mA
Output clamp current, Iок (Vo < 0 or Vo > Voo)	±20 mA
Max. output current sunk by any I/O pin	
Max. output current sourced by any I/O pin	
Max. output current sourced by a single I/O (Port A, B or C)	
Max. output current sunk by a single I/O (Port A, B or C)	
<b>Note 1:</b> Power dissipation is calculated as follows: Pdis = VDD x {IDD - $\sum$ IOH} + $\sum$ {(VI	DD-VOH) x IOH} + $\Sigma$ (VOL x IOL)

**†** NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### 21.0 PACKAGING INFORMATION

### 21.1 Package Marketing Information

### 18-Lead PDIP



### 28-Lead Skinny PDIP (.300")



### 28-Lead PDIP (.600")



### 18-Lead SOIC



### 28-Lead SOIC



### 20-Lead SSOP



### 28-Lead SSOP





### Example



### Example



### Example



### Example



### Example



### Example



### 28-Lead Plastic Dual In-line (P) - 600 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28	
Pitch	р		.100			2.54	
Top to Seating Plane	А	.160	.175	.190	4.06	4.45	4.83
Molded Package Thickness	A2	.140	.150	.160	3.56	3.81	4.06
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88
Molded Package Width	E1	.505	.545	.560	12.83	13.84	14.22
Overall Length	D	1.395	1.430	1.465	35.43	36.32	37.21
Tip to Seating Plane	L	.120	.130	.135	3.05	3.30	3.43
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.030	.050	.070	0.76	1.27	1.78
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.620	.650	.680	15.75	16.51	17.27
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-011 Drawing No. C04-079

### 18-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	р		.050			1.27	
Overall Height	Α	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	С	.009	.011	.012	0.23	0.27	0.30
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013 Drawing No. C04-051

### 20-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES*		N	<b>IILLIMETERS</b>	6
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	р		.026			0.65	
Overall Height	Α	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	Е	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25
Foot Angle	φ	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-150 Drawing No. C04-072

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