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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c55a-20i-ss

PIC16C5X

NOTES:

4.0 OSCILLATOR CONFIGURATIONS

4.1 Oscillator Types

PIC16C5Xs can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

1. LP: Low Power Crystal
2. XT: Crystal/Resonator
3. HS: High Speed Crystal/Resonator
4. RC: Resistor/Capacitor

Note: Not all oscillator selections available for all parts. See Section 9.1.

4.2 Crystal Oscillator/Ceramic Resonators

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 4-1). The PIC16C5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 4-2).

FIGURE 4-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)

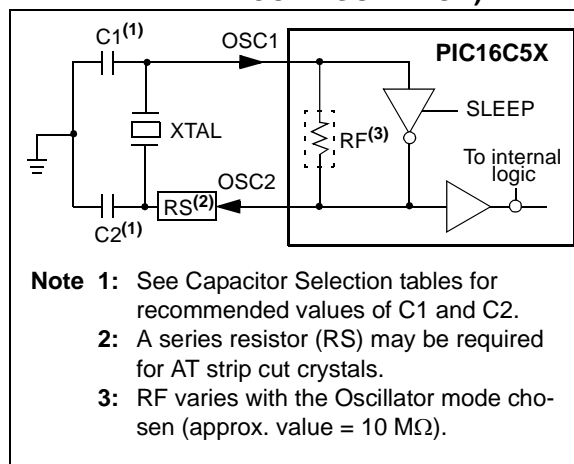


FIGURE 4-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

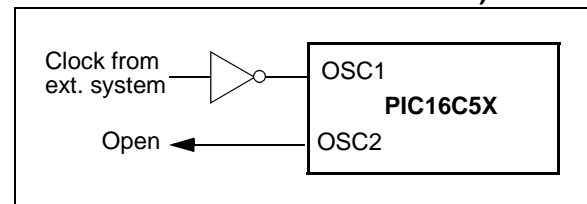


TABLE 4-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC16C5X, PIC16CR5X

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	68-100 pF	68-100 pF
	2.0 MHz	15-33 pF	15-33 pF
	4.0 MHz	10-22 pF	10-22 pF
HS	8.0 MHz	10-22 pF	10-22 pF
	16.0 MHz	10 pF	10 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 4-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC16C5X, PIC16CR5X

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz ⁽¹⁾	15 pF	15 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Note 1: For VDD > 4.5V, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

Note: If you change from this device to another device, please verify oscillator characteristics in your application.

PIC16C5X

6.5.1 PAGING CONSIDERATIONS – PIC16C56/CR56, PIC16C57/CR57 AND PIC16C58/CR58

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS Register will not be updated. Therefore, the next `GOTO`, `CALL` or modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA<1:0>).

For example, a `NOP` at location 1FFh (page 0) increments the PC to 200h (page 1). A `GOTO xxx` at 200h will return the program to address xxh on page 0 (assuming that PA<1:0> are clear).

To prevent this, the page preselect bits must be updated under program control.

6.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the RESET vector).

The STATUS Register page preselect bits are cleared upon a RESET, which means that page 0 is preselected.

Therefore, upon a RESET, a `GOTO` instruction at the RESET vector location will automatically cause the program to jump to page 0.

6.6 Stack

PIC16C5X devices have a 10-bit or 11-bit wide, two-level hardware push/pop stack.

A `CALL` instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential `CALL`'s are executed, only the most recent two return addresses are stored.

A `RETLW` instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential `RETLW`'s are executed, the stack will be filled with the address previously stored in level 2. Note that the W Register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the `RETLW` instruction, the PC is loaded with the Top of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC, therefore, paging is not an issue when returning from a subroutine.

PIC16C5X

NOTES:

10.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 10-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers in that bank is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 10-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x1F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
TO	Time-out bit
PD	Power-down bit
dest	Destination, either the W register or the specified register file location
[]	Options
()	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
<i>italics</i>	User defined term (font is courier)

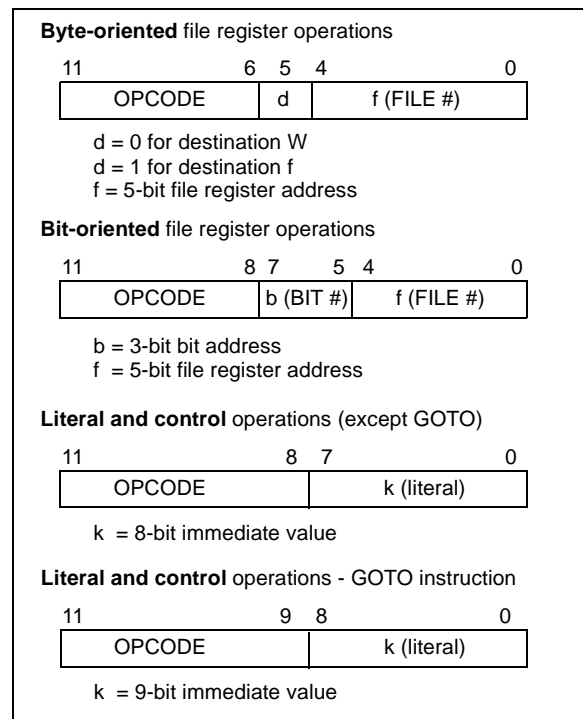
All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time would be 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time would be 2 μs.

Figure 10-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS



PIC16C5X

12.5 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	V _{IL}	Input Low Voltage					
		I/O ports	V _{SS}	—	0.15 V _{DD}	V	Pin at hi-impedance
		MCLR (Schmitt Trigger)	V _{SS}	—	0.15 V _{DD}	V	
		T0CKI (Schmitt Trigger)	V _{SS}	—	0.15 V _{DD}	V	
		OSC1 (Schmitt Trigger)	V _{SS}	—	0.15 V _{DD}	V	PIC16C5X-RC only ⁽³⁾
		OSC1 (Schmitt Trigger)	V _{SS}	—	0.3 V _{DD}	V	PIC16C5X-XT, 10, HS, LP
D040	V _{IH}	Input High Voltage					
		I/O ports	0.45 V _{DD}	—	V _{DD}	V	For all V _{DD} ⁽⁴⁾
		I/O ports	2.0	—	V _{DD}	V	4.0V < V _{DD} ≤ 5.5V ⁽⁴⁾
		I/O ports	0.36 V _{DD}	—	V _{DD}	V	V _{DD} > 5.5 V
		MCLR (Schmitt Trigger)	0.85 V _{DD}	—	V _{DD}	V	
		T0CKI (Schmitt Trigger)	0.85 V _{DD}	—	V _{DD}	V	
		OSC1 (Schmitt Trigger)	0.85 V _{DD}	—	V _{DD}	V	PIC16C5X-RC only ⁽³⁾
		OSC1 (Schmitt Trigger)	0.7 V _{DD}	—	V _{DD}	V	PIC16C5X-XT, 10, HS, LP
D050	V _{HYS}	Hysteresis of Schmitt Trigger inputs	0.15 V _{DD} *	—	—	V	
D060	I _{IL}	Input Leakage Current ^(1,2)					For V_{DD} ≤ 5.5 V:
		I/O ports	−1	0.5	+1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance
		MCLR	−5	—	—	μA	V _{PIN} = V _{SS} + 0.25V
		MCLR	—	0.5	+5	μA	V _{PIN} = V _{DD}
		T0CKI	−3	0.5	+3	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD}
		OSC1	−3	0.5	+3	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , PIC16C5X-XT, 10, HS, LP
D080	V _{OL}	Output Low Voltage					
		I/O ports	—	—	0.6	V	I _{OL} = 8.7 mA, V _{DD} = 4.5V
		OSC2/CLKOUT	—	—	0.6	V	I _{OL} = 1.6 mA, V _{DD} = 4.5V, PIC16C5X-RC
D090	V _{OH}	Output High Voltage ⁽²⁾					
		I/O ports	V _{DD} − 0.7	—	—	V	I _{OH} = −5.4 mA, V _{DD} = 4.5V
		OSC2/CLKOUT	V _{DD} − 0.7	—	—	V	I _{OH} = −1.0 mA, V _{DD} = 4.5V, PIC16C5X-RC

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 PIC16LCR54A-04I (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
PIC16CR54A-04, 10, 20 PIC16CR54A-04I, 10I, 20I (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
	IPD	Power-down Current⁽²⁾					
D006		PIC16LCR54A-Commercial	—	1.0	6.0	μA	V _{DD} = 2.5V, WDT disabled
			—	2.0	8.0*	μA	V _{DD} = 4.0V, WDT disabled
			—	3.0	15	μA	V _{DD} = 6.0V, WDT disabled
			—	5.0	25	μA	V _{DD} = 6.0V, WDT enabled
D006A		PIC16CR54A-Commercial	—	1.0	6.0	μA	V _{DD} = 2.5V, WDT disabled
			—	2.0	8.0*	μA	V _{DD} = 4.0V, WDT disabled
			—	3.0	15	μA	V _{DD} = 6.0V, WDT disabled
			—	5.0	25	μA	V _{DD} = 6.0V, WDT enabled
D007		PIC16LCR54A-Industrial	—	1.0	8.0	μA	V _{DD} = 2.5V, WDT disabled
			—	2.0	10*	μA	V _{DD} = 4.0V, WDT disabled
			—	3.0	20*	μA	V _{DD} = 4.0V, WDT enabled
			—	3.0	18	μA	V _{DD} = 6.0V, WDT disabled
			—	5.0	45	μA	V _{DD} = 6.0V, WDT enabled
D007A		PIC16CR54A-Industrial	—	1.0	8.0	μA	V _{DD} = 2.5V, WDT disabled
			—	2.0	10*	μA	V _{DD} = 4.0V, WDT disabled
			—	3.0	20*	μA	V _{DD} = 4.0V, WDT enabled
			—	3.0	18	μA	V _{DD} = 6.0V, WDT disabled
			—	5.0	45	μA	V _{DD} = 6.0V, WDT enabled

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all I_{DD} measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS}, T_{0CKI} = V_{DD}, MCLR = V_{DD}; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through R_{EXT}. The current through the resistor can be estimated by the formula: I_R = V_{DD}/2R_{EXT} (mA) with R_{EXT} in kΩ.

FIGURE 16-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF, 25°C

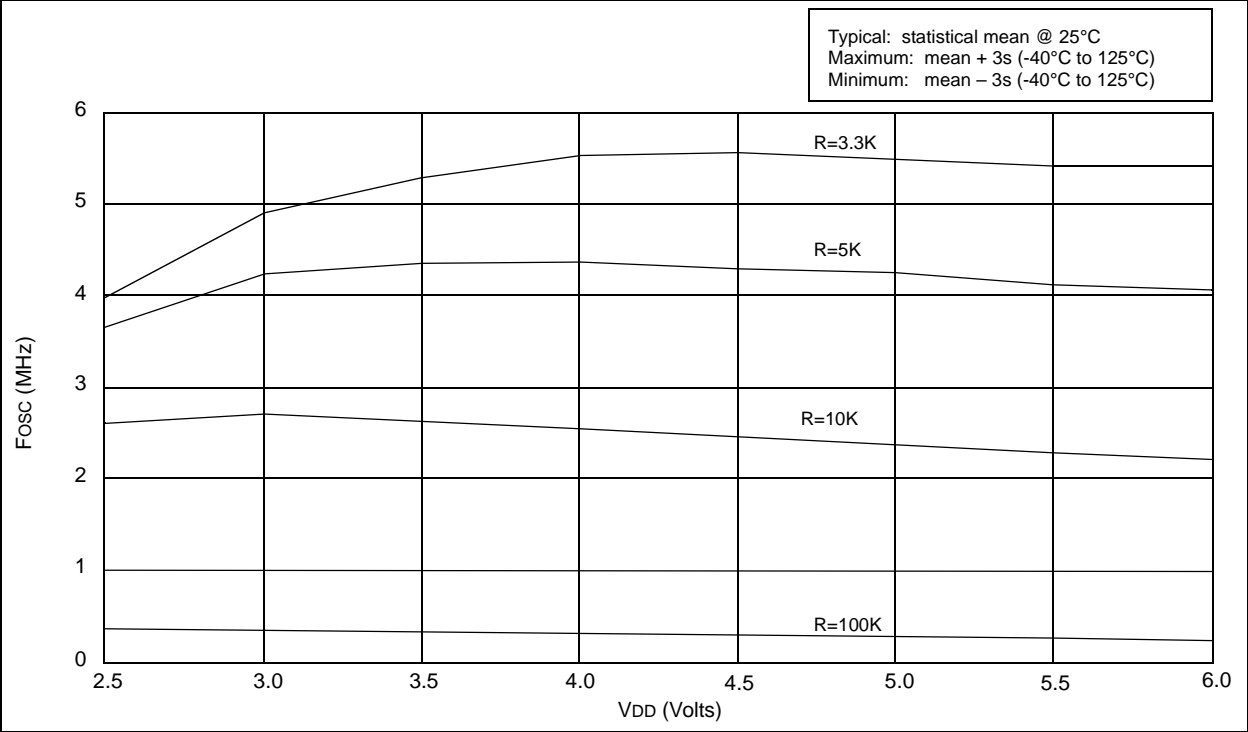


FIGURE 16-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF, 25°C

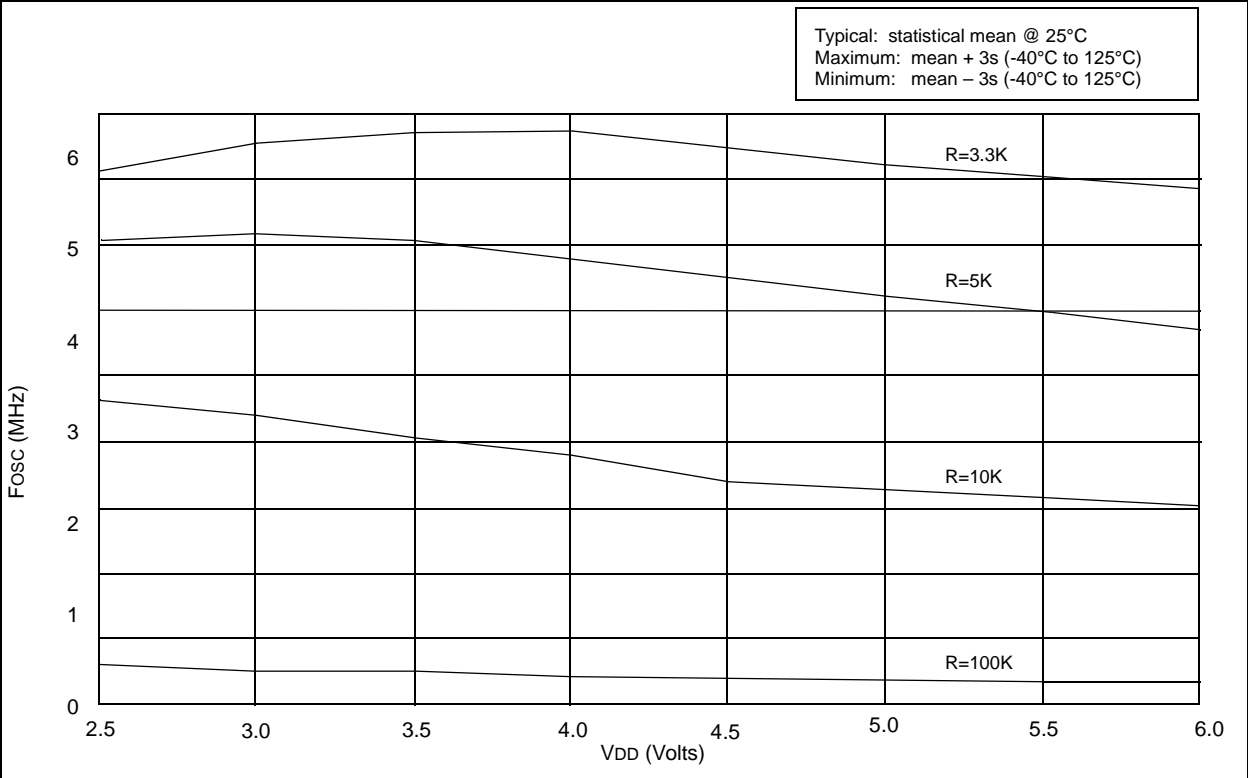


FIGURE 16-16: WDT TIMER TIME-OUT PERIOD vs. VDD⁽¹⁾

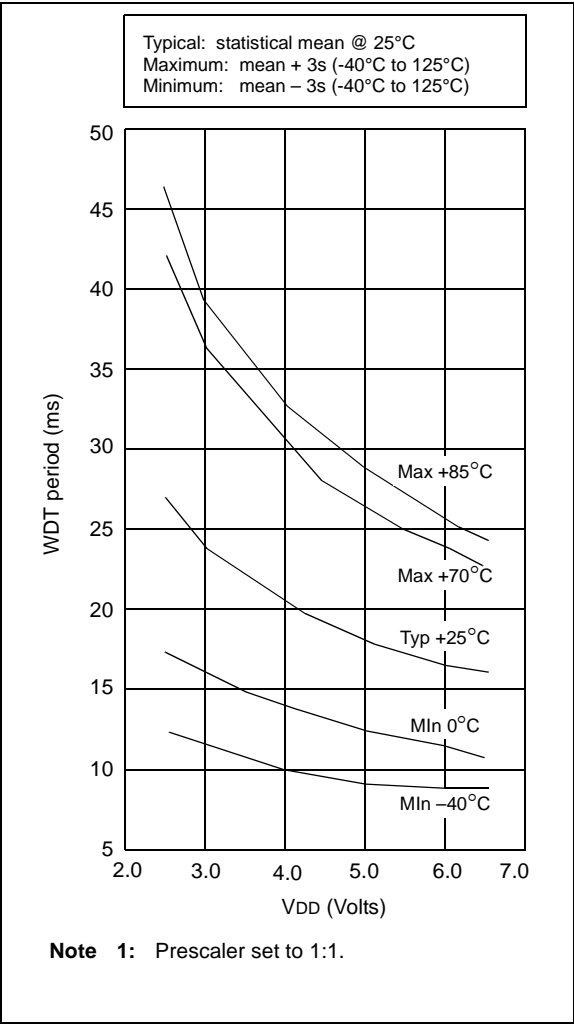
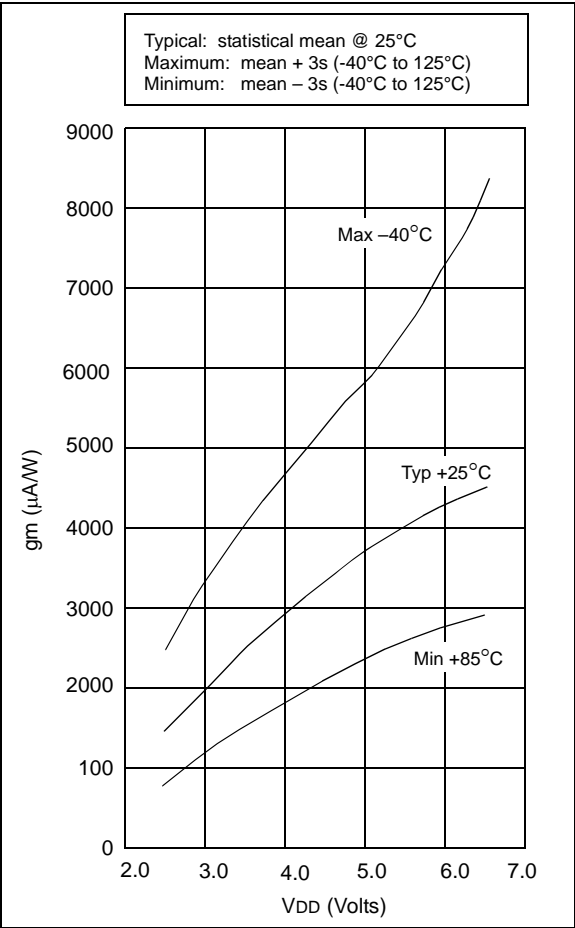


FIGURE 16-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD



PIC16C5X

NOTES:

17.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended) PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)				Standard Operating Conditions (unless otherwise specified)			
				Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended			
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	3.0 4.5	— —	5.5 5.5	V V	RC, XT, LP, and HS mode from 0 - 10 MHz from 10 - 20 MHz
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current ⁽²⁾ XT and RC ⁽³⁾ modes HS mode	— —	1.8 9.0	3.3 20	mA mA	FOSC = 4.0 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V
D020	IPD	Power-down Current ⁽²⁾	— — — — — —	0.3 10 12 4.8 18 26	17 50* 60* 31* 68* 90*	μA μA μA μA μA μA	VDD = 3.0V, WDT disabled VDD = 4.5V, WDT disabled VDD = 5.5V, WDT disabled VDD = 3.0V, WDT enabled VDD = 4.5V, WDT enabled VDD = 5.5V, WDT enabled

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{EXT}$ (mA) with REXT in kΩ.

FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. V_{DD} , $C_{EXT} = 300$ pF, 25°C

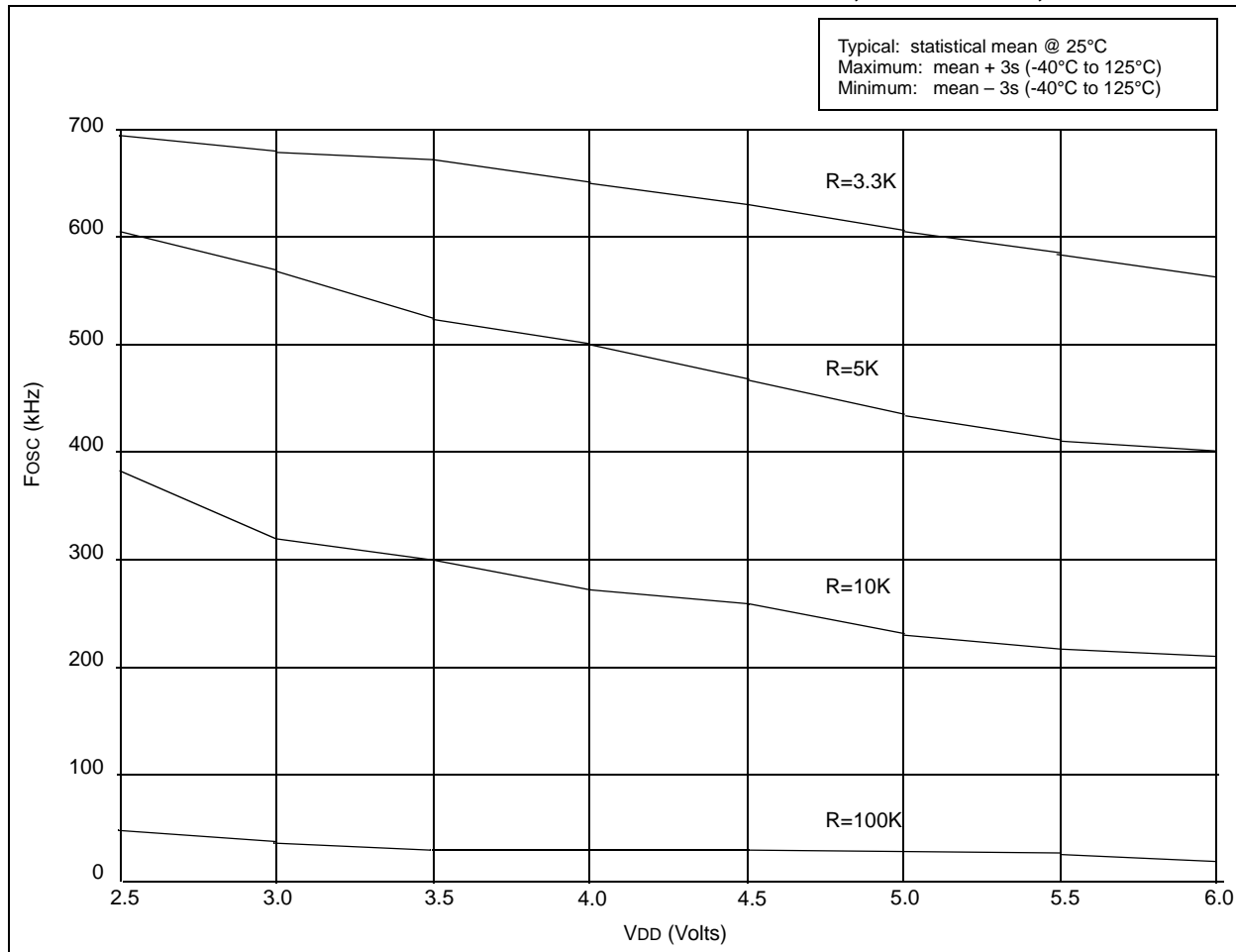


FIGURE 18-5: TYPICAL I_{PD} vs. V_{DD} , WATCHDOG DISABLED (25°C)

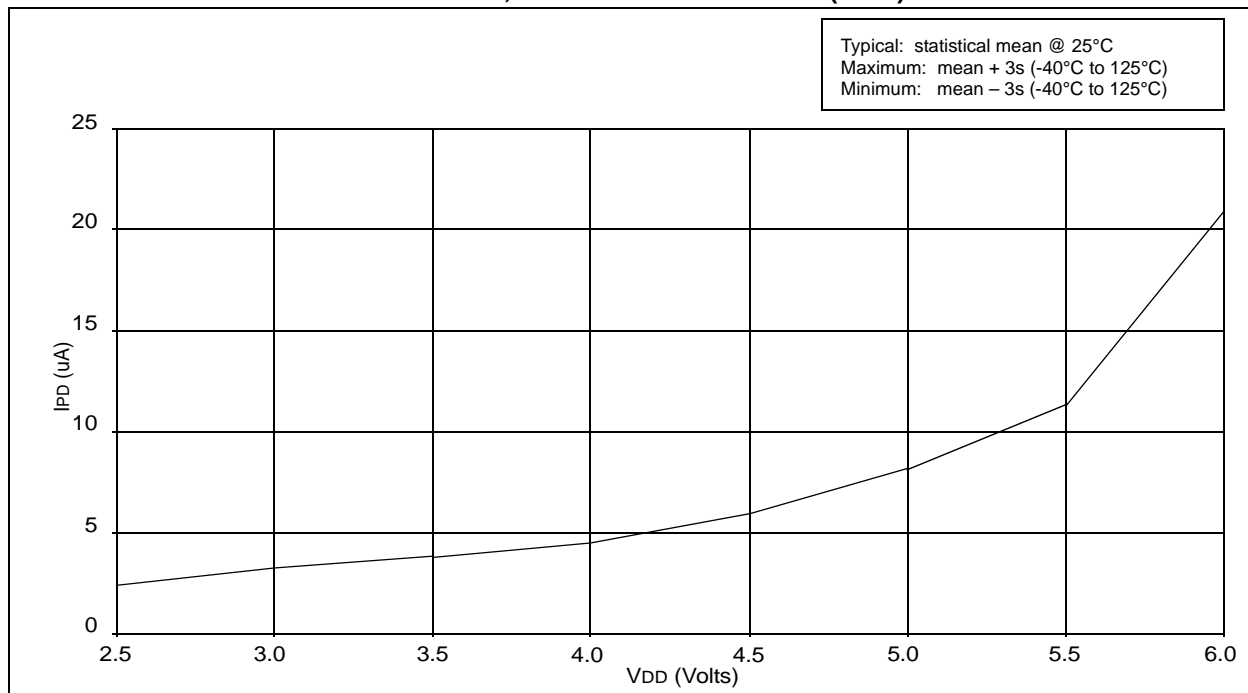


FIGURE 18-16: PORTA, B AND C I_{OH} vs. V_{OH}, V_{DD} = 5 V

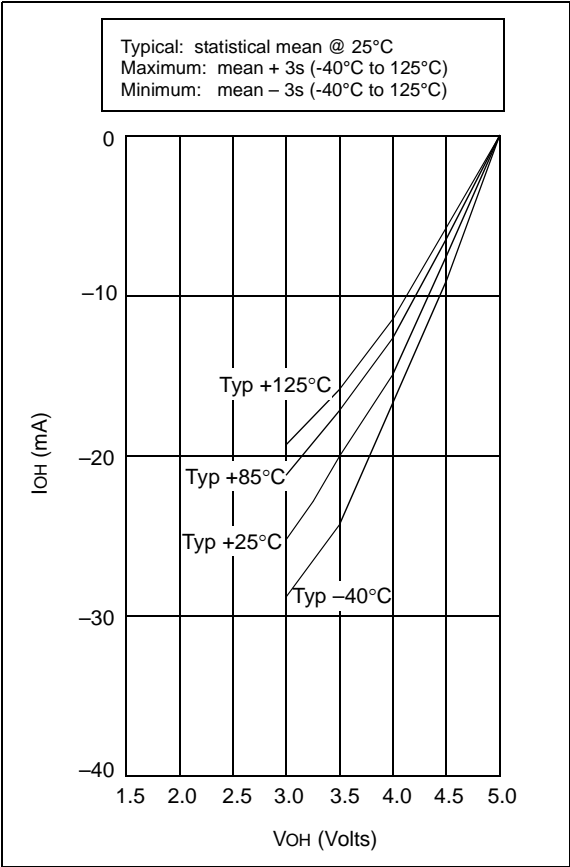
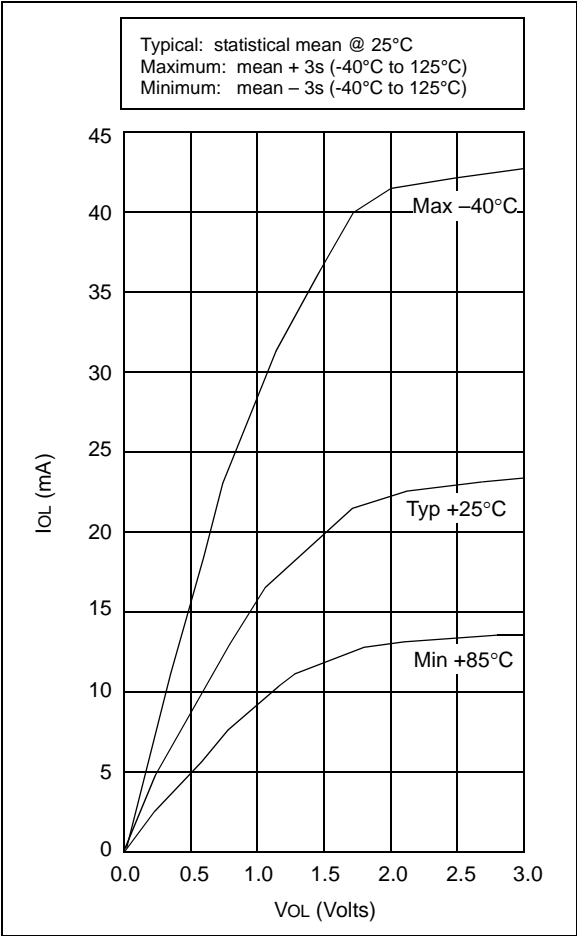
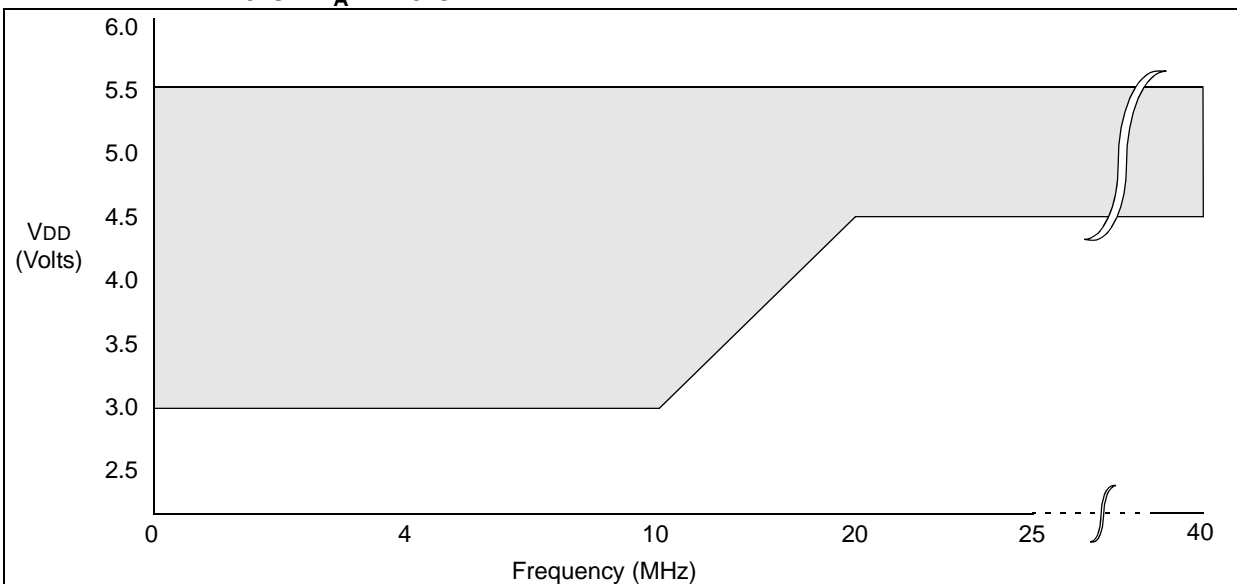


FIGURE 18-17: PORTA, B AND C I_{OL} vs. V_{OL}, V_{DD} = 3 V



PIC16C5X

FIGURE 19-1: PIC16C54C/C55A/C56A/C57C/C58B-40 VOLTAGE-FREQUENCY GRAPH, $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$



- Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.
- Note 2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
- Note 3:** Operation between 20 to 40 MHz requires the following:
- VDD between 4.5V. and 5.5V
 - OSC1 externally driven
 - OSC2 not connected
 - HS mode
 - Commercial temperatures
- Devices qualified for 40 MHz operation have -40 designation (ex: PIC16C54C-40/P).
- Note 4:** For operation between DC and 20 MHz, see Section 17.1.

FIGURE 19-6: TIMER0 CLOCK TIMINGS - PIC16C5X-40

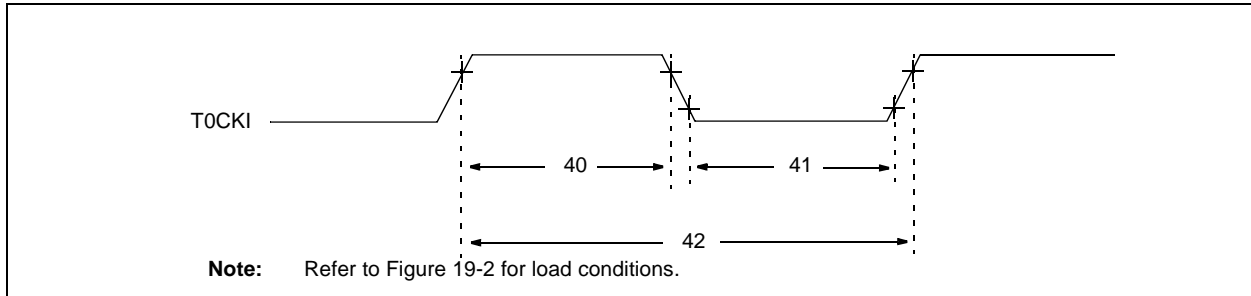


TABLE 19-4: TIMER0 CLOCK REQUIREMENTS PIC16C5X-40

AC Characteristics			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
		- With Prescaler	10^*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
		- With Prescaler	10^*	—	—	ns	
42	Tt0P	T0CKI Period	$20 \text{ or } \frac{T_{CY} + 40^*}{N}$	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

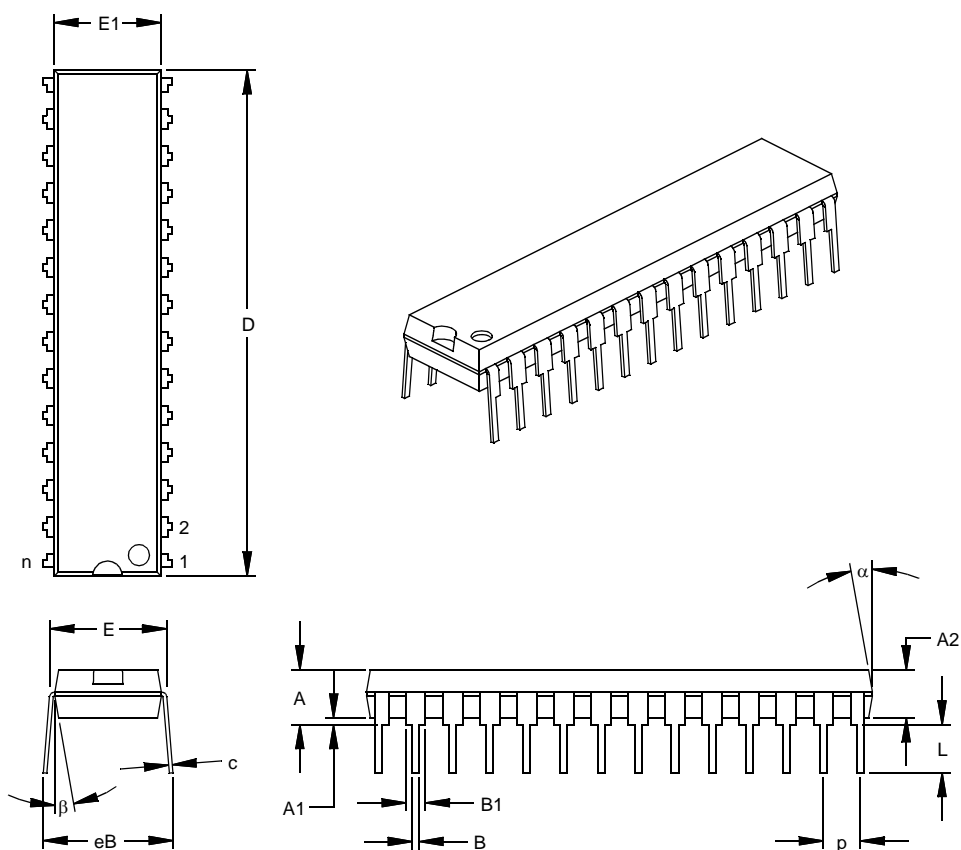
* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C5X

28-Lead Skinny Plastic Dual In-line (SP) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.150	.160	3.56	3.81	4.06
Molded Package Thickness	A2	.125	.130	.135	3.18	3.30	3.43
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.310	.325	7.62	7.87	8.26
Molded Package Width	E1	.275	.285	.295	6.99	7.24	7.49
Overall Length	D	1.345	1.365	1.385	34.16	34.67	35.18
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.040	.053	.065	1.02	1.33	1.65
Lower Lead Width	B	.016	.019	.022	0.41	0.48	0.56
Overall Row Spacing	§ eB	.320	.350	.430	8.13	8.89	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

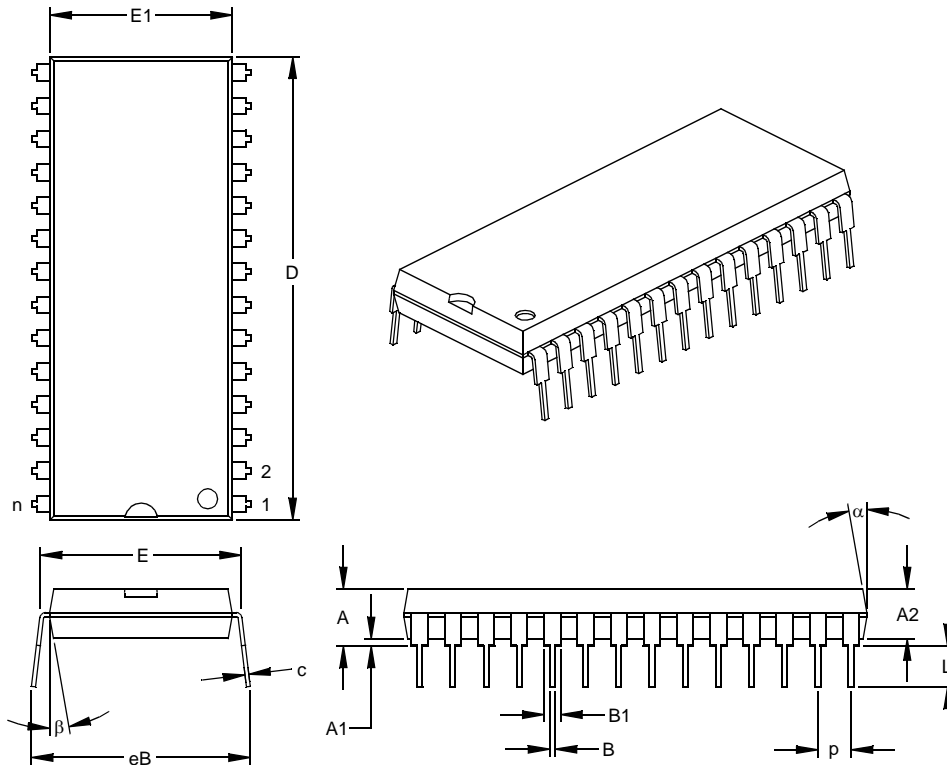
Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-095

Drawing No. C04-070

28-Lead Plastic Dual In-line (P) – 600 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.175	.190	4.06	4.45	4.83
Molded Package Thickness	A2	.140	.150	.160	3.56	3.81	4.06
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88
Molded Package Width	E1	.505	.545	.560	12.83	13.84	14.22
Overall Length	D	1.395	1.430	1.465	35.43	36.32	37.21
Tip to Seating Plane	L	.120	.130	.135	3.05	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.030	.050	.070	0.76	1.27	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§	.620	.650	.680	15.75	16.51	17.27
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-011

Drawing No. C04-079

APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

1. Check any `CALL`, `GOTO` or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change RESET vector to proper value for processor used.
6. Remove any use of the `ADDLW`, `RETURN` and `SUBLW` instructions.
7. Rewrite any code segments that use interrupts.

APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.

PIC16C5X

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this Data Sheet.

To: Technical Publications Manager
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Company _____
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City / State / ZIP / Country _____
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Application (optional):

Would you like a reply? ____Y ____N

Device: **PIC16C5X** Literature Number: **DS30453E**

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this data sheet easy to follow? If not, why?

4. What additions to the data sheet do you think would enhance the structure and subject?

5. What deletions from the data sheet could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

8. How would you improve our software, systems, and silicon products?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-	XX	X	/XX	XXX
Device		Frequency Range/OSC Type	Temperature Range	Package	Pattern
Device		PIC16C54 PIC16C54A PIC16CR54A PIC16C54C PIC16CR54C PIC16C55 PIC16C55A PIC16C56 PIC16C56A PIC16CR56A PIC16C57 PIC16C57C PIC16CR57C PIC16C58B PIC16CR58B	PIC16C54T ⁽²⁾ PIC16C54AT ⁽²⁾ PIC16CR54AT ⁽²⁾ PIC16C54CT ⁽²⁾ PIC16CR54CT ⁽²⁾ PIC16C55T ⁽²⁾ PIC16C55AT ⁽²⁾ PIC16C56T ⁽²⁾ PIC16C56AT ⁽²⁾ PIC16CR56AT ⁽²⁾ PIC16C57T ⁽²⁾ PIC16C57CT ⁽²⁾ PIC16CR57CT ⁽²⁾ PIC16C58BT ⁽²⁾ PIC16CR58BT ⁽²⁾		
Frequency Range/ Oscillator Type		RC Resistor Capacitor LP Low Power Crystal XT Standard Crystal/Resonator HS High Speed Crystal 02 200 KHz (LP) or 2 MHz (XT and RC) 04 200 KHz (LP) or 4 MHz (XT and RC) 10 10 MHz (HS only) 20 20 MHz (HS only) 40 40 MHz (HS only) b ⁽⁴⁾ No oscillator type for JW packages ⁽³⁾			
		*RC/LP/XT/HS are for 16C54/55/56/57 devices only -02 is available for 16LV54A only -04/10/20 options are available for all other devices -40 is available for 16C54C/55A/56A/57C/58B devices only			
Temperature Range		b ⁽⁴⁾ = 0°C to +70°C I = -40°C to +85°C E = -40°C to +125°C			
Package		S = Die in Waffle Pack JW = 28-pin 600 mil/18-pin 300 mil windowed CER-DIP ⁽³⁾ P = 28-pin 600 mil/18-pin 300 mil PDIP SO = 300 mil SOIC SS = 209 mil SSOP SP = 28-pin 300 mil Skinny PDIP			
		*See Section 21 for additional package information.			
Pattern		QTP, SQTP, ROM code (factory specified) or Special Requirements. Blank for OTP and Windowed devices.			

Examples:

- PIC16C55A - 04/P 301 = Commercial Temp., PDIP package, 4 MHz, standard VDD limits, QTP pattern #301
- PIC16LC54C - 04I/SO Industrial Temp., SOIC package, 200 kHz, extended VDD limits
- PIC16C57 - RC/SP = RC Oscillator, commercial temp, skinny PDIP package, 4 MHz, standard VDD limits
- PIC16C58BT -40/SS 123 = commercial temp, SSOP package in tape and reel, 4 MHz, extended VDD limits, ROM pattern #123

- Note**
- 1: C = normal voltage range
LC = extended
 - 2: T = in tape and reel - SOIC and SSOP packages only
 - 3: JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirements of each oscillator type, including LC devices.
 - 4: b = Blank

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Worldwide Site (www.microchip.com)