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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c56-lpe-so

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5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the MCLR/VPP pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is <u>RESET</u>. The DRT timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where MCLR is not tied to VDD is shown in Figure 5-3. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset TDRT msec after MCLR goes high.

In Figure 5-4, the on-chip Power-On Reset feature is being used (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the MCLR/VPP pin, and when the MCLR/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

Note: When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the <u>Embedded Control Handbook</u>.

The POR circuit does not produce an internal RESET when VDD declines.

FIGURE 5-2:

EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 k Ω will limit any current flowing into \overline{MCLR} from external capacitor C in the event of \overline{MCLR} pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

6.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 6-1).

The Special Registers can be classified into two sets. The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Details on Page
N/A	TRIS	I/O Cont	trol Regis	ters (TRIS	SA, TRIS	B, TRISC	;)			1111 1111	35
N/A	OPTION	Contains	s control b	oits to cor	figure Ti	mer0 and	Timer0/V	VDT pres	caler	11 1111	30
00h	INDF	Uses co	Jses contents of FSR to address data memory (not a physical register)					egister)	XXXX XXXX	32	
01h	TMR0	Timer0 I	Timer0 Module Register							XXXX XXXX	38
02h ⁽¹⁾	PCL	Low ord	er 8 bits c	of PC						1111 1111	31
03h	STATUS	PA2	PA1	PA0	TO	PD	Z	DC	С	0001 1xxx	29
04h	FSR	Indirect	Indirect data memory address pointer						•	1xxx xxxx (3)	32
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	xxxx	35
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	XXXX XXXX	35
07h ⁽²⁾	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	XXXX XXXX	35

|--|

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 6.5 for an explanation of how to access these bits.

2: File address 07h is a General Purpose Register on the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16CR58 and PIC16CR58.

3: These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for MCLR and WDT Reset, the value is 111u uuuu.

PIC16C5X

COMF	Complement f							
Syntax:	[<i>label</i>] COMF f,d							
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$							
Operation:	$(\overline{f}) \rightarrow (dest)$							
Status Affected:	Z							
Encoding:	0010 01df ffff							
Description:	The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.							
Words:	1							
Cycles:	1							
Example:	COMF REG1,0							
Before Instru	ction							
REG1	= 0x13							
After Instruct	ion							
REG1	= 0x13							
W	= 0xEC							

DECF	Decrement f							
Syntax:	[label] DECF f,d							
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$							
Operation:	(f) – 1	\rightarrow (dest)						
Status Affected:	Z							
Encoding:	0000	11df	ffff					
Description:	Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.							
Words:	1							
Cycles:	1							
Example:	DECF	CNT,	1					
Before Instruc CNT Z After Instructi CNT Z	ction = = on = =	0x01 0 0x00 1						

DECFSZ	Decrement f, Skip if 0							
Syntax:	[label] DECFSZ f,d							
Operands:	$\begin{array}{l} 0\leq f\leq 31\\ d\in [0,1] \end{array}$							
Operation:	(f) $-1 \rightarrow d$; skip if result = 0							
Status Affected:	None							
Encoding:	0010 11df ffff							
Description:	The contents of register 'f' are dec- remented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, the next instruc- tion, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle							
Words:	1							
Cycles:	1(2)							
Example:	HERE DECFSZ CNT, 1 GOTO LOOP							
	CONTINUE • • •							
Before Instru	uction							
PC	= address (HERE)							
After Instruc	tion							
CNT	= CNT - 1;							
IT CN I	= 0,							
	= address (CONTINUE);							
	\neq U, - address (UFDF, 1)							
FU	= addless (HERE+1)							

SUBWF	Subtr	act V	V from	f				
Syntax:	[label]	S	UBWF	f,d				
Operands:	$0 \le f \le d \in [0]$	≦ 31 (,1]						
Operation:	(f) – (^v	$W) \rightarrow$	(dest)					
Status Affected:	C, DC	;, Z						
Encoding:	0000) 1	LOdf	ffff				
Description:	Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.							
Words:	1							
Cycles:	1							
Example 1:	SUBW	F	REG1,	1				
Before Instruct REG1 W C After Instructi REG1 W C Example 2: Before Instructi REG1 W C After Instructi	ction = = on = = ction = = on	3 2 ? 1 2 1 2 ?	; resu	ılt is posi	tive			
REG1	=	0						
W	=	2						
С	=	1	; resu	ult is zero				
Example 3: Before Inst REG1 W C After Instructi	ructior = = = on	ו 1 2 ?						
REG1	=	0xFl	F					
W	=	2						
С	=	0	; resu	ılt is nega	ative			

SWAPF	Swap Nibbles in f						
Syntax:	[label] SWAPF f,d						
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$						
Operation:	$(f<3:0>) \rightarrow (dest<7:4>);$ $(f<7:4>) \rightarrow (dest<3:0>)$						
Status Affected:	None						
Encoding:	0011 10df ffff						
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.						
Words:	1						
Cycles:	1						
Example	SWAPF REG1, 0						
REG1 After Instructi REG1 W	= 0xA5 ion = 0xA5 = 0x5A						
TRIS	Load TRIS Register						
Syntax:	[<i>label</i>] TRIS f						
Operands:	f = 5, 6 or 7						
Operation:	$(W) \rightarrow TRIS$ register f						
Status Affected:	None						
Encoding:	0000 0000 0fff						
Description:	TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register.						
Words:	1						
Cycles:	1						
Example	TRIS PORTB						
Example TRIS PORTB Before Instruction W = 0xA5 After Instruction TRISB = 0xA5							

12.7 Timing Diagrams and Specifications



FIGURE 12-2: EXTERNAL CLOCK TIMING - PIC16C54/55/56/57

TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57

	Standard Operating Conditions (unless otherwise specified)								
AC Characteristics		Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial							
		-40)°C ≤]	TA ≤ + 85°	C for ind	ustrial			
		$-40^{\circ}C \le TA \le +125^{\circ}C$ for extended							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions		
1A	Fosc	External CLKIN Frequency ⁽¹⁾	DC		4.0	MHz	XT OSC mode		
			DC	—	10	MHz	10 MHz mode		
			DC	—	20	MHz	HS OSC mode (Comm/Ind)		
			DC	—	16	MHz	HS OSC mode (Ext)		
			DC	—	40	kHz	LP OSC mode		
		Oscillator Frequency ⁽¹⁾	DC	—	4.0	MHz	RC OSC mode		
			0.1	—	4.0	MHz	XT OSC mode		
			4.0	—	10	MHz	10 MHz mode		
			4.0	—	20	MHz	HS OSC mode (Comm/Ind)		
			4.0	—	16	MHz	HS OSC mode (Ext)		
			DC	_	40	kHz	LP osc mode		

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

13.3 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

DC CH	ARACTE	RISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$						
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions		
D030	VIL	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD	> > > > >	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes		
D040	Vih	Input High Voltage I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	2.0 0.6 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD		VDD VDD VDD VDD VDD VDD	V V V V V	VDD = 3.0V to 5.5V ⁽⁴⁾ Full VDD range ⁽⁴⁾ RC mode only ⁽³⁾ XT, HS and LP modes		
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	_	_	V			
D060	lı∟	Input Leakage Current ^(1,2) I/O ports	-1.0	_	+1.0	μA	For VDD \leq 5.5V: VSS \leq VPIN \leq VDD, pin at hi-impedance		
		MCLR MCLR TOCKI OSC1	-5.0 -3.0 -3.0	 0.5 0.5 0.5		μΑ μΑ μΑ μΑ	$VPIN = VSS + 0.25V$ $VPIN = VDD$ $VSS \le VPIN \le VDD$ $VSS \le VPIN \le VDD,$ $XT, HS and LP modes$		
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.5 0.5	V V	IOL = 10 mA, VDD = 6.0 V IOL = 1.9 mA, VDD = 6.0 V, RC mode only		
D090	Vон	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	Vdd – 0.5 Vdd – 0.5	_		V V	IOH = -4.0 mA, VDD = 6.0 V IOH = -0.8 mA, VDD = 6.0 V, RC mode only		

* These parameters are characterized but not tested.

- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- **Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
 - 2: Negative current is defined as coming out of the pin.
 - **3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
 - 4: The user may use the better of the two specifications.

13.5 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS

2. Tp	pS	
Т		
F	Frequency	T Time
Lowe	ercase letters (pp) and their meanings:	
рр		
2	to	mc MCLR
ck	CLKOUT	osc oscillator
су	cycle time	os OSC1
drt	device reset timer	t0 T0CKI
io	I/O port	wdt watchdog timer
Uppe	ercase letters and their meanings:	
S		
F	Fall	P Period
Н	High	R Rise
Ι	Invalid (Hi-impedance)	V Valid
L	Low	Z Hi-impedance

FIGURE 13-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16CR54A





FIGURE 14-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED



15.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended) PIC16LC54A-04E (Extended)

PIC16I	C54A-04F		Stand	, ard One	ratino	, Condi	tions (unless otherwise specified)		
(Exten	ded)	-	Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended						
PIC16C54A-04E, 10E, 20E (Extended)				Standard Operating Conditions (unless otherwise specified Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions		
	Vdd	Supply Voltage							
D001		PIC16LC54A	3.0 2.5		6.25 6.25	V V	XT and RC modes LP mode		
D001A		PIC16C54A	3.5 4.5		5.5 5.5	V V	RC and XT modes HS mode		
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾		1.5*	—	V	Device in SLEEP mode		
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	-	Vss	_	V	See Section 5.1 for details on Power-on Reset		
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset		
	IDD	Supply Current ⁽²⁾							
D010		PIC16LC54A	-	0.5	25	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes		
			-	11	27	μA	Fosc = 32 kHz, VDD = 2.5V, LP mode, Commercial		
				11	35	μA	Fosc = 32 kHz, VDD = 2.5V, LP mode, Industrial		
			—	11	37	μA	Fosc = 32 kHz, VDD = 2.5V, LP mode, Extended		
D010A		PIC16C54A	—	1.8	3.3	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes		
			-	4.8	10	mA	Fosc = 10 MHz, VDD = 5.5V, HS mode		
			-	9.0	20	mA	Fosc = 20 MHz, VDD = 5.5V, HS mode		

Legend: Rows with standard voltage device data only are shaded for improved readability.

- * These parameters are characterized but not tested.
- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

16.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.



FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

TABLE 16-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Average Fosc @ 5 V, 25°C	
20 pF	3.3K	5 MHz	± 27%
	5K	3.8 MHz	± 21%
	10K	2.2 MHz	± 21%
	100K	262 kHz	± 31%
100 pF	3.3K	1.6 MHz	± 13%
	5K	1.2 MHz	± 13%
	10K	684 kHz	± 18%
	100K	71 kHz	± 25%
300 pF	3.3K	660 kHz	± 10%
	5.0K	484 kHz	± 14%
	10K	267 kHz	± 15%
	100K	29 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for VDD = 5V.



FIGURE 16-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 PF, 25°C

FIGURE 16-7: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS - VDD







Typical: statistical mean @ 25°C. Maximum: mean - 3 s (-40°C to 125°C) Minimum: mean

FIGURE 16-14: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 PF, 25°C)

FIGURE 16-15: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 PF, -40°C to +85°C)









17.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial)		Stand: Opera	ard Ope ting Terr	e rating peratu	Condit re	ions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial	
PIC16C5X PIC16CR5X (Commercial, Industrial)			Standa Opera	ard Ope ting Terr	e rating nperatu	Condit re	ions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions
	IPD	Power-down Current ⁽²⁾					
D020		PIC16LC5X	—	0.25	2	μΑ	VDD = 2.5V, WDT disabled, Commercial
			—	0.25	3	μA	VDD = 2.5V, WDT disabled, Industrial
			_	1 1 25	5	μΑ μΑ	VDD = $2.5V$, WDT enabled, Commercial
		PIC16C5X		0.25	4.0	μΔ	$V_{DD} = 3.0V$ WDT disabled Commercial
DOZON				0.25	5.0	μ/(μΑ	$V_{DD} = 3.0V$, WDT disabled, Industrial
			_	1.8	7.0*	μA	VDD = 5.5V, WDT disabled, Commercial
			—	2.0	8.0*	μA	VDD = 5.5V, WDT disabled, Industrial
			—	4	12*	μA	VDD = 3.0V, WDT enabled, Commercial
				4	14*	μA	VDD = 3.0V, WDT enabled, Industrial
			—	9.8	27*	μA	VDD = 5.5V, WDT enabled, Commercial
				12	30*	μA	VDD = 5.5V, WDT enabled, Industrial

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .



TΔRI F 17-2·	CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X PIC16CR5X

AC Chara	acteristics	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for extended} \end{array}$				
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾		15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	_	40**	ns
15	TioV2ckH	Port in valid before CLKOUT ⁽¹⁾	0.25 TCY+30*	_	—	ns
16	TckH2iol	Port in hold after CLKOUT ⁽¹⁾	0*	_	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽²⁾	—	_	100*	ns
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD		—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽²⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Refer to Figure 17-5 for load conditions.

19.0 ELECTRICAL CHARACTERISTICS - PIC16LC54C 40MHz

Absolute Maximum Ratings^(†)

Ambient temperature under bias	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	–0.6V to (VDD + 0.6V)
Total power dissipation ⁽¹⁾	
Max. current out of Vss pin	
Max. current into Vod pin	
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, IIK (VI < 0 or VI > VDD)	±20 mA
Output clamp current, Iок (Vo < 0 or Vo > Voo)	±20 mA
Max. output current sunk by any I/O pin	
Max. output current sourced by any I/O pin	
Max. output current sourced by a single I/O (Port A, B or C)	
Max. output current sunk by a single I/O (Port A, B or C)	
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH} + \sum {(VI	DD-VOH) x IOH} + Σ (VOL x IOL)

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

20.0 DEVICE CHARACTERIZATION - PIC16LC54C 40MHz

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.





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PIC16C5X



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