



Welcome to E-XFL.COM

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

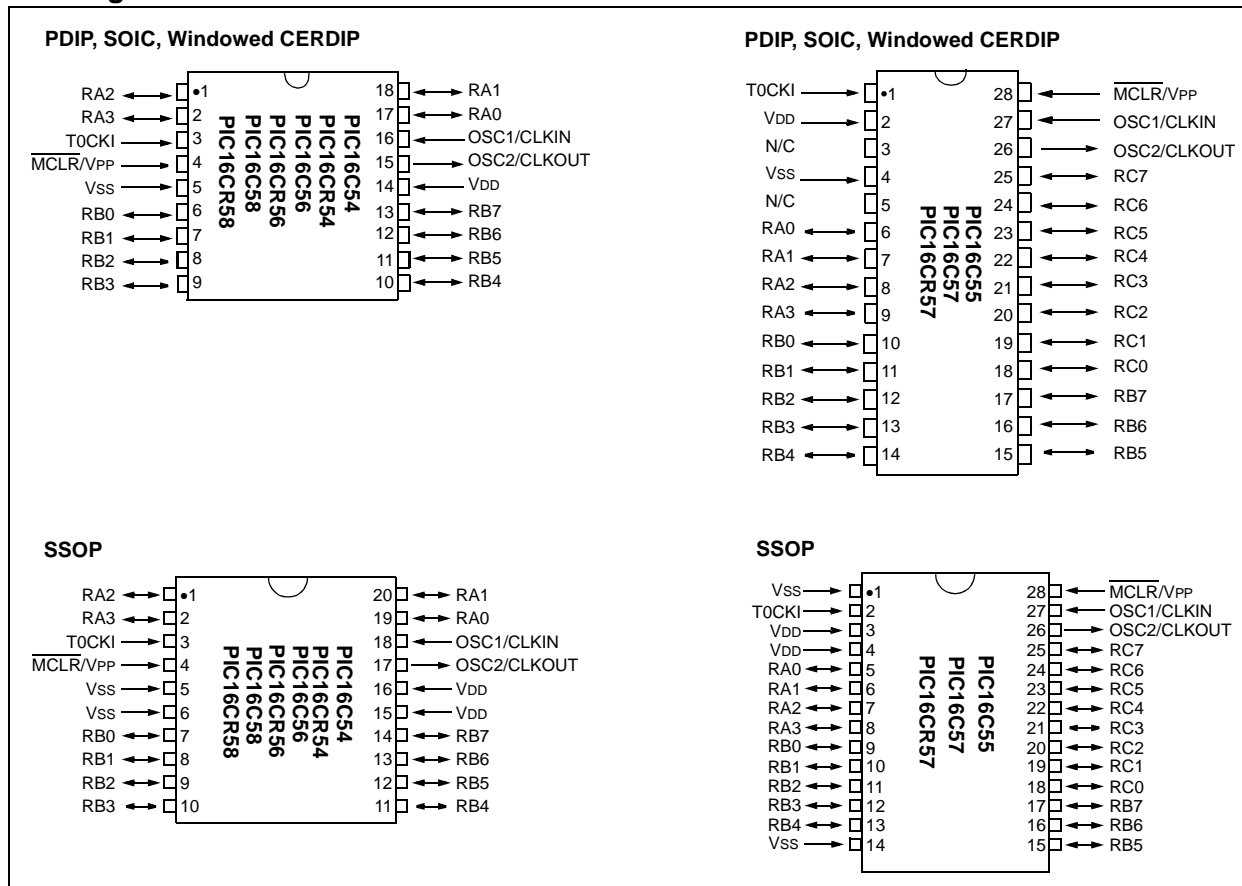
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c56-rc-ss

PIC16C5X

Pin Diagrams



Device Differences

Device	Voltage Range	Oscillator Selection (Program)	Oscillator	Process Technology (Microns)	ROM Equivalent	MCLR Filter
PIC16C54	2.5-6.25	Factory	See Note 1	1.2	PIC16CR54A	No
PIC16C54A	2.0-6.25	User	See Note 1	0.9	—	No
PIC16C54C	2.5-5.5	User	See Note 1	0.7	PIC16CR54C	Yes
PIC16C55	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C55A	2.5-5.5	User	See Note 1	0.7	—	Yes
PIC16C56	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C56A	2.5-5.5	User	See Note 1	0.7	PIC16CR56A	Yes
PIC16C57	2.5-6.25	Factory	See Note 1	1.2	—	No
PIC16C57C	2.5-5.5	User	See Note 1	0.7	PIC16CR57C	Yes
PIC16C58B	2.5-5.5	User	See Note 1	0.7	PIC16CR58B	Yes
PIC16CR54A	2.5-6.25	Factory	See Note 1	1.2	N/A	Yes
PIC16CR54C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR56A	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR57C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR58B	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

Note: The table shown above shows the generic names of the PIC16C5X devices. For device varieties, please refer to Section 2.0.

PIC16C5X

NOTES:

5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the $\overline{\text{MCLR}}/\text{VPP}$ pin to VDD . A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is RESET. The DRT timer begins counting once it detects $\overline{\text{MCLR}}$ to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where $\overline{\text{MCLR}}$ is not tied to VDD is shown in Figure 5-3. VDD is allowed to rise and stabilize before bringing $\overline{\text{MCLR}}$ high. The chip will actually come out of reset TDRT msec after $\overline{\text{MCLR}}$ goes high.

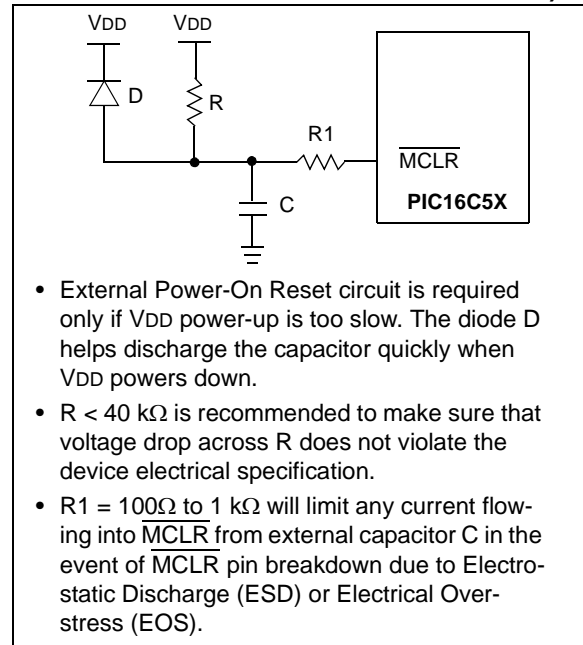
In Figure 5-4, the on-chip Power-On Reset feature is being used ($\overline{\text{MCLR}}$ and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the $\overline{\text{MCLR}}/\text{VPP}$ pin, and when the $\overline{\text{MCLR}}/\text{VPP}$ pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the $\text{VDD}(\text{min})$ value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

Note: When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the [Embedded Control Handbook](#).

The POR circuit does not produce an internal RESET when VDD declines.

FIGURE 5-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



6.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the \overline{TO} and \overline{PD} bits are not

writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS Register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 10.0, Instruction Set Summary.

REGISTER 6-1: STATUS REGISTER (ADDRESS: 03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
PA2	PA1	PA0	\overline{TO}	\overline{PD}	Z	DC	C
bit 7			bit 0				

bit 7: **PA2:** This bit unused at this time.

Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

bit 6-5: **PA<1:0>:** Program page preselect bits (PIC16C56/CR56)(PIC16C57/CR57)(PIC16C58/CR58)

00 = Page 0 (000h - 1FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58

01 = Page 1 (200h - 3FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58

10 = Page 2 (400h - 5FFh) - PIC16C57/CR57, PIC16C58/CR58

11 = Page 3 (600h - 7FFh) - PIC16C57/CR57, PIC16C58/CR58

Each page is 512 words.

Using the PA<1:0> bits as general purpose read/write bits in devices which do not use them for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: **\overline{TO} :** Time-out bit

1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction

0 = A WDT time-out occurred

bit 3: **\overline{PD} :** Power-down bit

1 = After power-up or by the `CLRWDT` instruction

0 = By execution of the `SLEEP` instruction

bit 2: **Z:** Zero bit

1 = The result of an arithmetic or logic operation is zero

0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC:** Digit carry/borrow bit (for `ADDWF` and `SUBWF` instructions)

ADDWF

1 = A carry from the 4th low order bit of the result occurred

0 = A carry from the 4th low order bit of the result did not occur

SUBWF

1 = A borrow from the 4th low order bit of the result did not occur

0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C:** Carry/borrow bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

ADDWF

1 = A carry occurred

0 = A carry did not occur

SUBWF

1 = A borrow did not occur

0 = A borrow occurred

RRF or RLF

Loaded with LSb or MSb, respectively

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

1 = bit is set

0 = bit is cleared

x = bit is unknown

PIC16C5X

6.4 OPTION Register

The OPTION Register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W Register will be transferred to the OPTION Register. A RESET sets the OPTION<5:0> bits.

REGISTER 6-2: OPTION REGISTER

U-0	U-0	W-1	W-1	W-1	W-1	W-1	W-1	
—	—	T0CS	TOSE	PSA	PS2	PS1	PS0	
bit 7								bit 0

bit 7-6: **Unimplemented:** Read as '0'

bit 5: **T0CS:** Timer0 clock source select bit

1 = Transition on T0CKI pin

0 = Internal instruction cycle clock (CLKOUT)

bit 4: **TOSE:** Timer0 source edge select bit

1 = Increment on high-to-low transition on T0CKI pin

0 = Increment on low-to-high transition on T0CKI pin

bit 3: **PSA:** Prescaler assignment bit

1 = Prescaler assigned to the WDT

0 = Prescaler assigned to Timer0

bit 2-0: **PS<2:0>:** Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

1 = bit is set

0 = bit is cleared

x = bit is unknown

6.7 Indirect Data Addressing; INDF and FSR Registers

The INDF Register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR Register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 6-1: INDIRECT ADDRESSING

- Register file 08 contains the value 10h
- Register file 09 contains the value 0Ah
- Load the value 08 into the FSR Register
- A read of the INDF Register will return the value of 10h
- Increment the value of the FSR Register by one (FSR = 09h)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF Register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 6-2.

EXAMPLE 6-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```

MOV LW  H'10'    ; initialize pointer
MOV WF  FSR      ; to RAM
NEXT    CLR F    INDF ; clear INDF Register
        INC F    FSR,F ; inc pointer
        BTFSC   FSR,4 ; all done?
        GOTO    NEXT ; NO, clear next

CONTINUE
        :          ; YES, continue
    
```

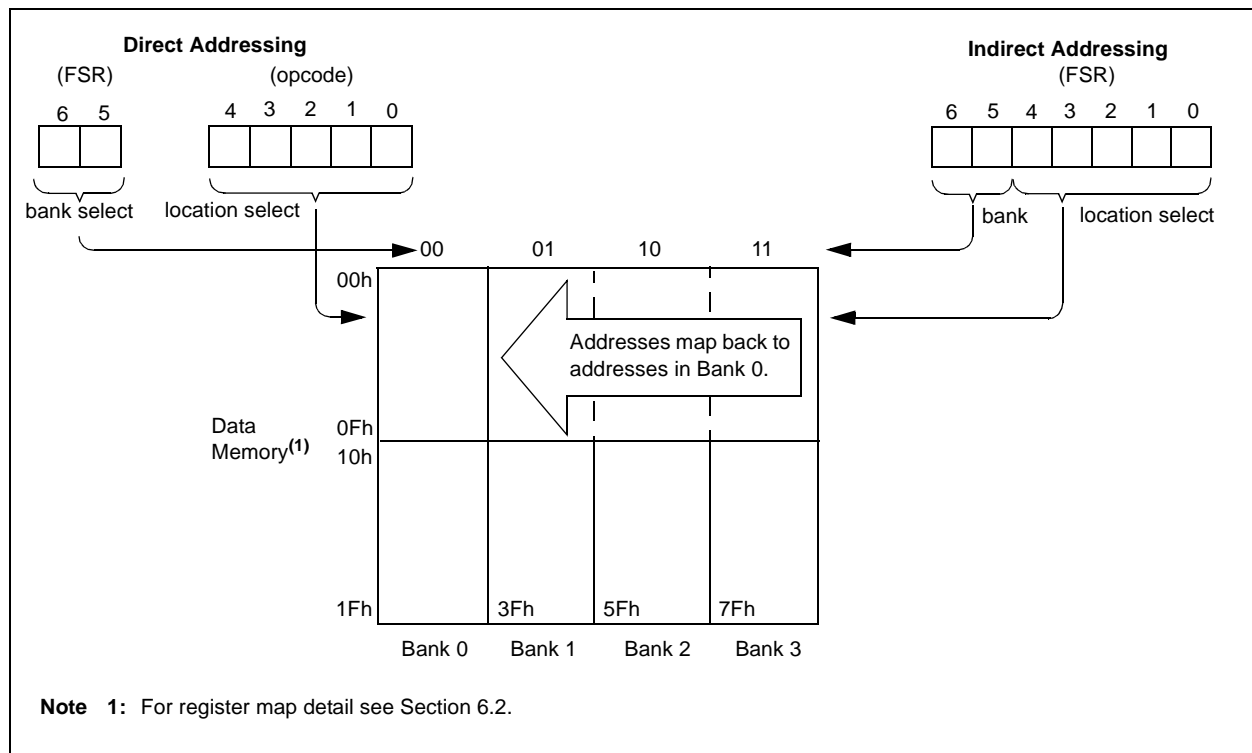
The FSR is either a 5-bit (PIC16C54, PIC16CR54, PIC16C55, PIC16CR55, PIC16C56, PIC16CR56) or 7-bit (PIC16C57, PIC16CR57, PIC16C58, PIC16CR58) wide register. It is used in conjunction with the INDF Register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC16C54, PIC16CR54, PIC16C55, PIC16CR55, PIC16C56, PIC16CR56: These do not use banking. FSR<6:5> bits are unimplemented and read as '1's.

PIC16C57, PIC16CR57, PIC16C58, PIC16CR58: FSR<6:5> are the bank select bits and are used to select the bank to be addressed (00 = bank 0, 01 = bank 1, 10 = bank 2, 11 = bank 3).

FIGURE 6-10: DIRECT/INDIRECT ADDRESSING



8.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

8.1.1 EXTERNAL CLOCK SYNCHRONIZATION

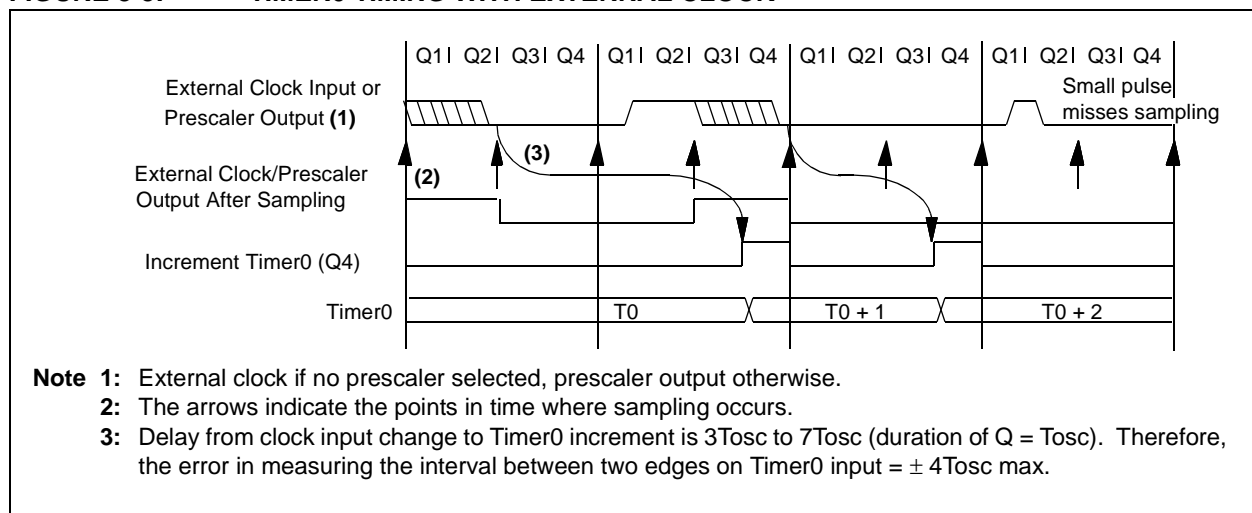
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 8-5). Therefore, it is necessary for T0CKI to be high for at least $2T_{osc}$ (and a small RC delay of 20 ns) and low for at least $2T_{osc}$ (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least $4T_{osc}$ (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

8.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 8-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 8-5: TIMER0 TIMING WITH EXTERNAL CLOCK



9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC16C5X family of microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator Selection (Section 4.0)
- RESET (Section 5.0)
- Power-On Reset (Section 5.1)
- Device Reset Timer (Section 5.2)
- Watchdog Timer (WDT) (Section 9.2)
- SLEEP (Section 9.3)
- Code protection (Section 9.4)
- ID locations (Section 9.5)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in RESET until the crystal oscillator is stable. With this timer on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake up from SLEEP through external RESET or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

9.3 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

9.3.1 SLEEP

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the \overline{TO} bit (STATUS<4>) is set, the \overline{PD} bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the \overline{MCLR}/VPP pin low.

For lowest current consumption while powered down, the $T0CKI$ input should be at VDD or VSS and the \overline{MCLR}/VPP pin must be at a logic high level ($\overline{MCLR} = V_{IH}$).

9.3.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. An external RESET input on \overline{MCLR}/VPP pin.
2. A Watchdog Timer Time-out Reset (if WDT was enabled).

Both of these events cause a device RESET. The \overline{TO} and \overline{PD} bits can be used to determine the cause of device RESET. The \overline{TO} bit is cleared if a WDT time-out occurred (and caused wake-up). The \overline{PD} bit, which is set on power-up, is cleared when SLEEP is invoked.

The WDT is cleared when the device wakes from SLEEP, regardless of the wake-up source.

9.4 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

9.5 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

Note: Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

ADDWF Add W and f

Syntax: [*label*] ADDWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) + (f) \rightarrow (\text{dest})$

Status Affected: C, DC, Z

Encoding:

0001	11df	ffff
------	------	------

Description: Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: ADDWF TEMP_REG, 0

Before Instruction

W = 0x17

TEMP_REG = 0xC2

After Instruction

W = 0xD9

TEMP_REG = 0xC2

ANDWF AND W with f

Syntax: [*label*] ANDWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) .\text{AND}. (f) \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

0001	01df	ffff
------	------	------

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: ANDWF TEMP_REG, 1

Before Instruction

W = 0x17

TEMP_REG = 0xC2

After Instruction

W = 0x17

TEMP_REG = 0x02

ANDLW AND literal with W

Syntax: [*label*] ANDLW k

Operands: $0 \leq k \leq 255$

Operation: $(W) .\text{AND}. (k) \rightarrow (W)$

Status Affected: Z

Encoding:

1110	kkkk	kkkk
------	------	------

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: ANDLW H'5F'

Before Instruction

W = 0xA3

After Instruction

W = 0x03

BCF Bit Clear f

Syntax: [*label*] BCF f,b

Operands: $0 \leq f \leq 31$
 $0 \leq b \leq 7$

Operation: $0 \rightarrow (f)$

Status Affected: None

Encoding:

0100	bbbf	ffff
------	------	------

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example: BCF FLAG_REG, 7

Before Instruction

FLAG_REG = 0xC7

After Instruction

FLAG_REG = 0x47

PIC16C5X

12.5 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	V _{IL}	Input Low Voltage					
		I/O ports	V _{SS}	—	0.15 V _{DD}	V	Pin at hi-impedance PIC16C5X-RC only ⁽³⁾ PIC16C5X-XT, 10, HS, LP
		MCLR (Schmitt Trigger)	V _{SS}	—	0.15 V _{DD}	V	
		T0CKI (Schmitt Trigger)	V _{SS}	—	0.15 V _{DD}	V	
		OSC1 (Schmitt Trigger)	V _{SS}	—	0.15 V _{DD}	V	
		OSC1 (Schmitt Trigger)	V _{SS}	—	0.3 V _{DD}	V	
D040	V _{IH}	Input High Voltage					
		I/O ports	0.45 V _{DD}	—	V _{DD}	V	For all V _{DD} ⁽⁴⁾ 4.0V < V _{DD} ≤ 5.5V ⁽⁴⁾ V _{DD} > 5.5 V
		I/O ports	2.0	—	V _{DD}	V	
		I/O ports	0.36 V _{DD}	—	V _{DD}	V	
		MCLR (Schmitt Trigger)	0.85 V _{DD}	—	V _{DD}	V	
		T0CKI (Schmitt Trigger)	0.85 V _{DD}	—	V _{DD}	V	PIC16C5X-RC only ⁽³⁾ PIC16C5X-XT, 10, HS, LP
		OSC1 (Schmitt Trigger)	0.85 V _{DD}	—	V _{DD}	V	
D050	V _{HYS}	Hysteresis of Schmitt Trigger inputs	0.15 V _{DD} *	—	—	V	
D060	I _{IL}	Input Leakage Current ^(1,2)					For V_{DD} ≤ 5.5 V: V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance V _{PIN} = V _{SS} + 0.25V V _{PIN} = V _{DD} V _{SS} ≤ V _{PIN} ≤ V _{DD} V _{SS} ≤ V _{PIN} ≤ V _{DD} , PIC16C5X-XT, 10, HS, LP
		I/O ports	−1	0.5	+1	μA	
		MCLR	−5	—	—	μA	
		MCLR	—	0.5	+5	μA	
		T0CKI	−3	0.5	+3	μA	
D080	V _{OL}	Output Low Voltage					
		I/O ports	—	—	0.6	V	I _{OL} = 8.7 mA, V _{DD} = 4.5V I _{OL} = 1.6 mA, V _{DD} = 4.5V, PIC16C5X-RC
D090	V _{OH}	Output High Voltage ⁽²⁾					
		I/O ports	V _{DD} − 0.7	—	—	V	I _{OH} = −5.4 mA, V _{DD} = 4.5V I _{OH} = −1.0 mA, V _{DD} = 4.5V, PIC16C5X-RC
D090	V _{OH}	OSC2/CLKOUT	V _{DD} − 0.7	—	—	V	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

PIC16C5X

12.7 Timing Diagrams and Specifications

FIGURE 12-2: EXTERNAL CLOCK TIMING - PIC16C54/55/56/57

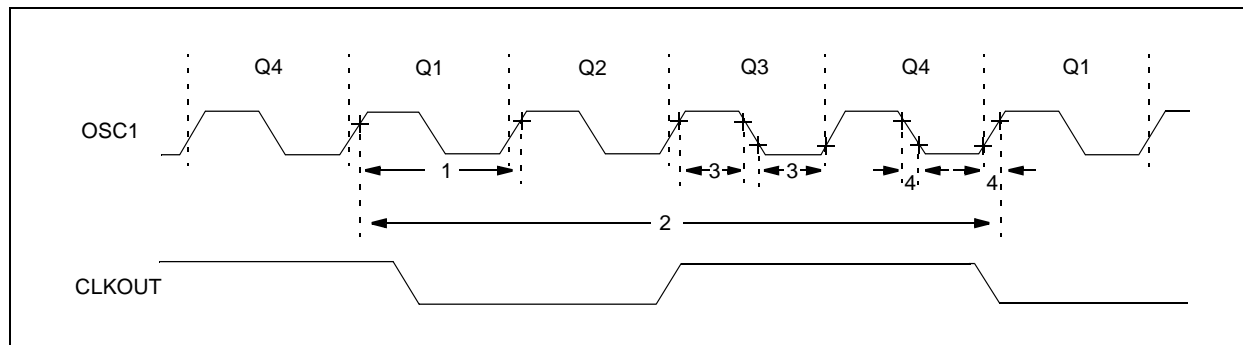


TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics		Operating Temperature					
		0°C ≤ TA ≤ +70°C for commercial					
		−40°C ≤ TA ≤ +85°C for industrial					
		−40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
1A	FOSC	External CLKIN Frequency ⁽¹⁾	DC	—	4.0	MHz	XT osc mode
			DC	—	10	MHz	10 MHz mode
			DC	—	20	MHz	HS osc mode (Comm/Ind)
			DC	—	16	MHz	HS osc mode (Ext)
			DC	—	40	kHz	LP osc mode
		Oscillator Frequency ⁽¹⁾	DC	—	4.0	MHz	RC osc mode
			0.1	—	4.0	MHz	XT osc mode
			4.0	—	10	MHz	10 MHz mode
			4.0	—	20	MHz	HS osc mode (Comm/Ind)
			4.0	—	16	MHz	HS osc mode (Ext)
			DC	—	40	kHz	LP osc mode

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 12-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54/55/56/57

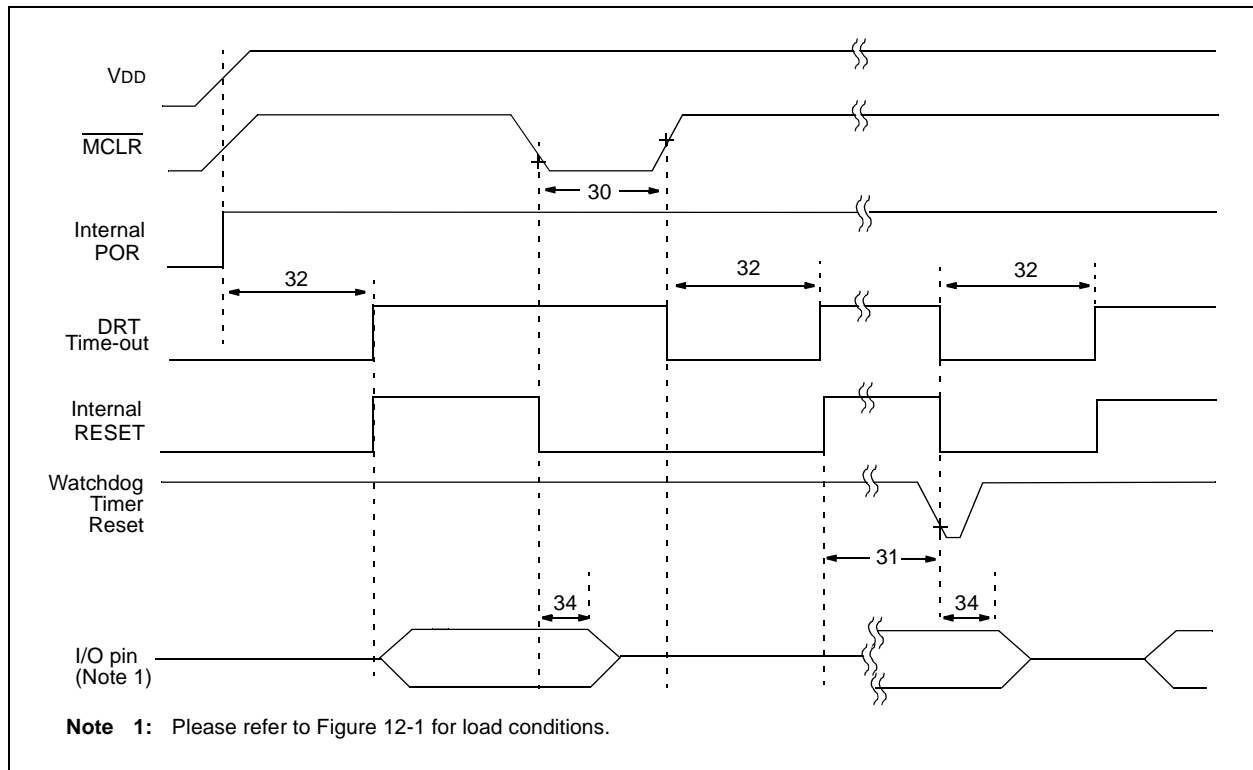


TABLE 12-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics							
Operating Temperature							
0°C ≤ TA ≤ +70°C for commercial							
-40°C ≤ TA ≤ +85°C for industrial							
-40°C ≤ TA ≤ +125°C for extended							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	100*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	—	—	100*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C5X

FIGURE 13-3: CLKOUT AND I/O TIMING - PIC16CR54A

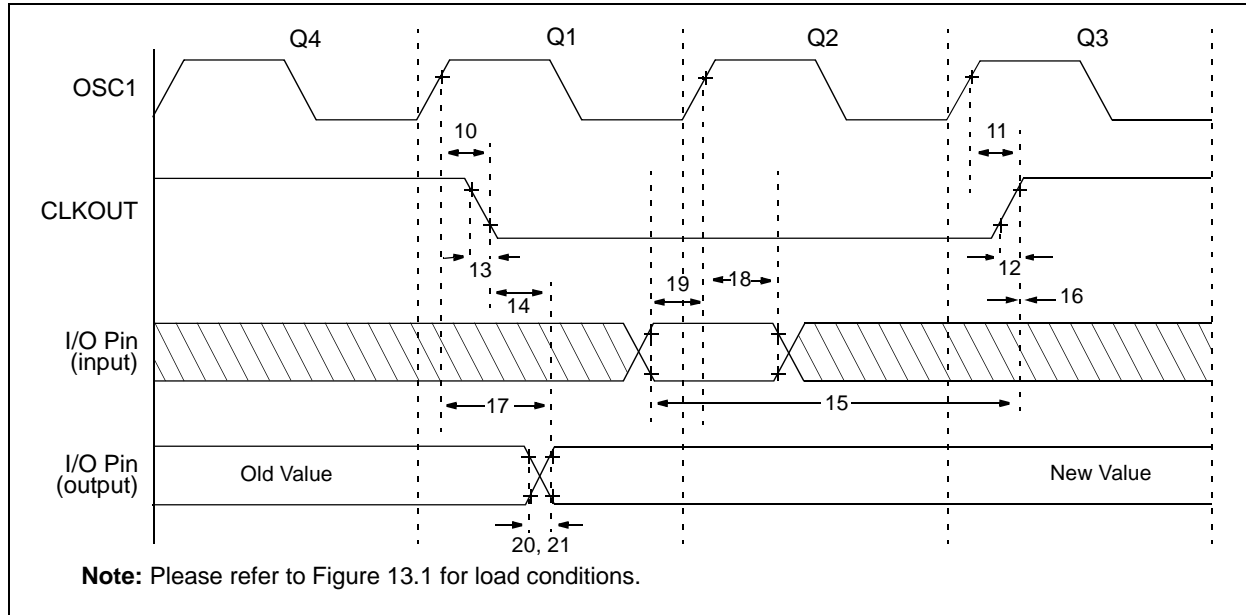


TABLE 13-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR54A

AC Characteristics		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature				
		0°C ≤ TA ≤ +70°C for commercial				
		-40°C ≤ TA ≤ +85°C for industrial				
		-40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽¹⁾	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ ⁽¹⁾	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽²⁾	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽²⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

2: Please refer to Figure 13.1 for load conditions.

PIC16C5X

NOTES:

PIC16C5X

17.3 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial, Extended) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial, Extended) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature				
			0°C ≤ TA ≤ +70°C for commercial				
			-40°C ≤ TA ≤ +85°C for industrial				
			-40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	VIL	Input Low Voltage I/O Ports I/O Ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VSS VSS VSS VSS VSS VSS	— — — — — —	0.8 V 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V V V	4.5V < VDD ≤ 5.5V Otherwise RC mode only ⁽³⁾ XT, HS and LP modes
D040	VIH	Input High Voltage I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	2.0 0.25 VDD+0.8 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD	— — — — — —	VDD VDD VDD VDD VDD VDD	V V V V V V	4.5V < VDD ≤ 5.5V Otherwise RC mode only ⁽³⁾ XT, HS and LP modes
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 VDD*	—	—	V	
D060	IIL	Input Leakage Current^(1,2) I/O ports MCLR MCLR T0CKI OSC1	-1.0 -5.0 -3.0 -3.0	0.5 — 0.5 0.5 0.5	+1.0 +5.0 +3.0 +3.0 —	μA μA μA μA μA	For VDD ≤ 5.5V: VSS ≤ VPIN ≤ VDD, pin at hi-impedance VPIN = VSS +0.25V VPIN = VDD VSS ≤ VPIN ≤ VDD VSS ≤ VPIN ≤ VDD, XT, HS and LP modes
D080	VOL	Output Low Voltage I/O ports OSC2/CLKOUT	— —	— —	0.6 0.6	V V	IOH = 8.7 mA, VDD = 4.5V IOH = 1.6 mA, VDD = 4.5V, RC mode only
D090	VOH	Output High Voltage⁽²⁾ I/O ports OSC2/CLKOUT	VDD - 0.7 VDD - 0.7	— —	— —	V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, RC mode only

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPIN pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

FIGURE 20-7: WDT TIMER TIME-OUT PERIOD vs. $V_{DD}^{(1)}$

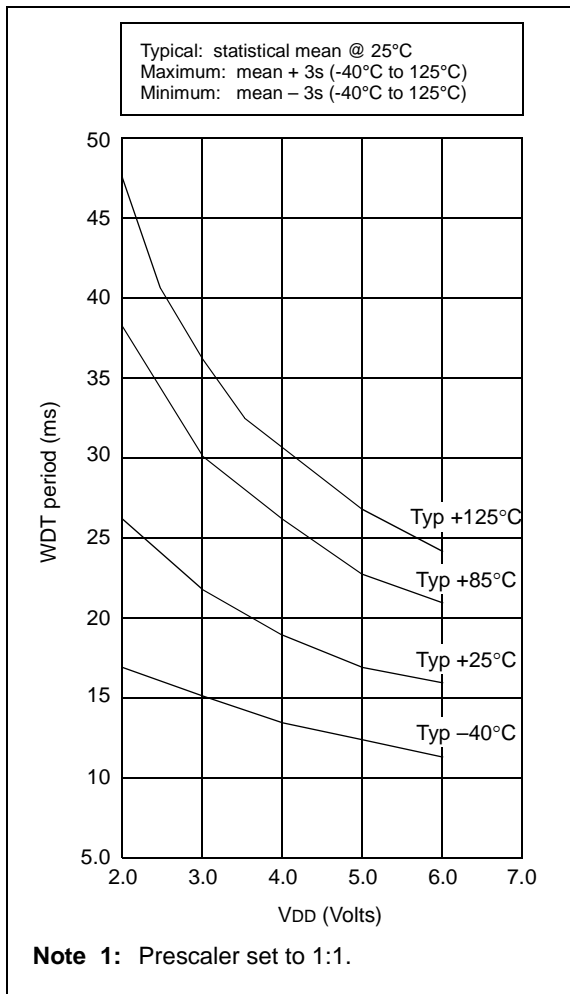


FIGURE 20-8: I_{OH} vs. V_{OH} , $V_{DD} = 5\text{ V}$

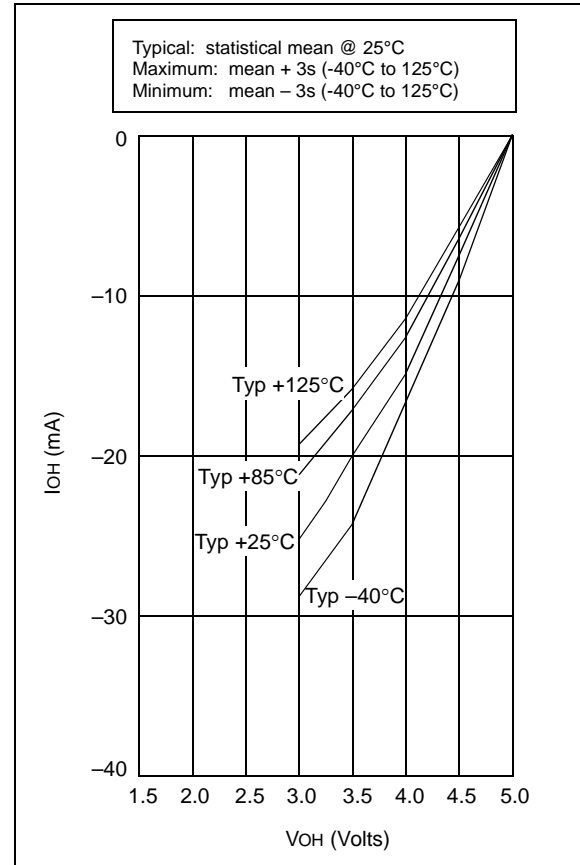


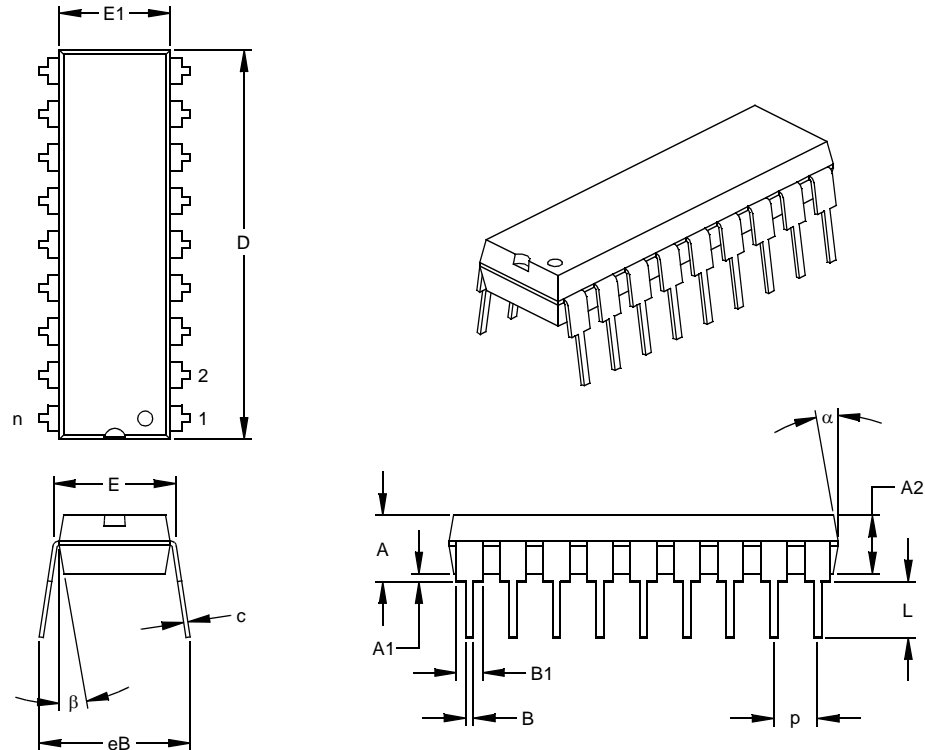
TABLE 20-1: INPUT CAPACITANCE

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
\overline{MCLR}	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of $\pm 25\%$ (three standard deviations) should be taken into account.

18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-007

INDEX

A

Absolute Maximum Ratings	
PIC16C54/55/56/57	67
PIC16C54A	103
PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/ C58B/CR58B	131
PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/ C58B/CR58B-40	155
PIC16CR54A	79
ADDWF	51
ALU	9
ANDLW	51
ANDWF	51
Applications	5
Architectural Overview	9
Assembler	
MPASM Assembler	61

B

Block Diagram	
On-Chip Reset Circuit	20
PIC16C5X Series	10
Timer0	37
TMR0/WDT Prescaler	41
Watchdog Timer	46
Brown-Out Protection Circuit	23
BSF	52
BTFSC	52
BTFSS	52

C

CALL	31, 53
Carry (C) bit	9, 29
Clocking Scheme	13
CLRF	53
CLRW	53
CLRWD	53
CMOS Technology	1
Code Protection	43, 47
COMF	54
Compatibility	182
Configuration Bits	44

D

Data Memory Organization	26
DC Characteristics	
PIC16C54/55/56/57	
Commercial	68, 71
Extended	70, 72
Industrial	69, 71
PIC16C54A	
Commercial	104, 109
Extended	106, 109
Industrial	104, 109
PIC16C54C/C55A/C56A/C57C/C58B-40	
Commercial	157, 158
PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/ C58B/CR58B	
Commercial	134, 138
Extended	137, 138
Industrial	134, 138
PIC16CR54A	
Commercial	80, 83

Extended	82, 84
Industrial	80, 83
PIC16LV54A	
Commercial	108, 109
Industrial	108, 109
DECF	54
DECFSZ	54
Development Support	61
Device Characterization	
PIC16C54/55/56/57/CR54A	91
PIC16C54A	117
PIC16C54C/C55A/C56A/C57C/C58B-40	165
Device Reset Timer (DRT)	23
Device Varieties	7
Digit Carry (DC) bit	9, 29
DRT	23

E

Electrical Specifications	
PIC16C54/55/56/57	67
PIC16C54A	103
PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/ C58B/CR58B	131
PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/ C58B/CR58B-40	155
PIC16CR54A	79
Errata	3
External Power-On Reset Circuit	21

F

Family of Devices	
PIC16C5X	6
FSR Register	33
Value on reset	20

G

General Purpose Registers	
Value on reset	20
GOTO	31, 55

H

High-Performance RISC CPU	1
---------------------------	---

I

I/O Interfacing	35
I/O Ports	35
I/O Programming Considerations	36
ICEPIC In-Circuit Emulator	62
ID Locations	43, 47
INCF	55
INCFSZ	55
INDF Register	33
Value on reset	20
Indirect Data Addressing	33
Instruction Cycle	13
Instruction Flow/Pipelining	13
Instruction Set Summary	49
IORLW	56
IORWF	56

K

KeeLoq Evaluation and Programming Tools	64
---	----

L

Loading of PC	31
---------------	----

PIC16C5X

M

MCLR Reset	
Register values on	20
Memory Map	
PIC16C54/CR54/C55	25
PIC16C56/CR56	25
PIC16C57/CR57/C58/CR58	25
Memory Organization	25
MOVF	56
MOVLW	56
MOVWF	57
MPLAB C17 and MPLAB C18 C Compilers	61
MPLAB ICD In-Circuit Debugger	63
MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE	62
MPLAB Integrated Development Environment Software	61
MPLINK Object Linker/MPLIB Object Librarian	62

N

NOP	57
-----------	----

O

One-Time-Programmable (OTP) Devices	7
OPTION	57
OPTION Register	30
Value on reset	20
Oscillator Configurations	15
Oscillator Types	
HS	15
LP	15
RC	15
XT	15

P

PA0 bit	29
PA1 bit	29
Paging	31
PC	31
Value on reset	20
PD bit	19, 29
Peripheral Features	1
PICDEM 1 Low Cost PIC MCU Demonstration Board	63
PICDEM 17 Demonstration Board	64
PICDEM 2 Low Cost PIC16CXX Demonstration Board	63
PICDEM 3 Low Cost PIC16CXXX Demonstration Board	64
PICSTART Plus Entry Level Development Programmer	63
Pin Configurations	2
Pinout Description - PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58, PIC16CR58	11
Pinout Description - PIC16C55, PIC16C57, PIC16CR57 ...	12
PORTA	35
Value on reset	20
PORTB	35
Value on reset	20
PORTC	35
Value on reset	20
Power-Down Mode	47
Power-On Reset (POR)	21
Register values on	20
Prescaler	40
PRO MATE II Universal Device Programmer	63
Program Counter	31
Program Memory Organization	25
Program Verification/Code Protection	47

Q

Q cycles	13
Quick-Turnaround-Production (QTP) Devices	7

R

RC Oscillator	17
Read Only Memory (ROM) Devices	7
Read-Modify-Write	36
Register File Map	
PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56	26
PIC16C57/CR57	27
PIC16C58/CR58	27
Registers	
Special Function	28
Value on reset	20
Reset	19
Reset on Brown-Out	23
RETLW	57
RLF	58
RRF	58

S

Serialized Quick-Turnaround-Production (SQTP) Devices...	7
SLEEP	43, 47, 58
Software Simulator (MPLAB SIM)	62
Special Features of the CPU	43
Special Function Registers	28
Stack	32
STATUS Register	9, 29
Value on reset	20
SUBWF	59
SWAPF	59

T

Timer0	
Switching Prescaler Assignment	40
Timer0 (TMR0) Module	37
TMR0 register - Value on reset	20
TMR0 with External Clock	39
Timing Diagrams and Specifications	
PIC16C54/55/56/57	74
PIC16C54A	111
PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/ C58B/CR58B	140
PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/ C58B/CR58B-40	160
PIC16CR54A	86
Timing Parameter Symbolology and Load Conditions	
PIC16C54/55/56/57	73
PIC16C54A	110
PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/ C58B/CR58B	139
PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/ C58B/CR58B-40	159
PIC16CR54A	85
TO bit	19, 29
TRIS	59
TRIS Registers	35
Value on reset	20

U

UV Erasable Devices	7
---------------------------	---