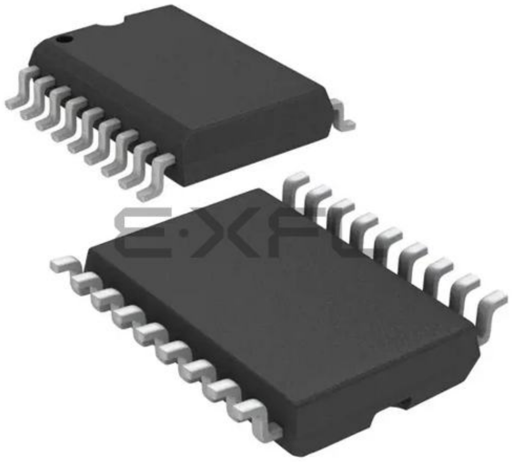
Microchip Technology - PIC16C56-RCI/SO Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c56-rci-so

NOTES:

5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the $\overline{\text{MCLR}}$/VPP pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is RESET. The DRT timer begins counting once it detects $\overline{\text{MCLR}}$ to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where $\overline{\text{MCLR}}$ is not tied to VDD is shown in Figure 5-3. VDD is allowed to rise and stabilize before bringing $\overline{\text{MCLR}}$ high. The chip will actually come out of reset TDRT msec after $\overline{\text{MCLR}}$ goes high.

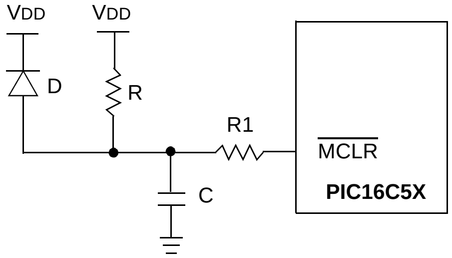
In Figure 5-4, the on-chip Power-On Reset feature is being used ($\overline{\text{MCLR}}$ and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the $\overline{\text{MCLR}}$/VPP pin, and when the $\overline{\text{MCLR}}$/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

Note:	When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the Embedded Control Handbook.

The POR circuit does not produce an internal RESET when VDD declines.

FIGURE 5-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{\text{MCLR}}$ from external capacitor C in the event of $\overline{\text{MCLR}}$ pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

6.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers and General Purpose Registers.

The Special Function Registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Purpose Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

For the PIC16C54, PIC16CR54, PIC16C56 and PIC16CR56, the register file is composed of 7 Special Function Registers and 25 General Purpose Registers (Figure 6-4).

For the PIC16C55, the register file is composed of 8 Special Function Registers and 24 General Purpose Registers.

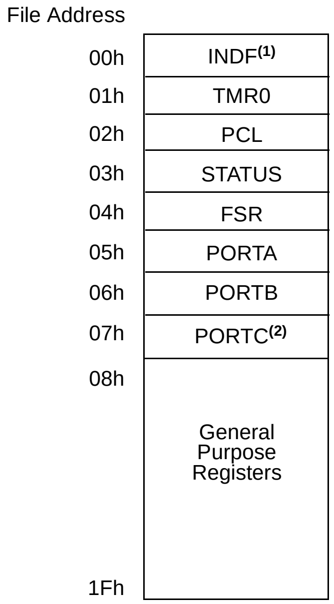
For the PIC16C57 and PIC16CR57, the register file is composed of 8 Special Function Registers, 24 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-5).

For the PIC16C58 and PIC16CR58, the register file is composed of 7 Special Function Registers, 25 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-6).

6.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the File Select Register (FSR). The FSR Register is described in Section 6.7.

FIGURE 6-4: PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56 REGISTER FILE MAP



File Address	
00h	INDF[1]
01h	TMR0
02h	PCL
03h	STATUS
04h	FSR
05h	PORTA
06h	PORTB
07h	PORTC[2]
08h 1Fh	General Purpose Registers

Note 1: Not a physical register. See Section 6.7.

2: PIC16C55 only, in all other devices this is implemented as a a general purpose register.

REGISTER 9-2: CONFIGURATION WORD FOR PIC16C54/C55/C56/C57

—	—	—	—	—	—	—	—	CP	WDTE	FOSC1	FOSC0
bit 11											bit 0

bit 11-4: **Unimplemented**: Read as ‘0’

bit 3: **CP:** Code protection bit.
`1` = Code protection off
`0` = Code protection on

bit 2: **WDTE:** Watchdog timer enable bit
`1` = WDT enabled
`0` = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator selection bits[2]
`00` = LP oscillator
`01` = XT oscillator
`10` = HS oscillator
`11` = RC oscillator

Note 1: Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

2: PIC16LV54A supports XT, RC and LP oscillator only.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

NOTES:

11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for pre-compiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

11.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

11.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows environment were chosen to best make these features available to you, the end user.

11.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

<table>
<tr><td colspan="3">PIC16LCR54A-04
PIC16LCR54A-04I
(Commercial, Industrial)</td><td colspan="5">Standard Operating Conditions (unless otherwise specified)
Operating Temperature 0°C ≤ TA ≤ +70°C for commercial
–40°C ≤ TA ≤ +85°C for industrial</td></tr>
<tr><td colspan="3">PIC16CR54A-04, 10, 20
PIC16CR54A-04I, 10I, 20I
(Commercial, Industrial)</td><td colspan="5">Standard Operating Conditions (unless otherwise specified)
Operating Temperature 0°C ≤ TA ≤ +70°C for commercial
–40°C ≤ TA ≤ +85°C for industrial</td></tr>
<tr><th>Param No.</th><th>Symbol</th><th>Characteristic/Device</th><th>Min</th><th>Typ†</th><th>Max</th><th>Units</th><th>Conditions</th></tr>
<tr><td></td><td>VDD</td><td colspan="6">Supply Voltage</td></tr>
<tr><td>D001</td><td></td><td>PIC16LCR54A</td><td>2.0</td><td>—</td><td>6.25</td><td>V</td><td></td></tr>
<tr><td>D001
D001A</td><td></td><td>PIC16CR54A</td><td>2.5
4.5</td><td>—
—</td><td>6.25
5.5</td><td>V
V</td><td>RC and XT modes
HS mode</td></tr>
<tr><td>D002</td><td>VDR</td><td>RAM Data Retention Voltage(1)</td><td>—</td><td>1.5*</td><td>—</td><td>V</td><td>Device in SLEEP mode</td></tr>
<tr><td>D003</td><td>VPOR</td><td>VDD Start Voltage to ensure Power-on Reset</td><td>—</td><td>VSS</td><td>—</td><td>V</td><td>See Section 5.1 for details on Power-on Reset</td></tr>
<tr><td>D004</td><td>SVDD</td><td>VDD Rise Rate to ensure Power-on Reset</td><td>0.05*</td><td>—</td><td>—</td><td>V/ms</td><td>See Section 5.1 for details on Power-on Reset</td></tr>
<tr><td></td><td>IDD</td><td colspan="6">Supply Current(2)</td></tr>
<tr><td>D005</td><td></td><td>PICLCR54A</td><td>—
—</td><td>10
—</td><td>20
70</td><td>μA
μA</td><td>Fosc = 32 kHz, VDD = 2.0V
Fosc = 32 kHz, VDD = 6.0V</td></tr>
<tr><td>D005A</td><td></td><td></td><td></td><td></td><td></td><td></td><td>RC(3) and XT modes:</td></tr>
<tr><td></td><td></td><td>PIC16CR54A</td><td>—
—
—</td><td>2.0
0.8
90</td><td>3.6
1.8
350</td><td>mA
mA
μA</td><td>FOSC = 4.0 MHz, VDD = 6.0V
FOSC = 4.0 MHz, VDD = 3.0V
FOSC = 200 kHz, VDD = 2.5V</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>HS mode:</td></tr>
<tr><td></td><td></td><td></td><td>—
—</td><td>4.8
9.0</td><td>10
20</td><td>mA
mA</td><td>FOSC = 10 MHz, VDD = 5.5V
FOSC = 20 MHz, VDD = 5.5V</td></tr>
</table>

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

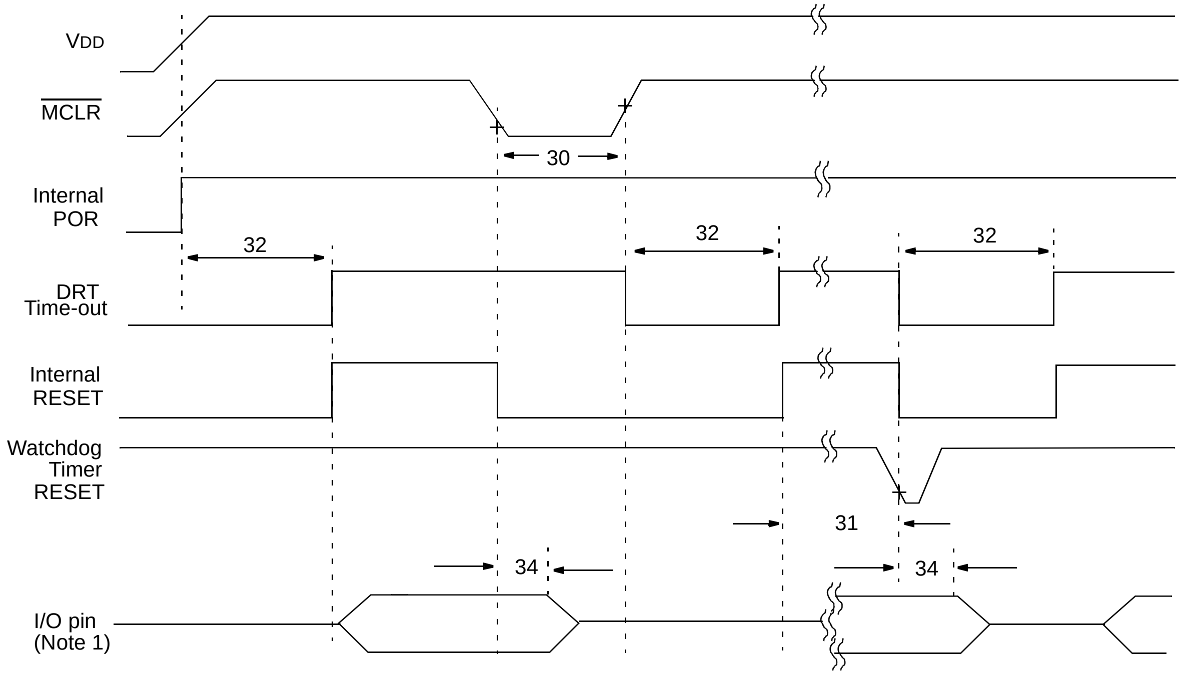
2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

FIGURE 13-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR54A



Note 1: Please refer to Figure 13.1 for load conditions.

TABLE 13-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial –40°C ≤ TA ≤ +125°C for extended					
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	1.0*	—	—	μs	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7.0*	18*	40*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	7.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	—	—	1.0*	μs	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 14-2: TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 20 PF

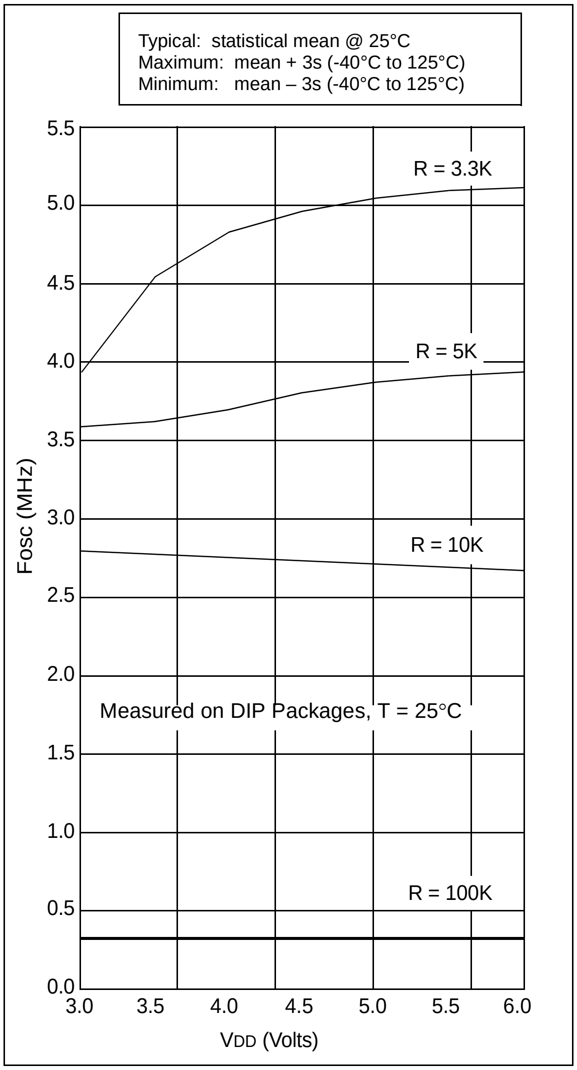


FIGURE 14-3: TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 100 PF

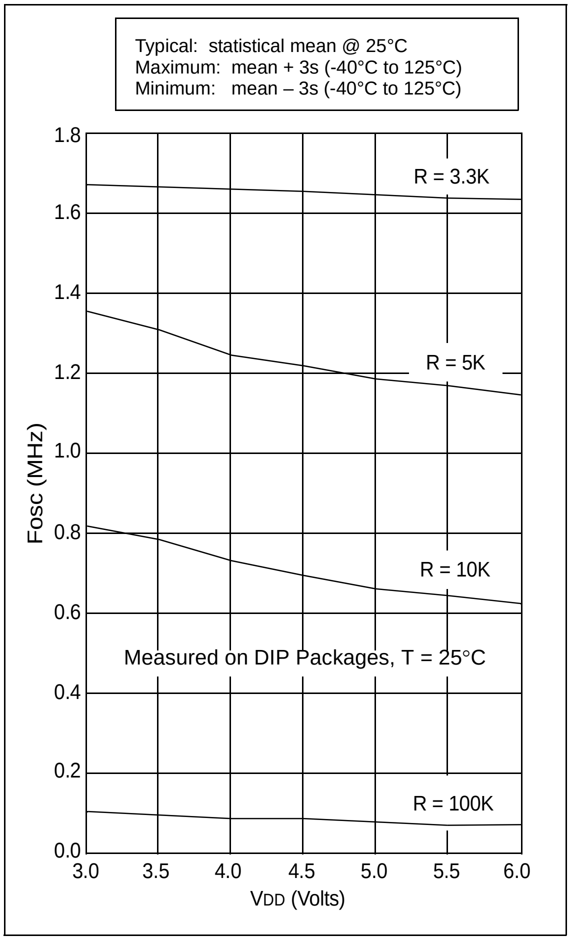


FIGURE 14-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED

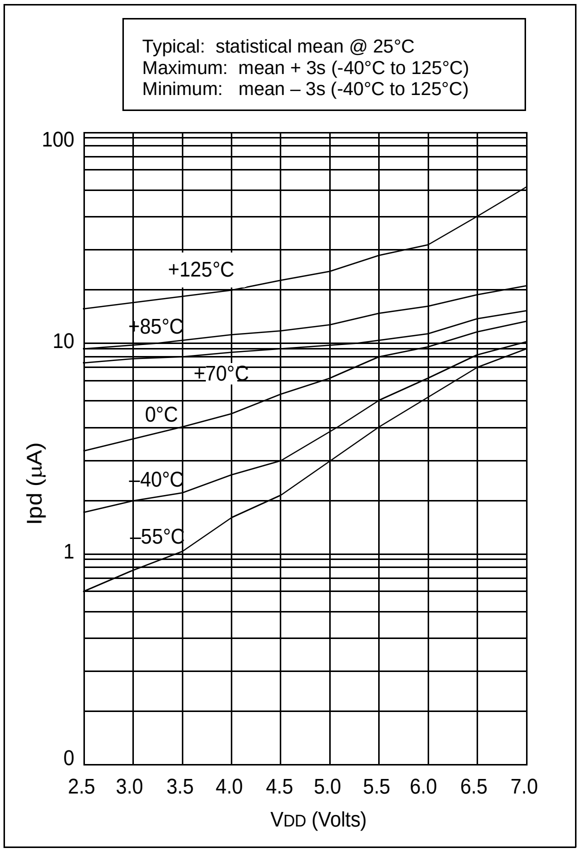


FIGURE 14-7: TYPICAL IPD vs. VDD, WATCHDOG ENABLED

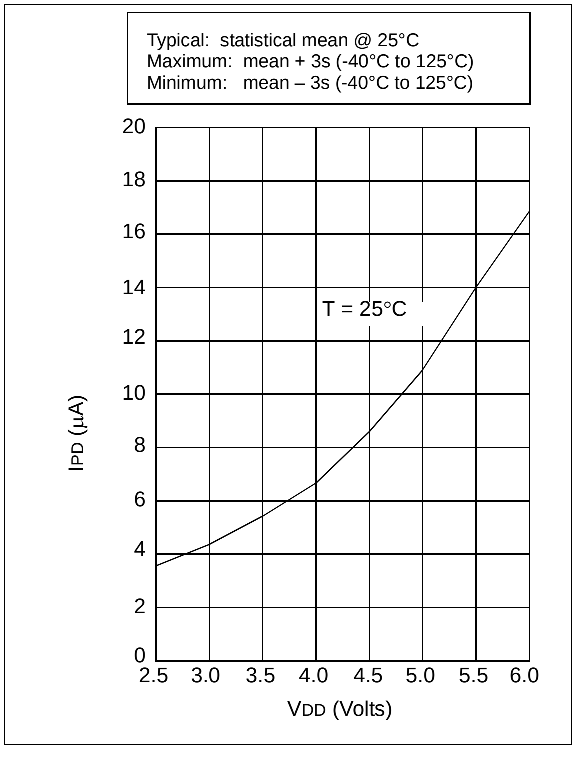
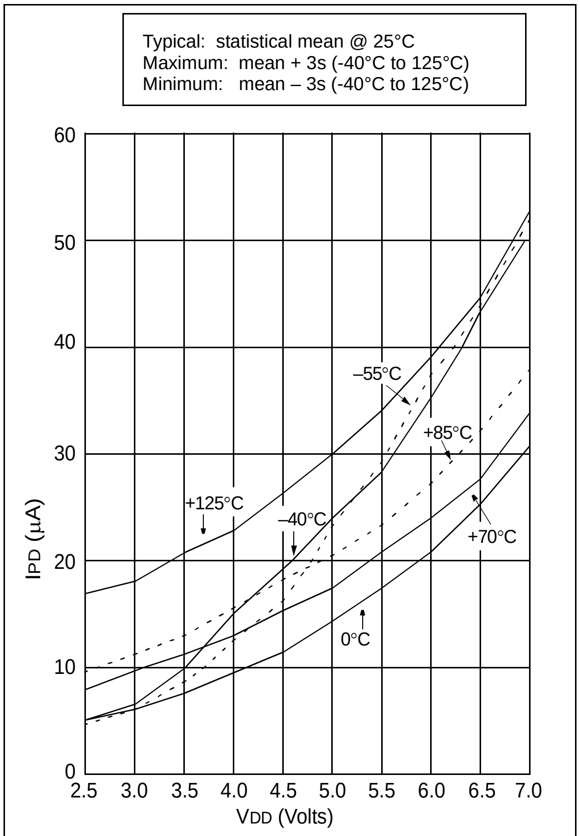


FIGURE 14-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED



IPD, with WDT enabled, has two components:
The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At –40°C, the latter dominates explaining the apparently anomalous behavior.

FIGURE 14-13: MAXIMUM IDD VS. FREQUENCY (EXTERNAL CLOCK, –40°C TO +85°C)

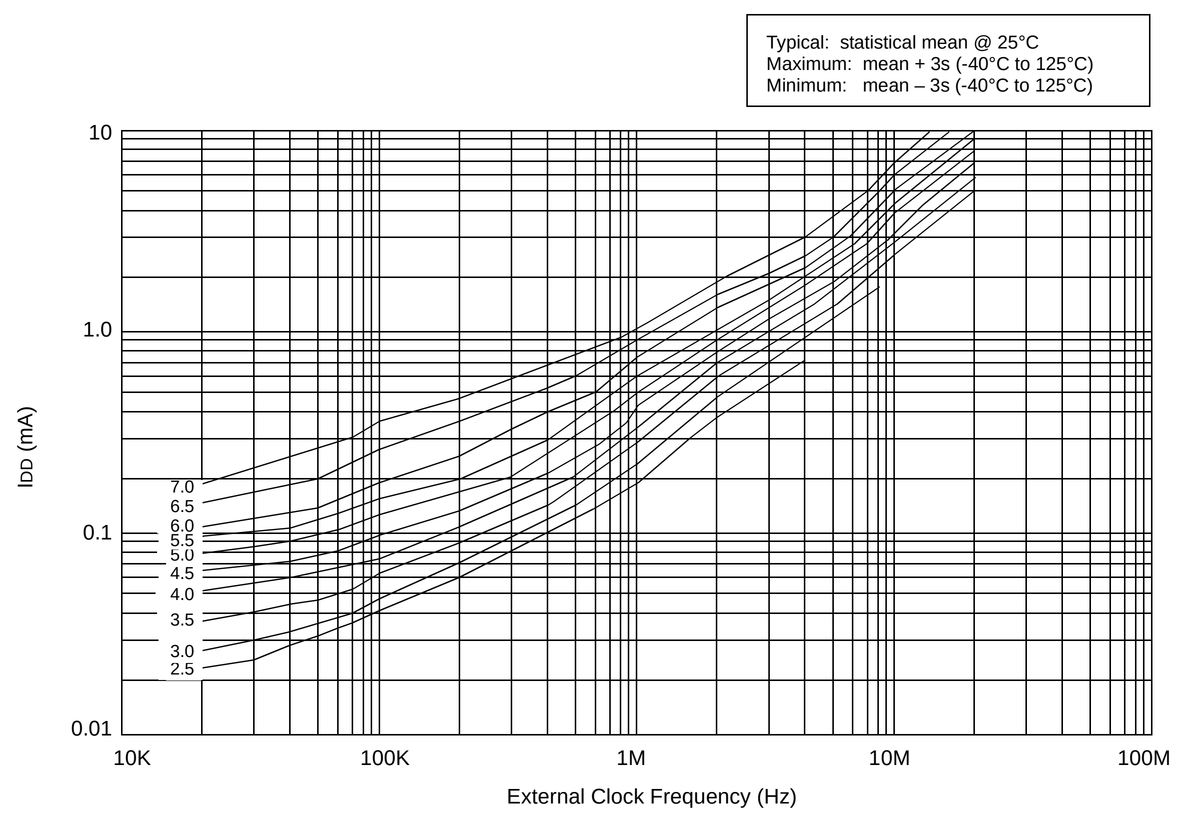


FIGURE 14-14: MAXIMUM IDD VS. FREQUENCY (EXTERNAL CLOCK –55°C TO +125°C)

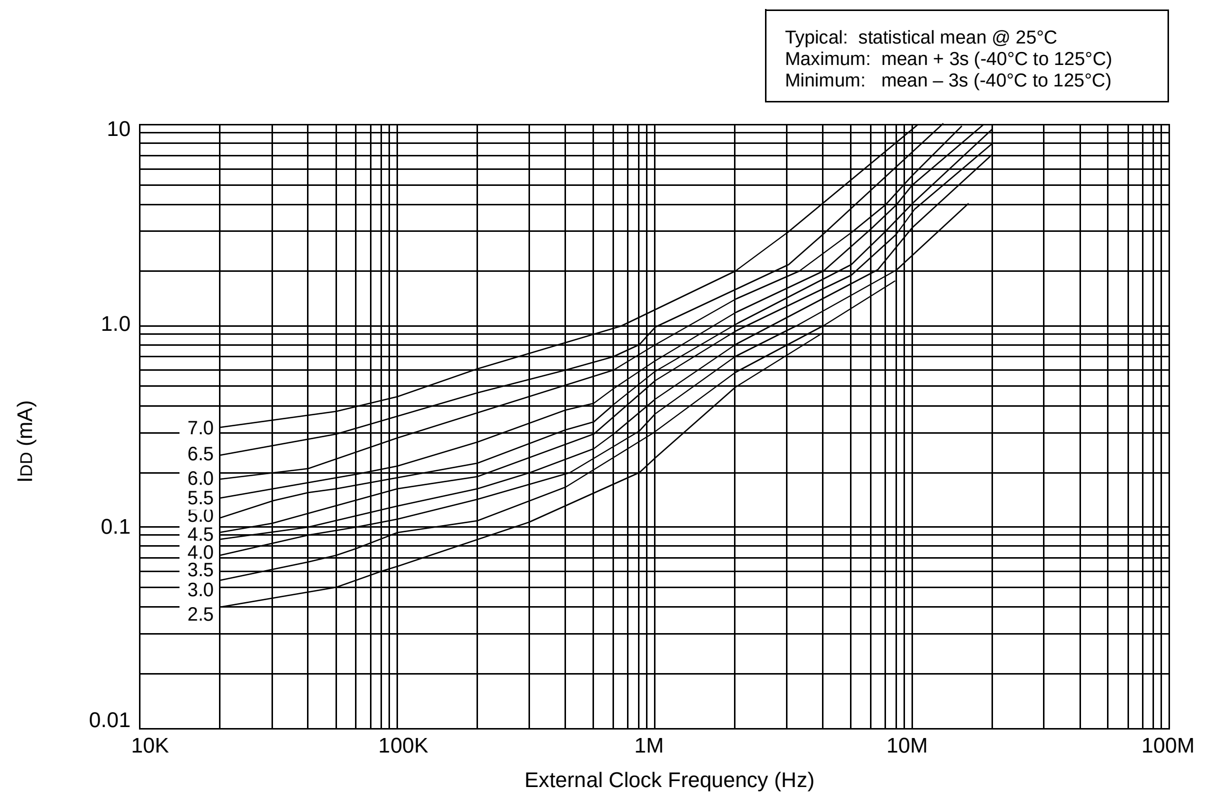


FIGURE 14-21: PORTA, B AND C IOL vs. VOL, VDD = 3 V

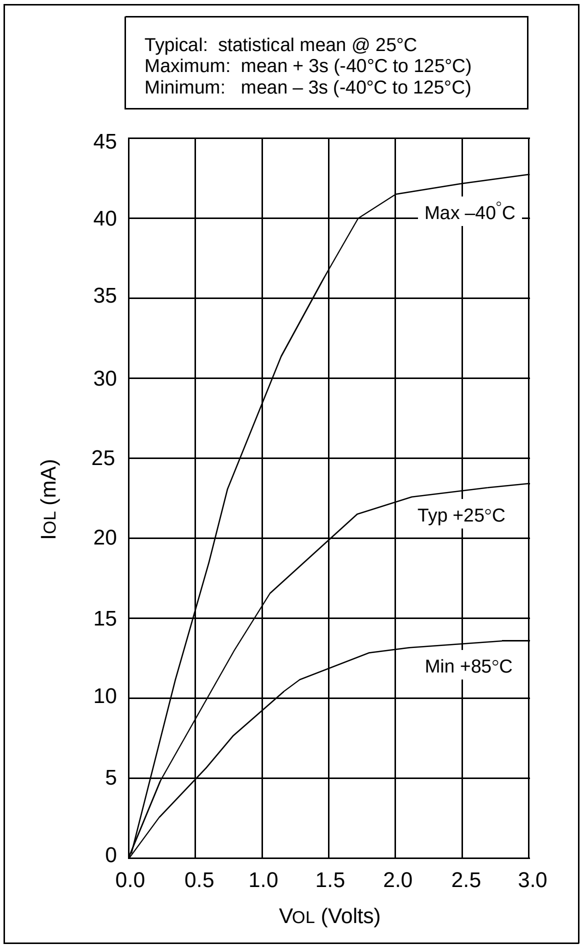


FIGURE 14-22: PORTA, B AND C IOL vs. VOL, VDD = 5 V

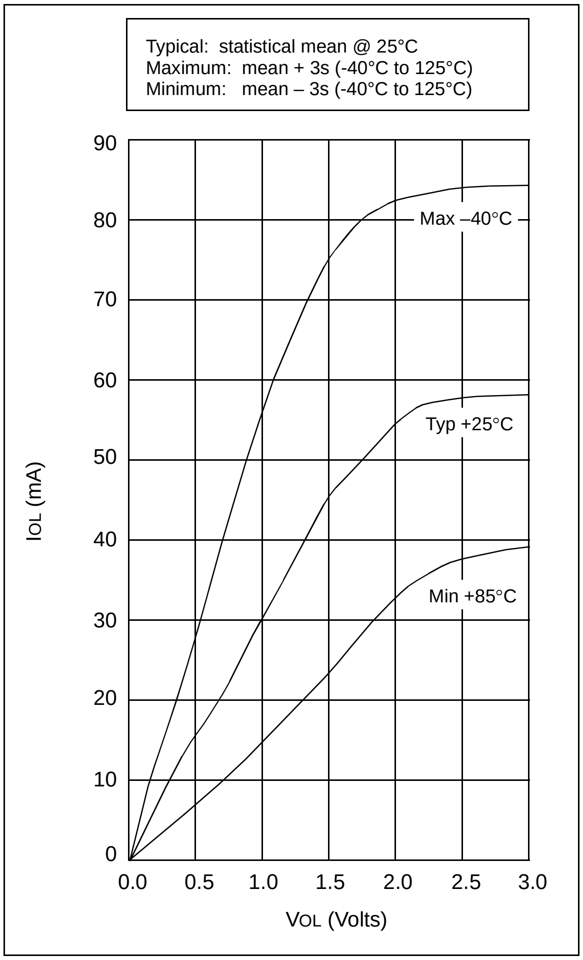


TABLE 14-2: INPUT CAPACITANCE FOR PIC16C54/56

Pin	Typical Capacitance (pF)	
	18L PDIP	**18L SOIC**
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{\text{MCLR}}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

TABLE 14-3: INPUT CAPACITANCE FOR PIC16C55/57

Pin	Typical Capacitance (pF)	
	28L PDIP (600 mil)	**28L SOIC**
RA port	5.2	4.8
RB port	5.6	4.7
RC port	5.0	4.1
$\overline{\text{MCLR}}$	17.0	17.0
OSC1	6.6	3.5
OSC2/CLKOUT	4.6	3.5
T0CKI	4.5	3.5

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial –20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I –40°C ≤ TA ≤ +125°C for extended						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
1	TOSC	External CLKIN Period[1]	250	—	—	ns	XT OSC mode
			500	—	—	ns	XT OSC mode (PIC16LV54A)
			250	—	—	ns	HS OSC mode (04)
			100	—	—	ns	HS OSC mode (10)
			50	—	—	ns	HS OSC mode (20)
			5.0	—	—	μs	LP OSC mode
		Oscillator Period[1]	250	—	—	ns	RC OSC mode
			500	—	—	ns	RC OSC mode (PIC16LV54A)
			250	—	10,000	ns	XT OSC mode
			500	—	—	ns	XT OSC mode (PIC16LV54A)
			250	—	250	ns	HS OSC mode (04)
			100	—	250	ns	HS OSC mode (10)
			50	—	250	ns	HS OSC mode (20)
			5.0	—	200	μs	LP OSC mode
2	Tcy	Instruction Cycle Time[2]	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

† Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

18.0 DEVICE CHARACTERIZATION - PIC16LC54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean – 3σ) respectively, where σ is a standard deviation, over the whole temperature range.

FIGURE 18-1: TYPICAL RC OSCILLATOR FREQUENCY VS. TEMPERATURE

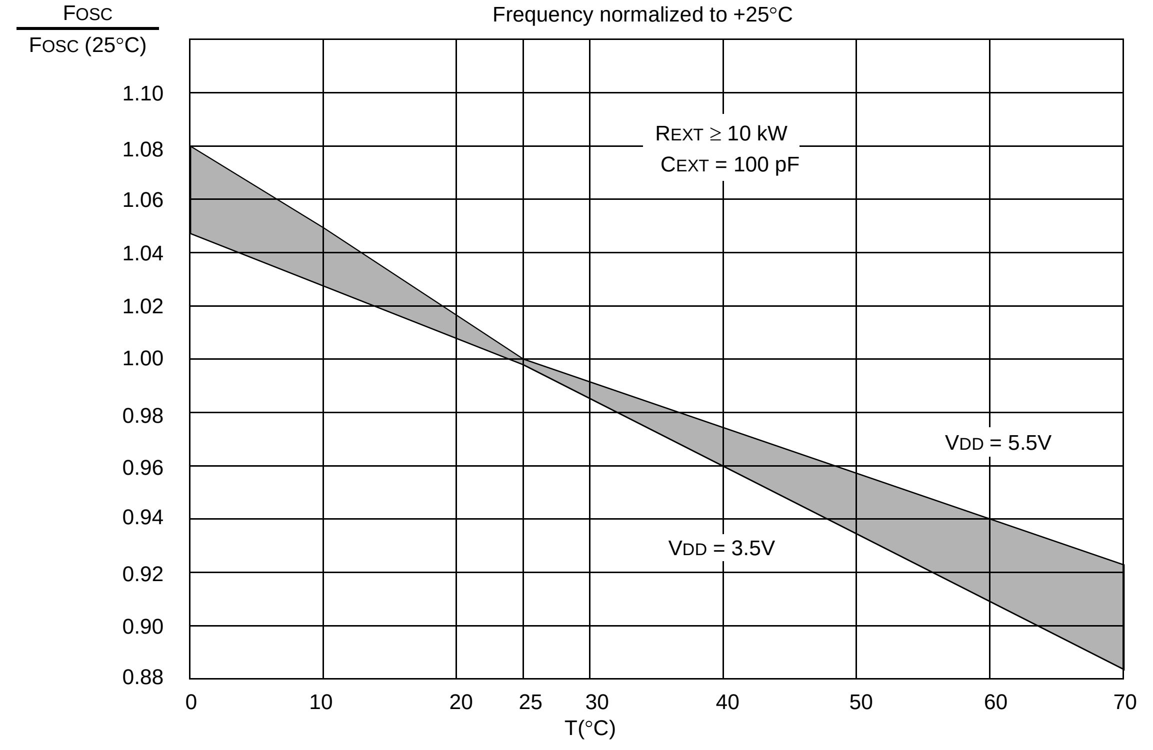


TABLE 18-1: RC OSCILLATOR FREQUENCIES

CEXT	REXT	Average Fosc @ 5V, 25°C	
20 pF	3.3K	5 MHz	± 27%
	5K	3.8 MHz	± 21%
	10K	2.2 MHz	± 21%
	100K	262 kHz	± 31%
100 pF	3.3K	1.63 MHz	± 13%
	5K	1.2 MHz	± 13%
	10K	684 kHz	± 18%
	100K	71 kHz	± 25%
300 pF	3.3K	660 kHz	± 10%
	5.0K	484 kHz	± 14%
	10K	267 kHz	± 15%
	100K	29 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5V.

FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF, 25°C

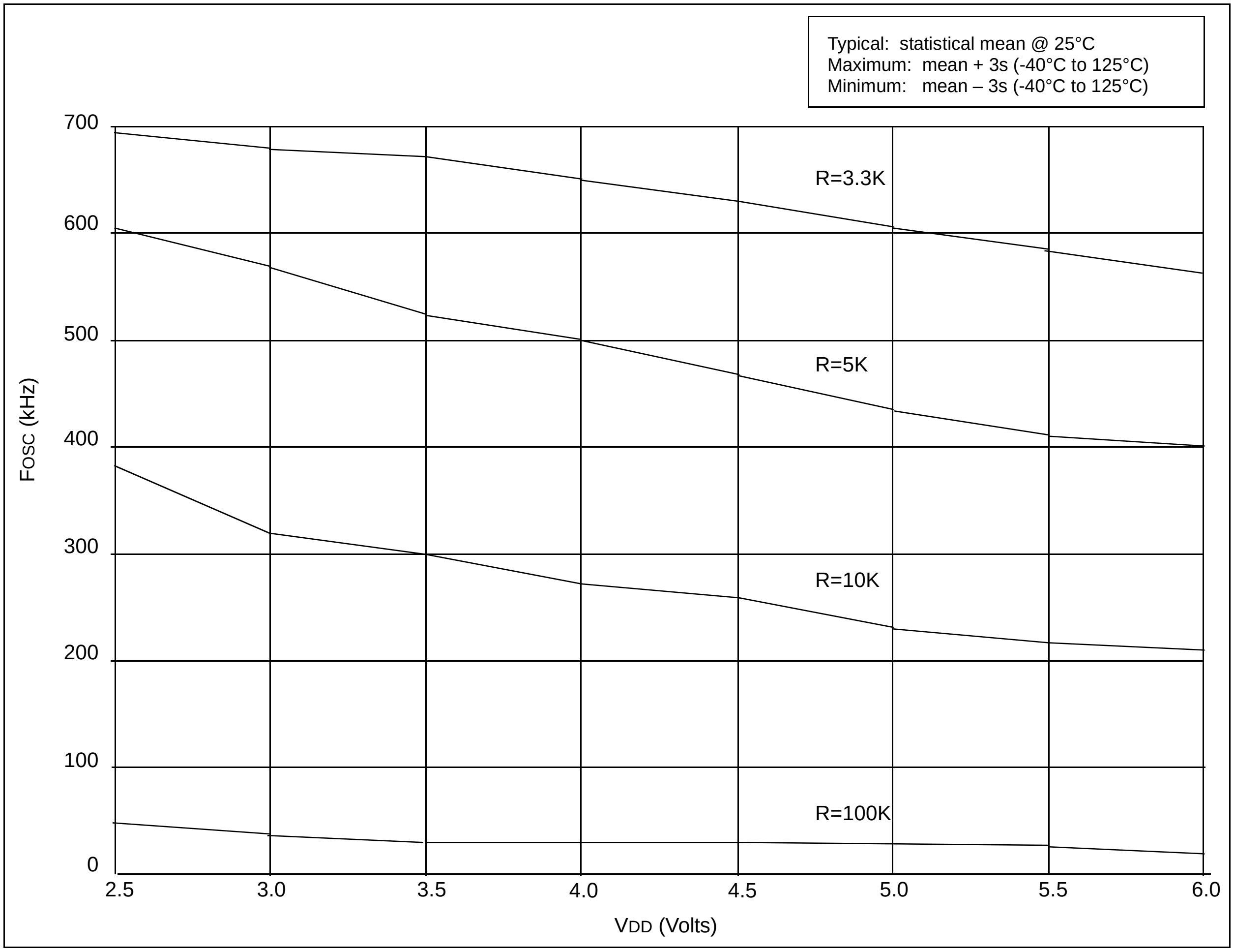
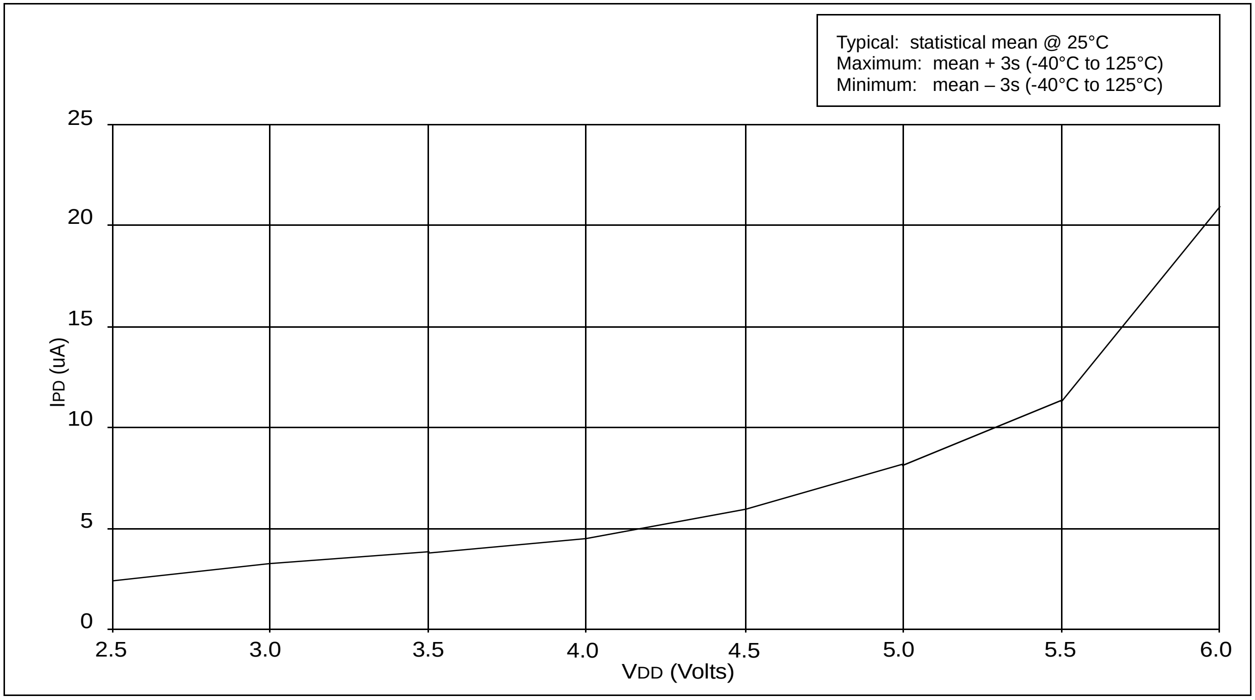


FIGURE 18-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)



19.4 Timing Diagrams and Specifications

FIGURE 19-3: EXTERNAL CLOCK TIMING - PIC16C5X-40

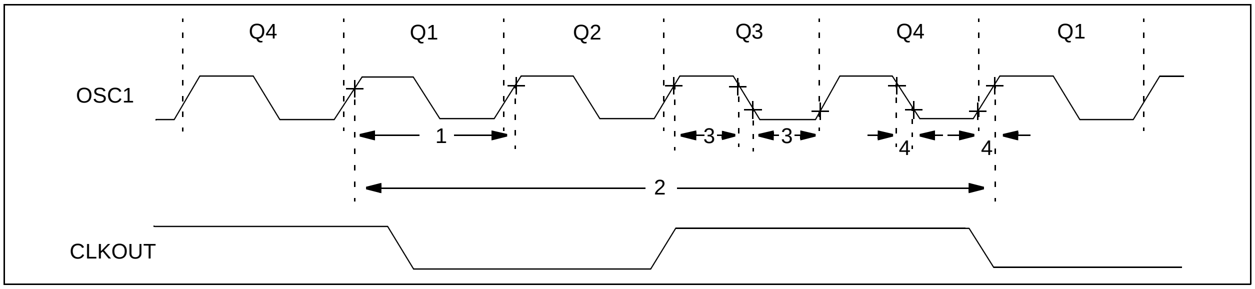


TABLE 19-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X-40

AC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial					
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	FOSC	External CLKIN Frequency(1)	20	—	40	MHz	HS OSC mode
1	TOSC	External CLKIN Period(1)	25	—	—	ns	HS OSC mode
2	Tcy	Instruction Cycle Time(2)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	6.0*	—	—	ns	HS oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	6.5*	ns	HS oscillator

* These parameters are characterized but not tested.

† Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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Device: **PIC16C5X**
Literature Number: **DS30453E**

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-	XX	X	/XX	XXX
Device		Frequency Range/OSC Type	Temperature Range	Package	Pattern

Device	PIC16C54 PIC16C54A PIC16CR54A PIC16C54C PIC16CR54C PIC16C55 PIC16C55A PIC16C56 PIC16C56A PIC16CR56A PIC16C57 PIC16C57C PIC16CR57C PIC16C58B PIC16CR58B	PIC16C54T(2) PIC16C54AT(2) PIC16CR54AT(2) PIC16C54CT(2) PIC16CR54CT(2) PIC16C55T(2) PIC16C55AT(2) PIC16C56T(2) PIC16C56AT(2) PIC16CR56AT(2) PIC16C57T(2) PIC16C57CT(2) PIC16CR57CT(2) PIC16C58BT(2) PIC16CR58BT(2)

Frequency Range/ Oscillator Type	RC	Resistor Capacitor
	LP	Low Power Crystal
	XT	Standard Crystal/Resonator
	HS	High Speed Crystal
	02	200 KHz (LP) or 2 MHz (XT and RC)
	04	200 KHz (LP) or 4 MHz (XT and RC)
	10	10 MHz (HS only)
	20	20 MHz (HS only)
	40	40 MHz (HS only)
	b(4)	No oscillator type for JW packages(3)

*RC/LP/XT/HS are for 16C54/55/56/57 devices only
-02 is available for 16LV54A only
-04/10/20 options are available for all other devices
-40 is available for 16C54C/55A/56A/57C/58B devices only

Temperature Range	b(4)	=	0°C	to	+70°C
	I	=	-40°C	to	+85°C
	E	=	-40°C	to	+125°C

Package	S	=	Die in Waffle Pack
	JW	=	28-pin 600 mil/18-pin 300 mil windowed CERDIP(3)
	P	=	28-pin 600 mil/18-pin 300 mil PDIP
	SO	=	300 mil SOIC
	SS	=	209 mil SSOP
	SP	=	28-pin 300 mil Skinny PDIP

*See Section 21 for additional package information.

Pattern	QTP, SQTP, ROM code (factory specified) or Special Requirements. Blank for OTP and Windowed devices.

Examples:

a) PIC16C55A - 04/P 301 = Commercial Temp., PDIP package, 4 MHz, standard VDD limits, QTP pattern #301
b) PIC16LC54C - 04I/SO Industrial Temp., SOIC package, 200 kHz, extended VDD limits
c) PIC16C57 - RC/SP = RC Oscillator, commercial temp, skinny PDIP package, 4 MHz, standard VDD limits
d) PIC16C58BT -40/SS 123 = commercial temp, SSOP package in tape and reel, 4 MHz, extended VDD limits, ROM pattern #123

Note 1: C = normal voltage range
LC = extended
2: T = in tape and reel - SOIC and SSOP packages only
3: JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirements of each oscillator type, including LC devices.
4: b = Blank

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