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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c56-rci-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pi	n Numb	er	Pin	Buffer	Description
DIP	SOIC	SSOP	Туре	Туре	Description
17	17	19	I/O	TTL	Bi-directional I/O port
18	18	20	I/O	TTL	
1	1	1	I/O	TTL	
2	2	2	I/O	TTL	
6	6	7	I/O	TTL	Bi-directional I/O port
7	7	8	I/O	TTL	
8	8	9	I/O	TTL	
9	9	10	I/O	TTL	
10	10	11	I/O	TTL	
11	11	12	I/O	TTL	
12	12	13	I/O	TTL	
13	13	14	I/O	TTL	
3	3	3	Ι	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in
					use, to reduce current consumption.
4	4	4	Ι	ST	Master clear (RESET) input/programming voltage input.
					This pin is an active low RESET to the device. Voltage on
					the MCLR/VPP pin must not exceed VDD to avoid unin-
					tended entering of Programming mode.
16	16	18	I	ST	Oscillator crystal input/external clock source input.
15	15	17	0	_	Oscillator crystal output. Connects to crystal or resonator
					in crystal Oscillator mode. In RC mode, OSC2 pin outputs
					CLKOUT, which has 1/4 the frequency of OSC1 and
					denotes the instruction cycle rate.
14	14	15,16	Р	_	Positive supply for logic and I/O pins.
5	5	5,6	Р	—	Ground reference for logic and I/O pins.
	Pi DIP 17 18 1 2 6 7 8 9 10 11 12 13 3 3 4 16 15	Pin Numb   DIP SOIC   17 17   18 18   1 1   2 2   6 6   7 7   8 8   9 9   10 10   11 11   12 12   13 13   3 3   4 4   16 16   15 15   14 14	Pin Number   DIP SOIC SSOP   17 17 19   18 18 20   1 1 1   2 2 2   6 6 7   7 7 8   8 8 9   9 9 10   10 10 11   11 11 12   12 12 13   13 13 14   3 3 3   4 4 4   15 15 17   14 14 15,16	Pin Pin   DIP SOIC SSOP Type   17 17 19 I/O   18 18 20 I/O   1 1 1 I/O   2 2 2 I/O   6 6 7 I/O   7 7 8 I/O   8 9 I/O I/O   9 9 10 I/O   10 10 11 I/O   11 11 12 I/O   12 12 13 I/O   13 13 14 I/O   3 3 3 I   16 16 18 I   15 15 17 O   14 14 15,16 P	Pin Buffer   DIP SOIC SSOP Type Type   17 17 19 I/O TTL   18 18 20 I/O TTL   1 1 1/O TTL   2 2 2 I/O TTL   6 6 7 I/O TTL   7 7 8 I/O TTL   9 9 10 I/O TTL   10 10 11 I/O TTL   11 11 12 I/O TTL   9 9 10 I/O TTL   10 10 11 I/O TTL   12 12 13 I/O TTL   13 13 14 I/O TTL   3 3 3 I ST   16 16 18 I ST   15 15 17 <td< td=""></td<>

# TABLE 3-1:PINOUT DESCRIPTION - PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16CR58,<br/>PIC16CR58

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

#### 5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the MCLR/VPP pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is <u>RESET</u>. The DRT timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where MCLR is not tied to VDD is shown in Figure 5-3. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset TDRT msec after MCLR goes high.

In Figure 5-4, the on-chip Power-On Reset feature is being used (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the MCLR/VPP pin, and when the MCLR/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

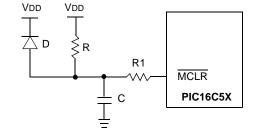
Note: When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see Power-Up Considerations AN522 in the <u>Embedded Control</u> <u>Handbook</u>.

The POR circuit does not produce an internal RESET when VDD declines.

#### FIGURE 5-2:

#### EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 =  $100\Omega$  to 1 k $\Omega$  will limit any current flowing into  $\overline{MCLR}$  from external capacitor C in the event of  $\overline{MCLR}$  pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

## 5.2 Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides an 18 ms nominal time-out on RESET regardless of Oscillator mode used. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows VDD to rise above VDD min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after the voltage on the MCLR/VPP pin has reached a logic high (VIH) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The Device Reset time delay will vary from chip to chip due to VDD, temperature, and process variation. See AC parameters for details.

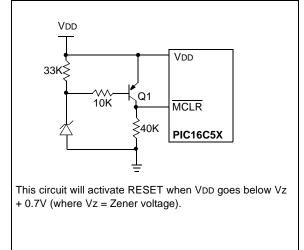
The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the PIC16C5X from SLEEP mode automatically.

## 5.3 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be RESET in the event of a brown-out.

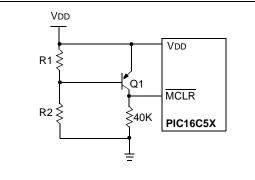
To RESET PIC16C5X devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 5-6, Figure 5-7 and Figure 5-8.





#### FIGURE 5-7:

#### EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2

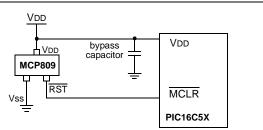


This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

#### FIGURE 5-8:

#### EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX families of supervisors provide push-pull and open collector outputs with both "active high and active low" RESET pins. There are 7 different trip point selections to accommodate 5V and 3V systems. NOTES:

# 7.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., **MOPOREW**) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

# 7.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used (RA<3:0>). Bits 7-4 are unimplemented and read as '0's.

# 7.2 PORTB

PORTB is an 8-bit I/O Register (PORTB<7:0>).

# 7.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16CR56, PIC16CR56, PIC16CS8 and PIC16CR58.

# 7.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the

**KS f** instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

Note:	A read of the ports reads the pins, not the
	output data latches. That is, if an output
	driver on a pin is enabled and driven high,
	but the external system is holding it low, a
	read of the port will indicate that the pin is
	low.

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

TABLE 7-1:	SUMMARY OF PORT REGISTERS

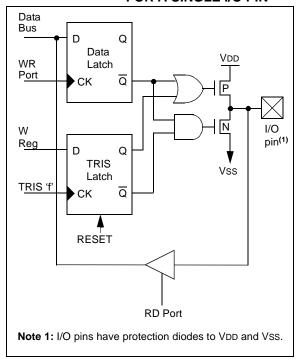
#### Value on Value on Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 MCLR and Address Name Bit 7 Bit 6 Power-On Reset WDT Reset TRIS N/A I/O Control Registers (TRISA, TRISB, TRISC) 1111 1111 1111 1111 05h PORTA RA3 RA2 RA1 RA0 ---- xxxx uuuu PORTB 06h RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0 XXXX XXXX นนนน นนนน 07h PORTC RC7 RC6 RC5 RC4 RC3 RC2 RC1 RC0 XXXX XXXX น่นนน นนนน

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'

## 7.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 7-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., **MOPORE**, **W**). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

#### FIGURE 7-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



# 9.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT Reset or Wake-up Reset generates a device RESET.

The  $\overline{\text{TO}}$  bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset (Section 6.3).

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 9.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

#### 9.2.1 WDT PERIOD

An 8-bit counter is available as a prescaler for the Timer0 module (Section 8.2), or as a postscaler for the Watchdog Timer (WDT), respectively. For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not

both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio (Section 6.4).

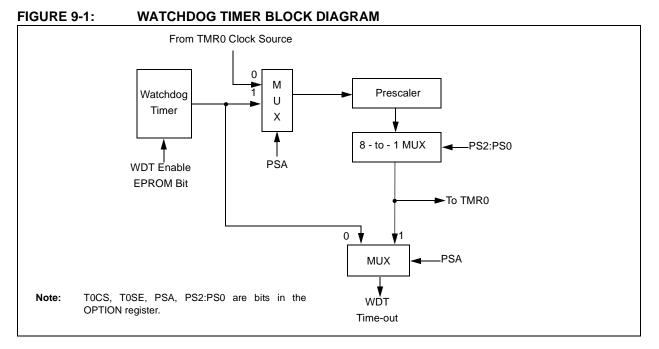
The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see Device Characterization).

Under worst case conditions (VDD = Min., Temperature = Max., WDT prescaler = 1:128), it may take several seconds before a WDT time-out occurs.

#### 9.2.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction RESETS the WDT and the prescaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.



#### TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	<u>Value</u> on MCLR and WDT Reset
N/A	OPTION	—		Tosc	Tose	PSA	PS2	PS1	PS0	11 1111	11 1111

Legend: u = unchanged, - = unimplemented, read as '0'. Shaded cells not used by Watchdog Timer.

ADDWF	Add W	and f		
Syntax:	[ label ] A	DDWF	f,d	
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$			
Operation:	(W) + (f)	$\rightarrow$ (dest)		
Status Affected:	C, DC, Z			
Encoding:	0001	11df	ffff	
Description:	and regis	ster 'f'. If 'd in the W sult is sto	of the W r d' is 0 the register. I red back	result f 'd' is
Words:	1			
Cycles:	1			
Example:	ADDWF	TEMP_RE	G, 0	
Before Instr W TEMP_I After Instruc W TEMP_F	= REG = ction =	0x17 0xC2 0xD9 0xC2		

ANDWF	AND W with f
Syntax:	[ label ] ANDWF f,d
Operands:	$\begin{array}{l} 0\leq f\leq 31\\ d\in [0,1] \end{array}$
Operation:	(W) .AND. (f) $\rightarrow$ (dest)
Status Affected:	Z
Encoding:	0001 01df ffff
Description:	The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W regis- ter. If 'd' is '1' the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	ANDWF TEMP_REG, 1
Before Instru W TEMP_ After Instruc W TEMP_	= 0x17 REG = 0xC2 tion = 0x17

ANDLW	AND literal with W				
Syntax:	[ <i>label</i> ] ANDLW k				
Operands:	$0 \le k \le 255$				
Operation:	(W).AND. (k) $\rightarrow$ (W)				
Status Affected:	Z				
Encoding:	1110 kkkk kkkk				
Description:	The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W regis- ter.				
Words:	1				
Cycles:	1				
Example:	ANDLW H'5F'				
Before Instru W = After Instruc W =	0xA3				

BCF	Bit Clea	r f				
Syntax:	[ label ]	[label] BCF f,b				
Operands:		$\begin{array}{l} 0 \leq f \leq 31 \\ 0 \leq b \leq 7 \end{array}$				
Operation:	$0 \rightarrow (f < b$	>)				
Status Affected:	None					
Encoding:	0100	bbbf	ffff			
Description:	Bit 'b' in i	register 'f'	is cleared.			
Words:	1					
Cycles:	1					
Example:	BCF	FLAG_RE	IG, 7			
Before Instruction FLAG_REG = 0xC7 After Instruction						
FLAG_F	REG =	0x47				

# 11.0 DEVELOPMENT SUPPORT

The PIC<sup>®</sup> microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB<sup>®</sup> IDE Software
- Assemblers/Compilers/Linkers
  - MPASM<sup>™</sup> Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/
  - MPLIB<sup>™</sup> Object Librarian
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - ICEPIC<sup>™</sup> In-Circuit Emulator
- In-Circuit Debugger
- MPLAB ICD
- Device Programmers
  - PRO MATE<sup>®</sup> II Universal Device Programmer
- PICSTART<sup>®</sup> Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
  - PICDEM<sup>™</sup>1 Demonstration Board
  - PICDEM 2 Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - KEELOQ<sup>®</sup> Demonstration Board

## 11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows<sup>®</sup>-based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

# 11.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel<sup>®</sup> standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

# 11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

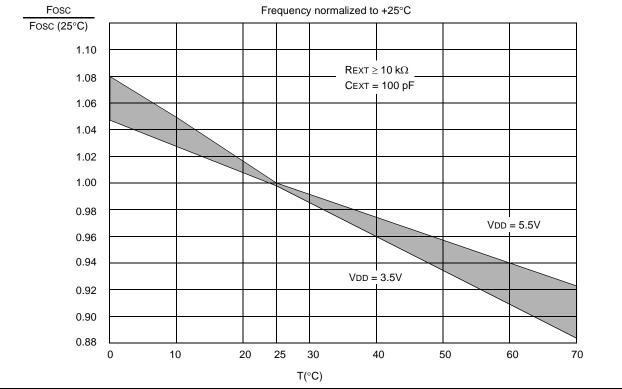
For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

# 14.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean +  $3\sigma$ ) or (mean -  $3\sigma$ ) respectively, where  $\sigma$  is a standard deviation, over the whole temperature range.



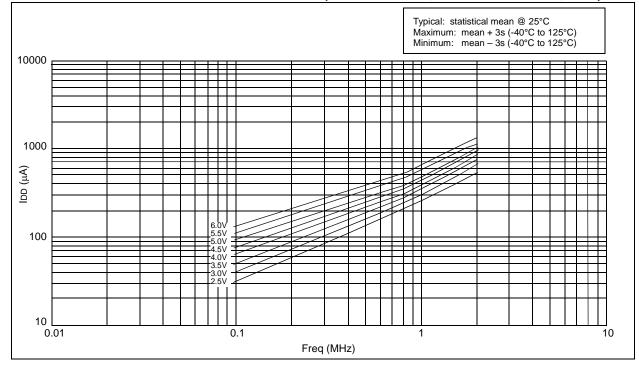


#### TABLE 14-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Ave Fosc @	
20 pF	3.3K	5 MHz	± 27%
	5K	3.8 MHz	± 21%
	10K	2.2 MHz	± 21%
	100K	262 kHz	± 31%
100 pF	3.3K	1.6 MHz	± 13%
	5K	1.2 MHz	± 13%
	10K	684 kHz	± 18%
	100K	71 kHz	± 25%
300 pF	3.3K	660 kHz	± 10%
	5.0K	484 kHz	± 14%
	10K	267 kHz	± 15%
	100K	29 kHz	± 19%

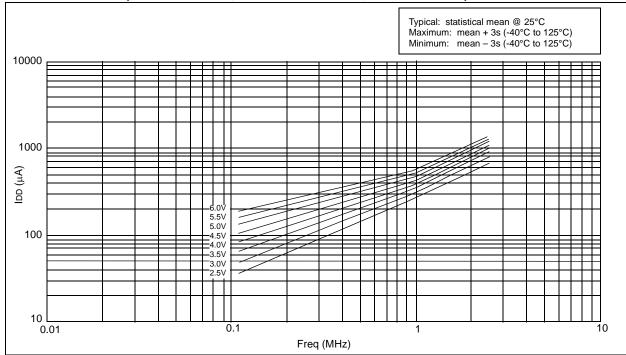
The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is  $\pm 3$  standard deviations from the average value for VDD = 5V.



#### FIGURE 16-12: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 PF, 25°C)

FIGURE 16-13: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 PF, -40°C to +85°C)



# 18.0 DEVICE CHARACTERIZATION - PIC16LC54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean +  $3\sigma$ ) or (mean -  $3\sigma$ ) respectively, where  $\sigma$  is a standard deviation, over the whole temperature range.

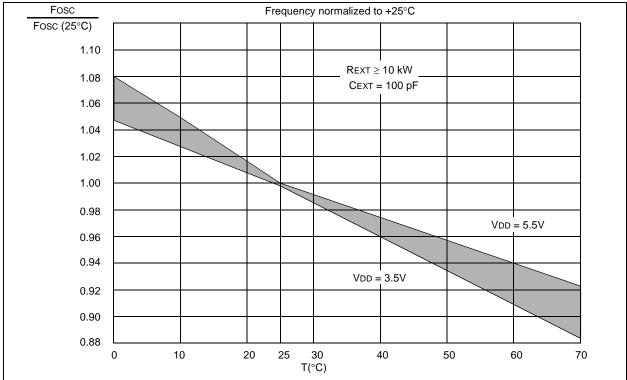


FIGURE 18-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

#### TABLE 18-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext		rage 5V, 25°C
20 pF	3.3K	5 MHz	± 27%
	5K	3.8 MHz	± 21%
	10K	2.2 MHz	± 21%
	100K	262 kHz	± 31%
100 pF	3.3K	1.63 MHz	± 13%
	5K	1.2 MHz	± 13%
	10K	684 kHz	± 18%
	100K	71 kHz	± 25%
300 pF	3.3K	660 kHz	± 10%
	5.0K	484 kHz	± 14%
	10K	267 kHz	± 15%
	100K	29 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is  $\pm 3$  standard deviation from average value for VDD = 5V.