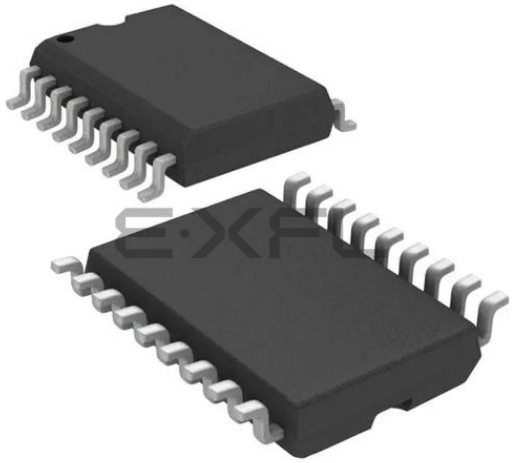

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 12 |
| Program Memory Size | 1.5KB (1K x 12) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 25 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 6.25V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 18-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 18-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16c56-xt-so |

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## 4.3 External Crystal Oscillator Circuit

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 4-3 shows an implementation example of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

**FIGURE 4-3: EXAMPLE OF EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)**

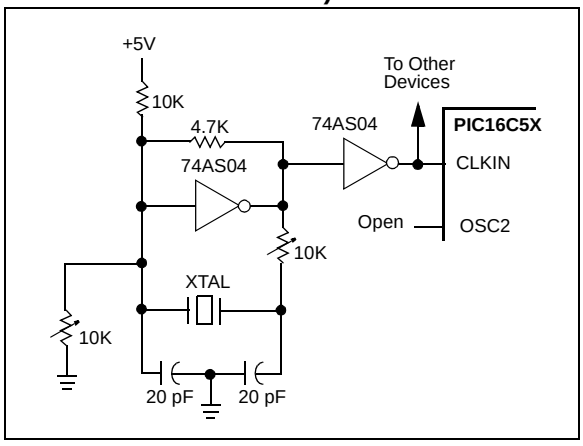
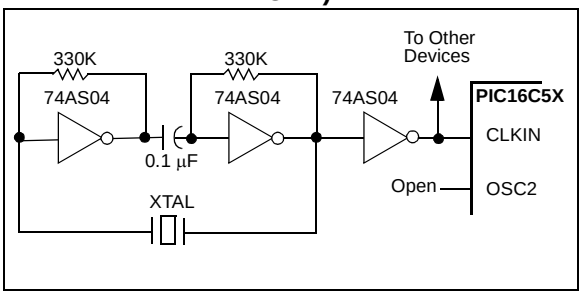



Figure 4-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

**FIGURE 4-4: EXAMPLE OF EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)**



**NOTES:**

## 6.0 MEMORY ORGANIZATION

PIC16C5X memory is organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one or two STATUS Register bits. For devices with a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Selection Register (FSR).

### 6.1 Program Memory Organization

The PIC16C54, PIC16CR54 and PIC16C55 have a 9-bit Program Counter (PC) capable of addressing a 512 x 12 program memory space (Figure 6-1). The PIC16C56 and PIC16CR56 have a 10-bit Program Counter (PC) capable of addressing a 1K x 12 program memory space (Figure 6-2). The PIC16CR57, PIC16C58 and PIC16CR58 have an 11-bit Program Counter capable of addressing a 2K x 12 program memory space (Figure 6-3). Accessing a location above the physically implemented address will cause a wraparound.

A NOP at the RESET vector location will cause a restart at location 000h. The RESET vector for the PIC16C54, PIC16CR54 and PIC16C55 is at 1FFh. The RESET vector for the PIC16C56 and PIC16CR56 is at 3FFh. The RESET vector for the PIC16C57, PIC16CR57, PIC16C58, and PIC16CR58 is at 7FFh. See Section 6.5 for additional information using CALL and GOTO instructions.

**FIGURE 6-1: PIC16C54/CR54/C55 PROGRAM MEMORY MAP AND STACK**

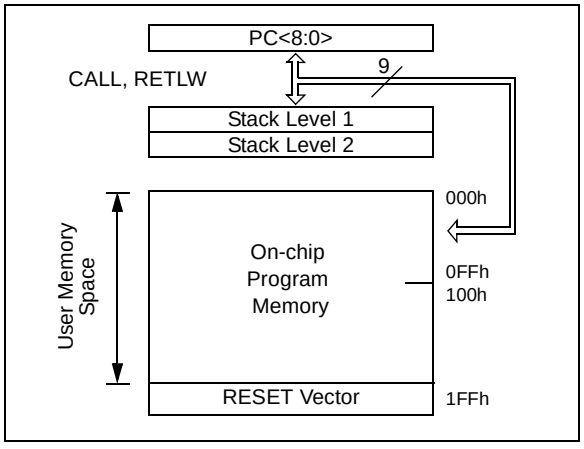



**FIGURE 6-2: PIC16C56/CR56 PROGRAM MEMORY MAP AND STACK**

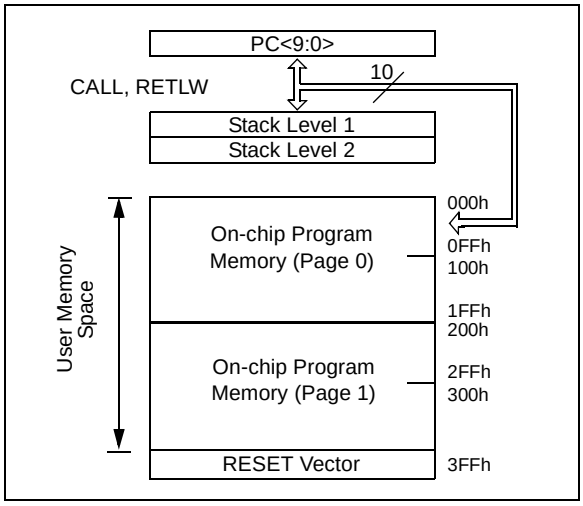
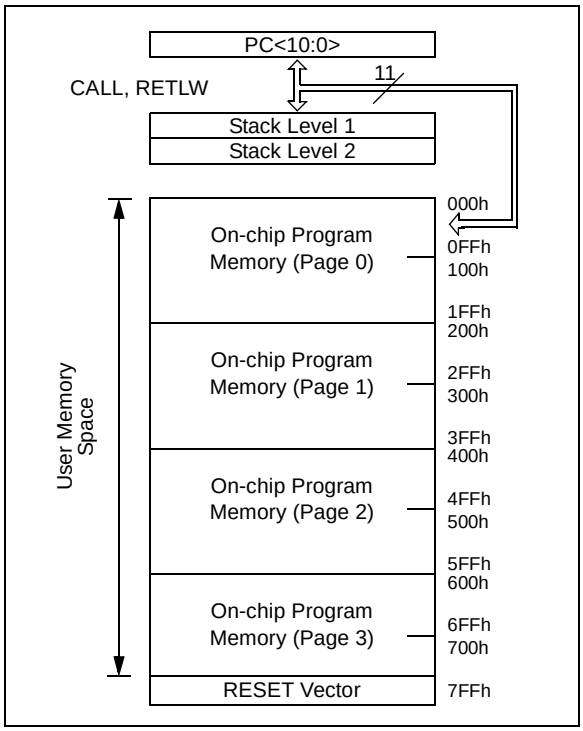



**FIGURE 6-3: PIC16C57/CR57/C58/ CR58 PROGRAM MEMORY MAP AND STACK**



**BSF** **Bit Set f**

Syntax: [ *label* ] BSF f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: $1 \rightarrow (f<b>)$

Status Affected: None

Encoding:

| 0101 | bbbf | ffff |
|---|---|---|

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Example:
```
BSF     FLAG_REG,    7
```
Before Instruction
FLAG_REG = 0x0A
After Instruction
FLAG_REG = 0x8A

**BTFSC** **Bit Test f, Skip if Clear**

Syntax: [ *label* ] BTFSC f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

| 0110 | bbbf | ffff |
|---|---|---|

Description: If bit 'b' in register 'f' is 0 then the next instruction is skipped.
If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and a `NOP` is executed instead, making this a 2-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address `(HERE)`
After Instruction
if FLAG<1> = 0,
PC = address `(TRUE)`;
if FLAG<1> = 1,
PC = address `(FALSE)`

**BTFSS** **Bit Test f, Skip if Set**

Syntax: [ *label* ] BTFSS f,b

Operands: $0 \le f \le 31$
$0 \le b < 7$

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

| 0111 | bbbf | ffff |
|---|---|---|

Description: If bit 'b' in register 'f' is '1' then the next instruction is skipped.
If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a `NOP` is executed instead, making this a 2-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSS   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address `(HERE)`
After Instruction
If FLAG<1> = 0,
PC = address `(FALSE)`;
if FLAG<1> = 1,
PC = address `(TRUE)`

**SUBWF** **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – (W) → (dest)

Status Affected: C, DC, Z

Encoding:

| 0000 | 10df | ffff |
|---|---|---|

Description: Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1: `SUBWF REG1, 1`

Before Instruction
REG1 = 3
W = 2
C = ?
After Instruction
REG1 = 1
W = 2
C = 1 ; result is positive

Example 2:
Before Instruction
REG1 = 2
W = 2
C = ?
After Instruction
REG1 = 0
W = 2
C = 1 ; result is zero

Example 3:
Before Instruction
REG1 = 1
W = 2
C = ?
After Instruction
REG1 = 0xFF
W = 2
C = 0 ; result is negative

**SWAPF** **Swap Nibbles in f**

Syntax: [ *label* ] SWAPF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f<3:0>) → (dest<7:4>);
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

| 0011 | 10df | ffff |
|---|---|---|

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example `SWAPF REG1, 0`

Before Instruction
REG1 = 0xA5
After Instruction
REG1 = 0xA5
W = 0x5A

**TRIS** **Load TRIS Register**

Syntax: [ *label* ] TRIS f

Operands: f = 5, 6 or 7

Operation: (W) → TRIS register f

Status Affected: None

Encoding:

| 0000 | 0000 | 0fff |
|---|---|---|

Description: TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register.

Words: 1

Cycles: 1

Example `TRIS PORTB`

Before Instruction
W = 0xA5
After Instruction
TRISB = 0xA5

## 12.3 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

| PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended) | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | | | | | |
| | | PIC16C5X-RCE | 3.25 | — | 6.0 | V | |
| | | PIC16C5X-XTE | 3.25 | — | 6.0 | V | |
| | | PIC16C5X-10E | 4.5 | — | 5.5 | V | |
| | | PIC16C5X-HSE | 4.5 | — | 5.5 | V | |
| | | PIC16C5X-LPE | 2.5 | — | 6.0 | V | |
| D002 | VDR | **RAM Data Retention Voltage(1)** | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | VSS | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D010 | IDD | **Supply Current(2)** | | | | | |
| | | PIC16C5X-RCE(3) | — | 1.8 | 3.3 | mA | FOSC = 4 MHz, VDD = 5.5V |
| | | PIC16C5X-XTE | — | 1.8 | 3.3 | mA | FOSC = 4 MHz, VDD = 5.5V |
| | | PIC16C5X-10E | — | 4.8 | 10 | mA | FOSC = 10 MHz, VDD = 5.5V |
| | | PIC16C5X-HSE | — | 4.8 | 10 | mA | FOSC = 10 MHz, VDD = 5.5V |
| | | PIC16C5X-HSE | — | 9.0 | 20 | mA | FOSC = 16 MHz, VDD = 5.5V |
| | | PIC16C5X-LPE | — | 19 | 55 | μA | FOSC = 32 kHz, VDD = 3.25V, WDT disabled |
| D020 | IPD | **Power-down Current(2)** | — | 5.0 | 22 | μA | VDD = 3.25V, WDT enabled |
| | | | — | 0.8 | 18 | μA | VDD = 3.25V, WDT disabled |

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

## 12.4 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial) PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D030 | VIL | **Input Low Voltage** | | | | | |
| | | I/O ports | VSS | — | 0.2 VDD | V | Pin at hi-impedance |
| | | MCLR (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | T0CKI (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | OSC1 (Schmitt Trigger) | VSS | — | 0.15 VDD | V | PIC16C5X-RC only(3) |
| | | OSC1 (Schmitt Trigger) | VSS | — | 0.3 VDD | V | PIC16C5X-XT, 10, HS, LP |
| D040 | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | 0.45 VDD | — | VDD | V | For all VDD(4) |
| | | I/O ports | 2.0 | — | VDD | V | 4.0V < VDD ≤ 5.5V(4) |
| | | I/O ports | 0.36 VDD | — | VDD | V | VDD > 5.5V |
| | | MCLR (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | T0CKI (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | OSC1 (Schmitt Trigger) | 0.85 VDD | — | VDD | V | PIC16C5X-RC only(3) |
| | | OSC1 (Schmitt Trigger) | 0.7 VDD | — | VDD | V | PIC16C5X-XT, 10, HS, LP |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current(1,2)** | | | | | **For VDD ≤ 5.5V:** |
| | | I/O ports | –1 | 0.5 | +1 | µA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| | | MCLR | –5 | — | — | µA | VPIN = VSS + 0.25V |
| | | MCLR | — | 0.5 | +5 | µA | VPIN = VDD |
| | | T0CKI | –3 | 0.5 | +3 | µA | VSS ≤ VPIN ≤ VDD |
| | | OSC1 | –3 | 0.5 | +3 | µA | VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, 10, HS, LP |
| D080 | VOL | **Output Low Voltage** | | | | | |
| | | I/O ports | — | — | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | — | — | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC |
| D090 | VOH | **Output High Voltage(2)** | | | | | |
| | | I/O ports | VDD – 0.7 | — | — | V | IOH = –5.4 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | VDD – 0.7 | — | — | V | IOH = –1.0 mA, VDD = 4.5V, PIC16C5X-RC |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

**4:** The user may use the better of the two specifications.

## 13.4 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D030 | VIL | **Input Low Voltage** | | | | | |
| | | I/O ports | Vss | — | 0.15 VDD | V | Pin at hi-impedance |
| | | MCLR (Schmitt Trigger) | Vss | — | 0.15 VDD | V | |
| | | T0CKI (Schmitt Trigger) | Vss | — | 0.15 VDD | V | |
| | | OSC1 (Schmitt Trigger) | Vss | — | 0.15 VDD | V | RC mode only(3) |
| | | OSC1 | Vss | — | 0.3 VDD | V | XT, HS and LP modes |
| D040 | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | 0.45 VDD | — | VDD | V | For all VDD(4) |
| | | I/O ports | 2.0 | — | VDD | V | 4.0V < VDD ≤ 5.5V(4) |
| | | I/O ports | 0.36 VDD | — | VDD | V | VDD > 5.5V |
| | | MCLR (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | T0CKI (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | OSC1 (Schmitt Trigger) | 0.85 VDD | — | VDD | V | RC mode only(3) |
| | | OSC1 | 0.7 VDD | — | VDD | V | XT, HS and LP modes |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current(1,2)** | | | | | **For VDD ≤ 5.5V:** |
| | | I/O ports | –1.0 | 0.5 | +1.0 | µA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| | | MCLR | –5.0 | — | — | µA | VPIN = VSS + 0.25V |
| | | MCLR | — | 0.5 | +5.0 | µA | VPIN = VDD |
| | | T0CKI | –3.0 | 0.5 | +3.0 | µA | VSS ≤ VPIN ≤ VDD |
| | | OSC1 | –3.0 | 0.5 | +3.0 | µA | VSS ≤ VPIN ≤ VDD, XT, HS and LP modes |
| D080 | VOL | **Output Low Voltage** | | | | | |
| | | I/O ports | — | — | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | — | — | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V, RC mode only |
| D090 | VOH | **Output High Voltage(2)** | | | | | |
| | | I/O ports | VDD – 0.7 | — | — | V | IOH = –5.4 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | VDD – 0.7 | — | — | V | IOH = –1.0 mA, VDD = 4.5V, RC mode only |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

**4:** The user may use the better of the two specifications.

## 15.4 DC Characteristics: PIC16C54A-04, 10, 20, PIC16LC54A-04, PIC16LV54A-02 (Commercial) PIC16C54A-04I, 10I, 20I, PIC16LC54A-04I, PIC16LV54A-02I (Industrial) PIC16C54A-04E, 10E, 20E, PIC16LC54A-04E (Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–20°C ≤ TA ≤ +85°C for industrial-PIC16LV54A-02I<br>–40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D030 | VIL | **Input Low Voltage** | | | | | |
| | | I/O ports | VSS | — | 0.2 VDD | V | Pin at hi-impedance |
| | | MCLR (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | T0CKI (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | OSC1 (Schmitt Trigger) | VSS | — | 0.15 VDD | V | RC mode only(3) |
| | | OSC1 | VSS | — | 0.3 VDD | | XT, HS and LP modes |
| D040 | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | 0.2 VDD + 1 | — | VDD | V | For all VDD(4) |
| | | I/O ports | 2.0 | — | VDD | V | 4.0V < VDD ≤ 5.5V(4) |
| | | MCLR (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | T0CKI (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | OSC1 (Schmitt Trigger) | 0.85 VDD | — | VDD | V | RC mode only(3) |
| | | OSC1 | 0.7 VDD | — | VDD | V | XT, HS and LP modes |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current(1,2)** | | | | | **For VDD ≤ 5.5V:** |
| | | I/O ports | -1.0 | 0.5 | +1.0 | µA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| | | MCLR | -5.0 | — | +5.0 | µA | VPIN = VSS +0.25V |
| | | MCLR | — | 0.5 | +3.0 | µA | VPIN = VDD |
| | | T0CKI | -3.0 | 0.5 | +3.0 | µA | VSS ≤ VPIN ≤ VDD |
| | | OSC1 | -3.0 | 0.5 | — | µA | VSS ≤ VPIN ≤ VDD, XT, HS and LP modes |
| D080 | VOL | **Output Low Voltage** | | | | | |
| | | I/O ports | — | — | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | — | — | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V, RC mode only |
| | VOH | **Output High Voltage(2)** | | | | | |
| | | I/O ports | VDD - 0.7 | — | — | V | IOH = -5.4 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | VDD - 0.7 | — | — | V | IOH = -1.0 mA, VDD = 4.5V, RC mode only |

* These parameters are characterized but not tested.

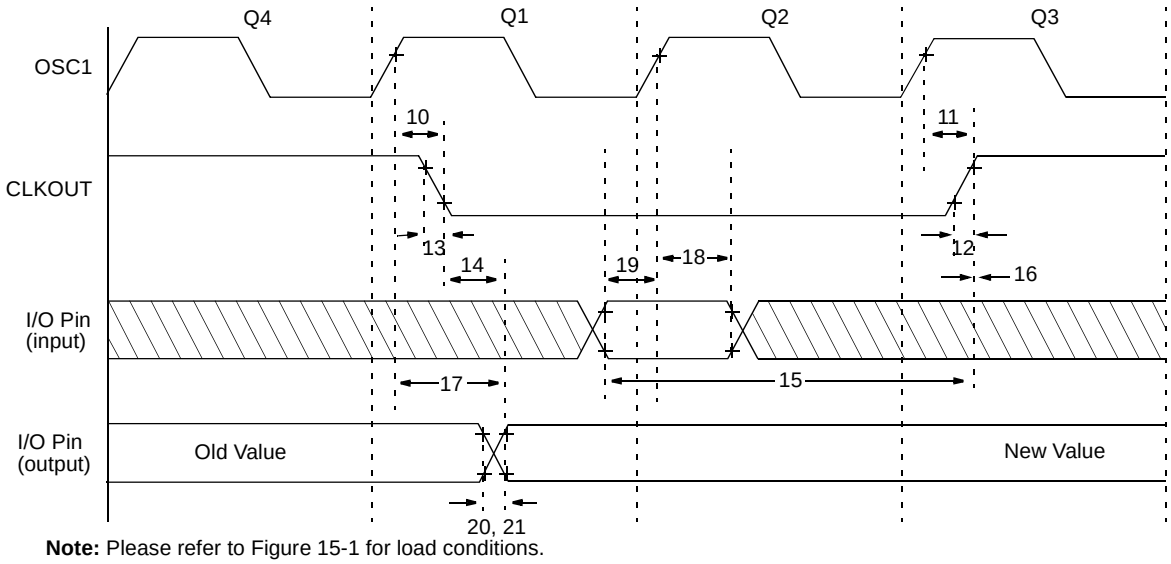
† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

**FIGURE 15-3: CLKOUT AND I/O TIMING - PIC16C54A**




**Note:** Please refer to Figure 15-1 for load conditions.

**TABLE 15-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54A**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I<br>–40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** |
| 10 | TosH2ckL | OSC1↑ to CLKOUT↓(1) | — | 15 | 30** | ns |
| 11 | TosH2ckH | OSC1↑ to CLKOUT↑(1) | — | 15 | 30** | ns |
| 12 | TckR | CLKOUT rise time(1) | — | 5.0 | 15** | ns |
| 13 | TckF | CLKOUT fall time(1) | — | 5.0 | 15** | ns |
| 14 | TckL2ioV | CLKOUT↓ to Port out valid(1) | — | — | 40** | ns |
| 15 | TioV2ckH | Port in valid before CLKOUT↑(1) | 0.25 TCY+30* | — | — | ns |
| 16 | TckH2ioI | Port in hold after CLKOUT↑(1) | 0* | — | — | ns |
| 17 | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid(2) | — | — | 100* | ns |
| 18 | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | TBD | — | — | ns |
| 19 | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | TBD | — | — | ns |
| 20 | TioR | Port output rise time(2) | — | 10 | 25** | ns |
| 21 | TioF | Port output fall time(2) | — | 10 | 25** | ns |

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

**2:** Please refer to Figure 15-1 for load conditions.

**FIGURE 16-7: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS - VDD**

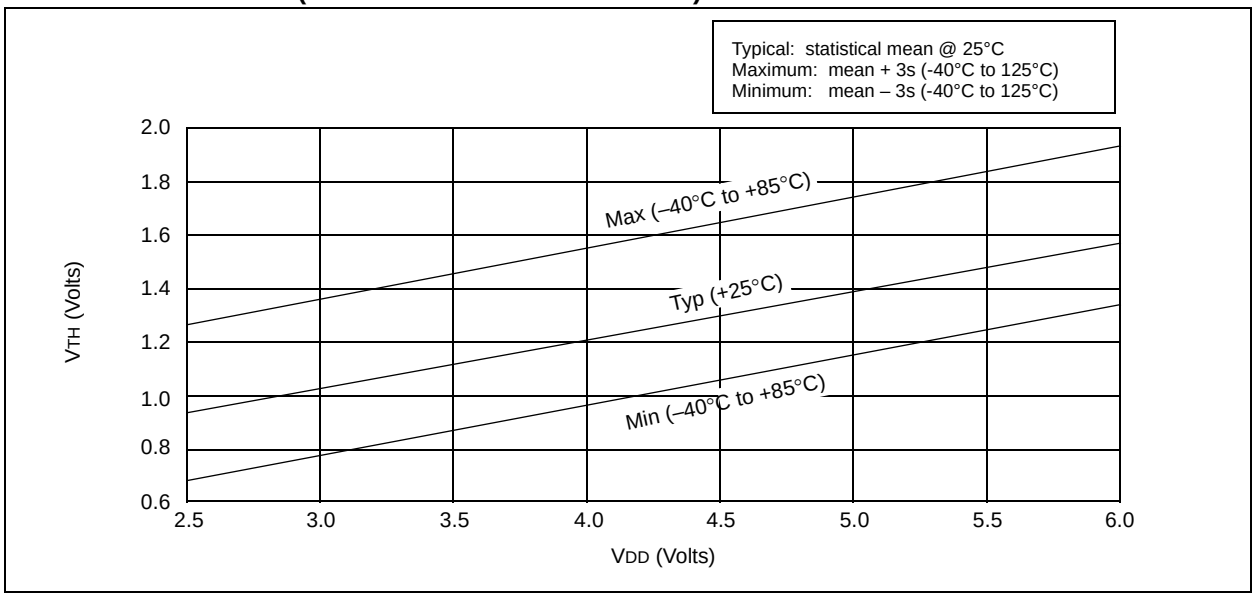



**FIGURE 16-8: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. VDD**

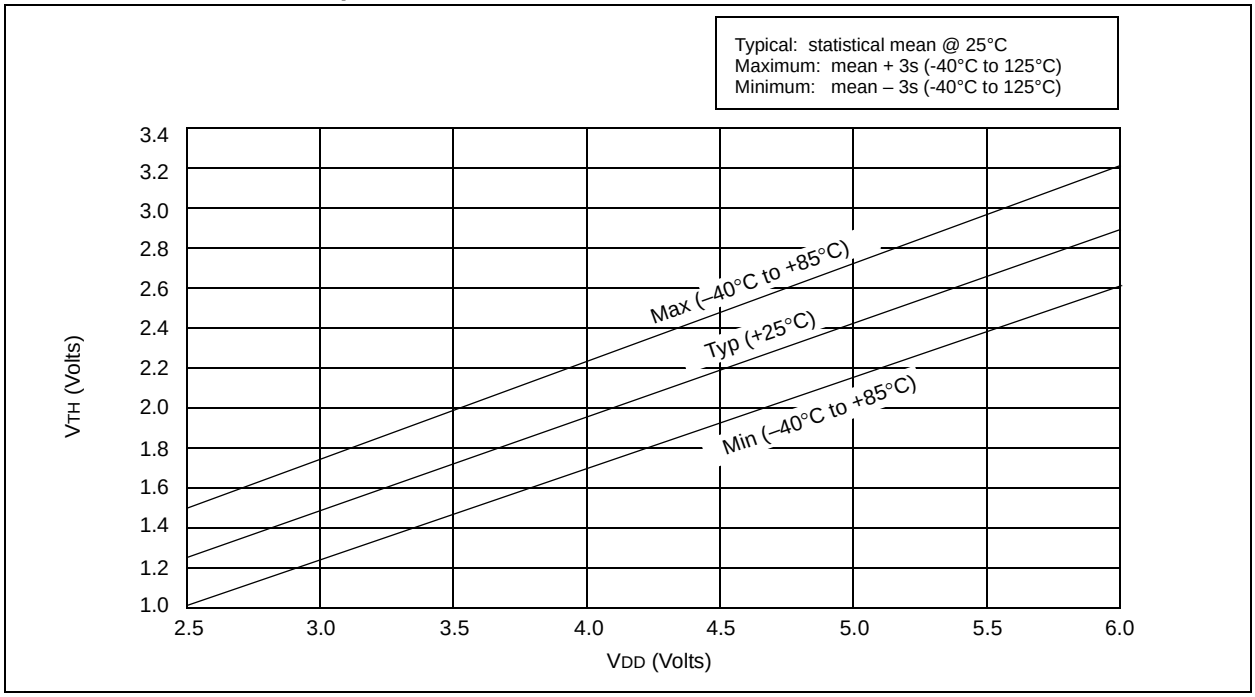


**FIGURE 16-18: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD**

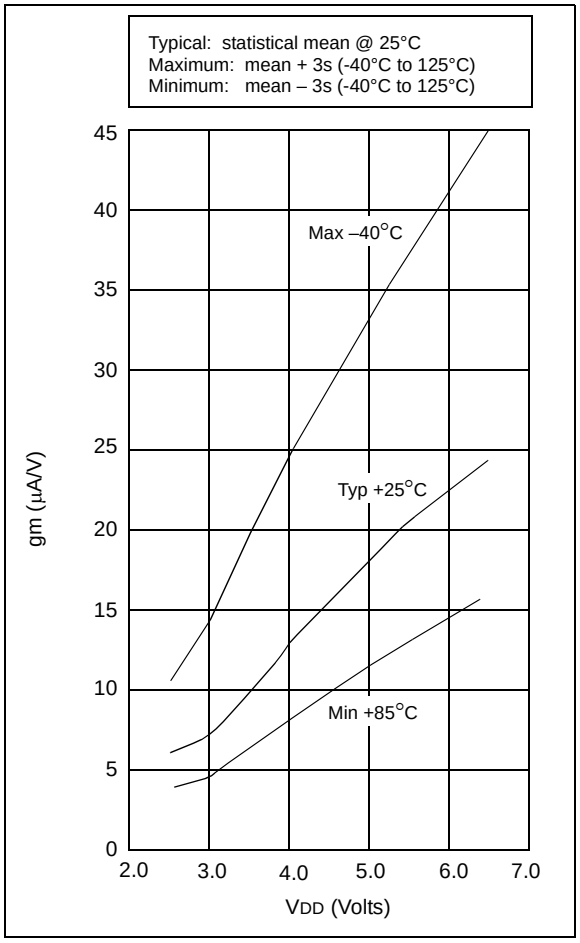



**FIGURE 16-19: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD**

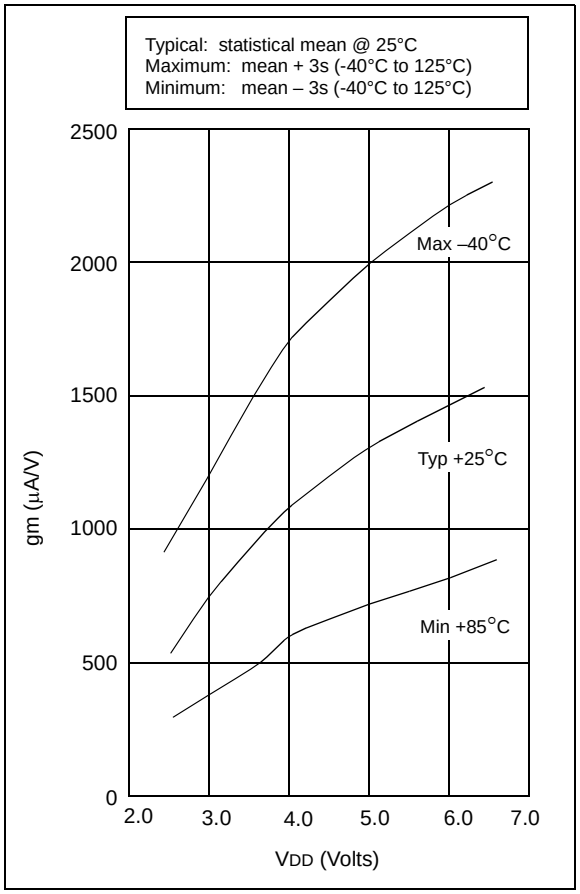
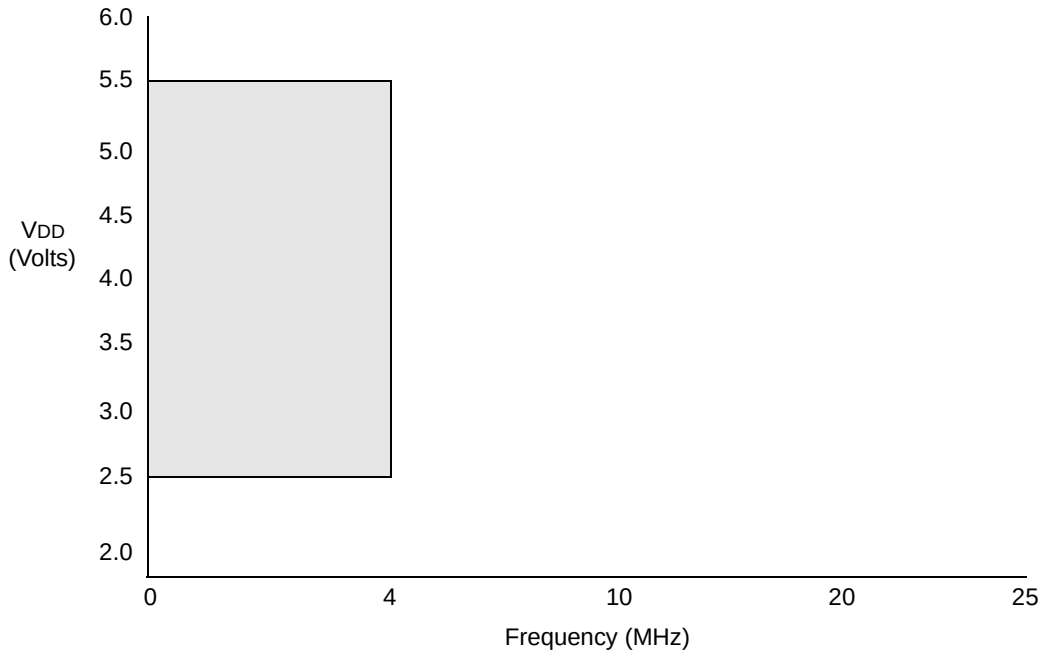


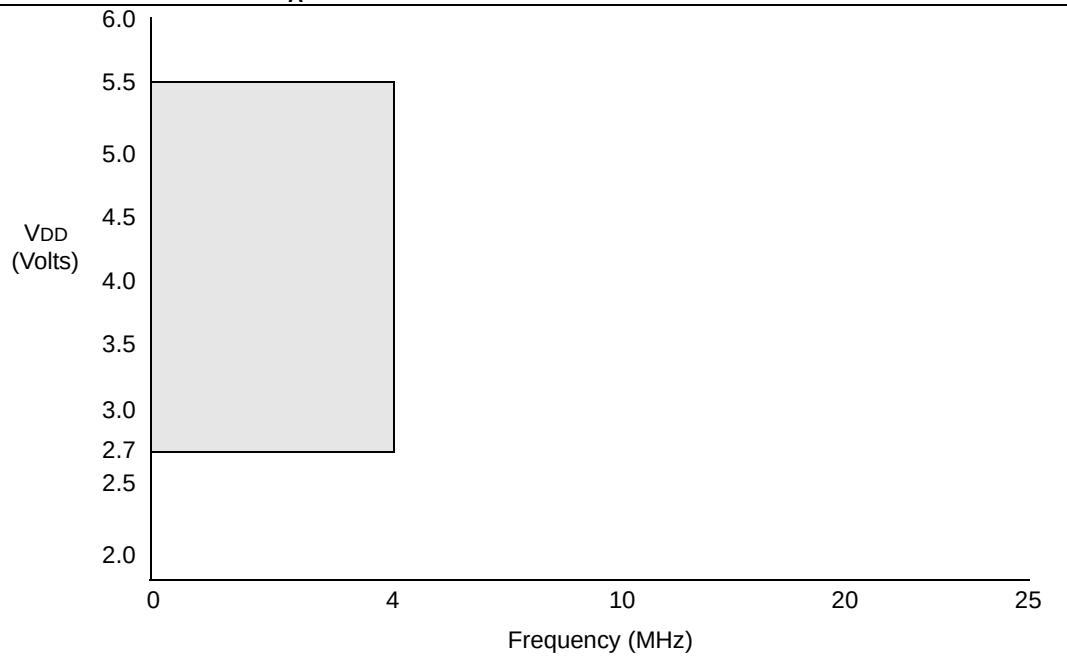
**FIGURE 17-3: PIC16LC54C/55A/56A/57C/58B VOLTAGE-FREQUENCY GRAPH, $0°C \leq T_A \leq +85°C$**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

**2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

**FIGURE 17-4: PIC16LC54C/55A/56A/57C/58B VOLTAGE-FREQUENCY GRAPH, $-40°C \leq T_A \leq 0°C$**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

**2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

**FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF, 25°C**

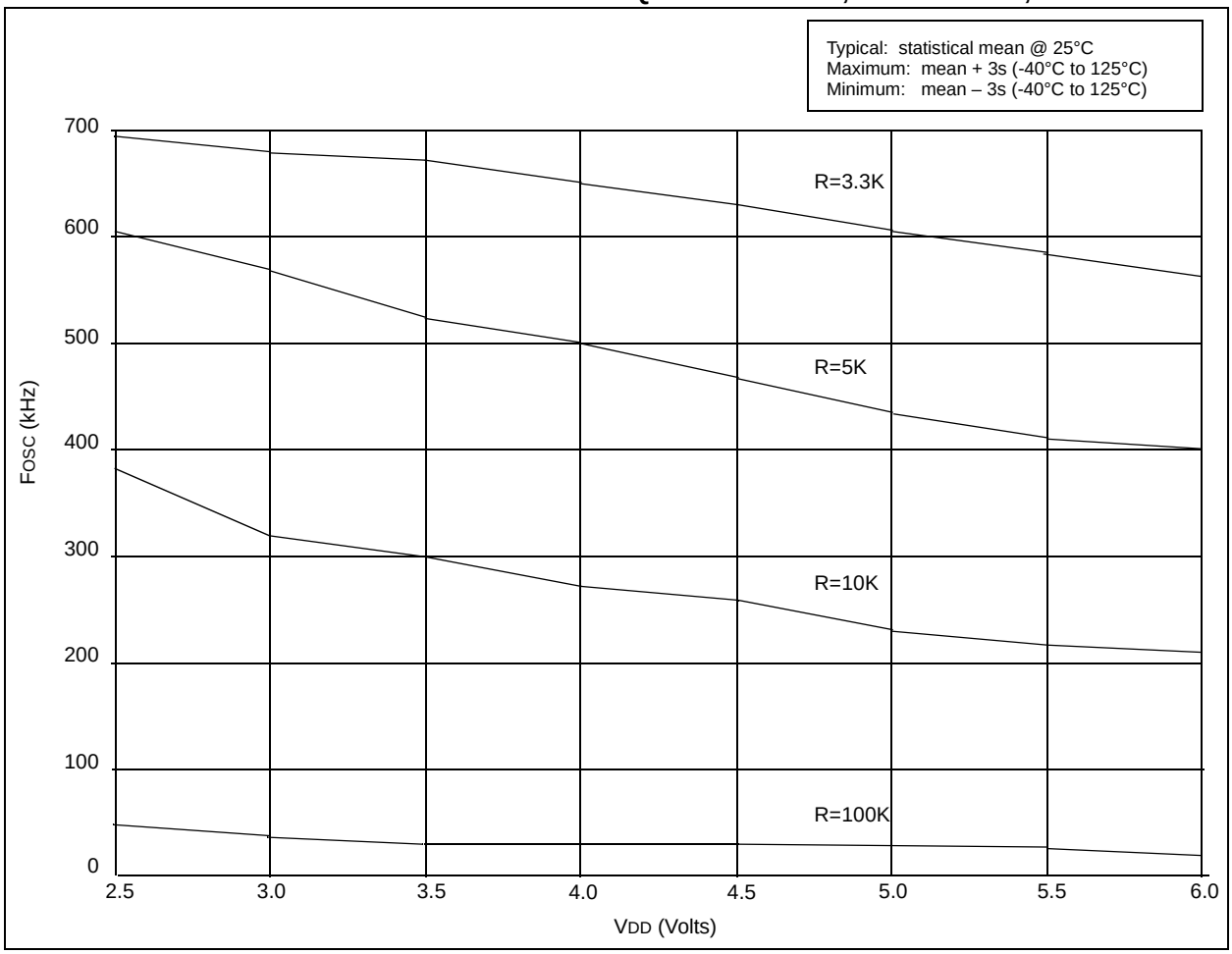



**FIGURE 18-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)**

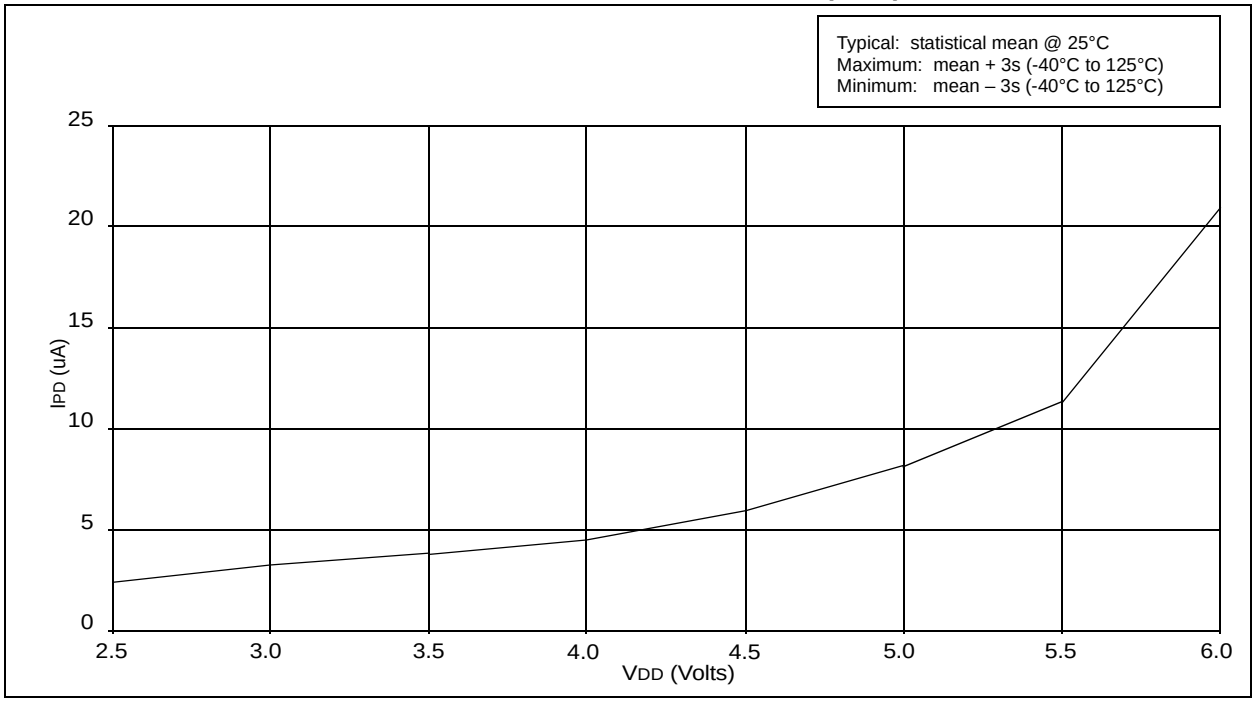


**FIGURE 18-10: $V_{TH}$ (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (IN XT, HS AND LP MODES) vs. $V_{DD}$**

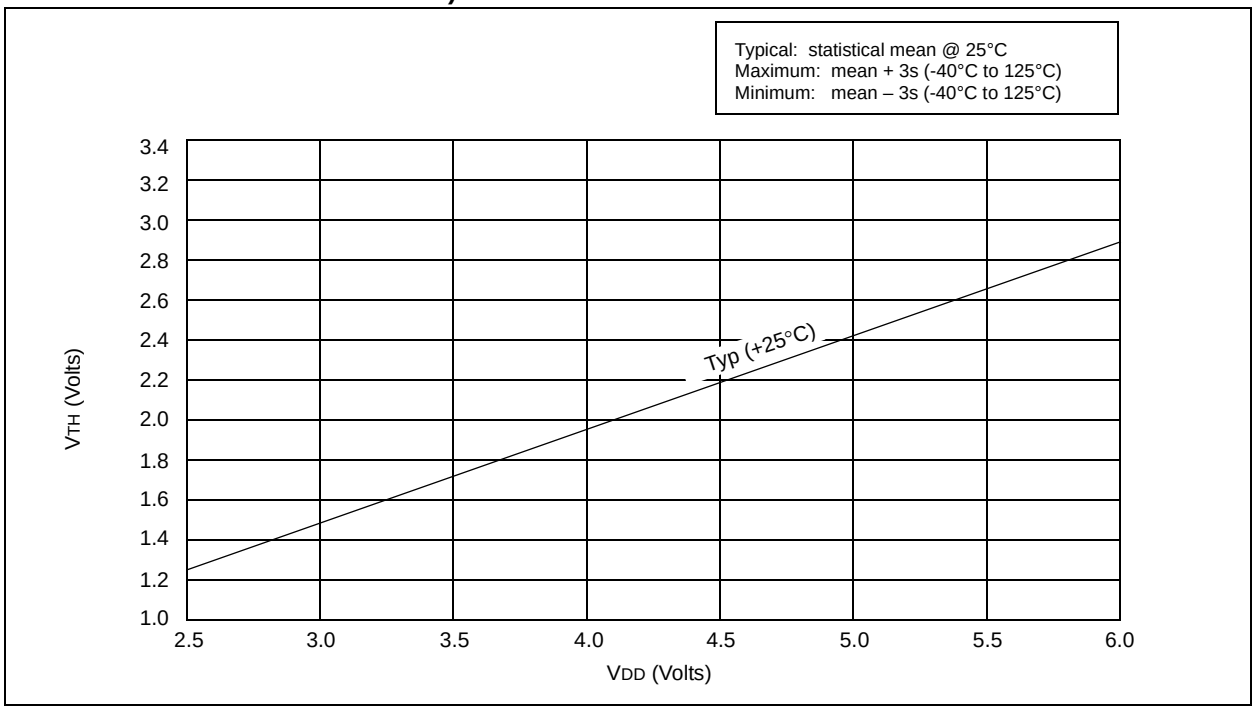
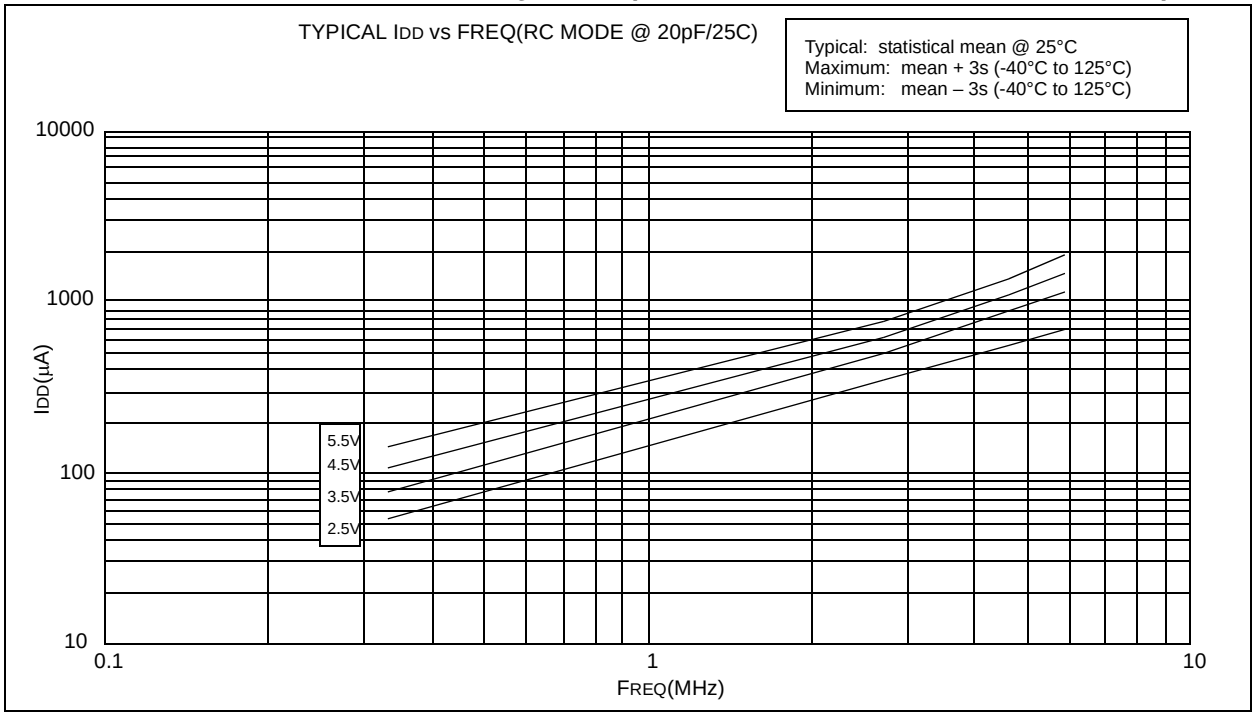



**FIGURE 18-11: TYPICAL $I_{DD}$ vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, 25°C)**



## 19.0 ELECTRICAL CHARACTERISTICS - PIC16LC54C 40MHz

**Absolute Maximum Ratings(†)**

Ambient temperature under bias ..... –55°C to +125°C
Storage temperature ..... –65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ ..... 0 to +14V
Voltage on all other pins with respect to $V_{SS}$ ..... –0.6V to ($V_{DD}$ + 0.6V)
Total power dissipation(1) ..... 800 mW
Max. current out of $V_{SS}$ pin ..... 150 mA
Max. current into $V_{DD}$ pin ..... 100 mA
Max. current into an input pin (T0CKI only) ..... ±500 μA
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) ..... ±20 mA
Max. output current sunk by any I/O pin ..... 25 mA
Max. output current sourced by any I/O pin ..... 20 mA
Max. output current sourced by a single I/O (Port A, B or C) ..... 50 mA
Max. output current sunk by a single I/O (Port A, B or C) ..... 50 mA

**Note 1:** Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 19.4 Timing Diagrams and Specifications

**FIGURE 19-3: EXTERNAL CLOCK TIMING - PIC16C5X-40**

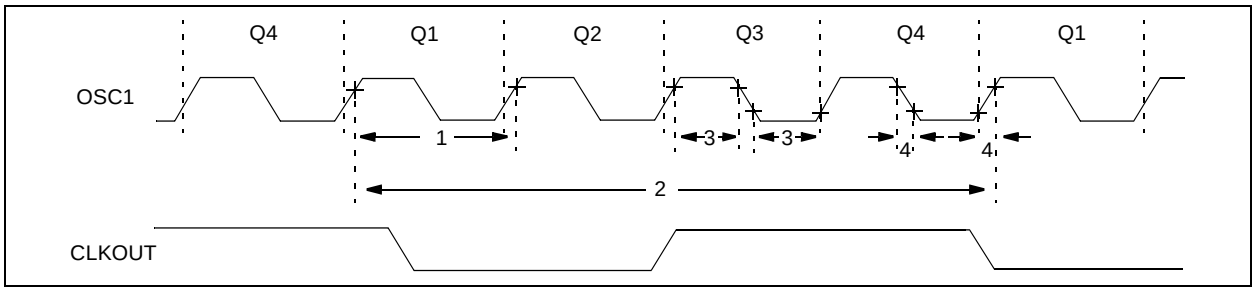



**TABLE 19-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X-40**

| AC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | FOSC | External CLKIN Frequency(1) | 20 | — | 40 | MHz | HS OSC mode |
| 1 | TOSC | External CLKIN Period(1) | 25 | — | — | ns | HS OSC mode |
| 2 | Tcy | Instruction Cycle Time(2) | — | 4/FOSC | — | — | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 6.0* | — | — | ns | HS oscillator |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 6.5* | ns | HS oscillator |

* These parameters are characterized but not tested.

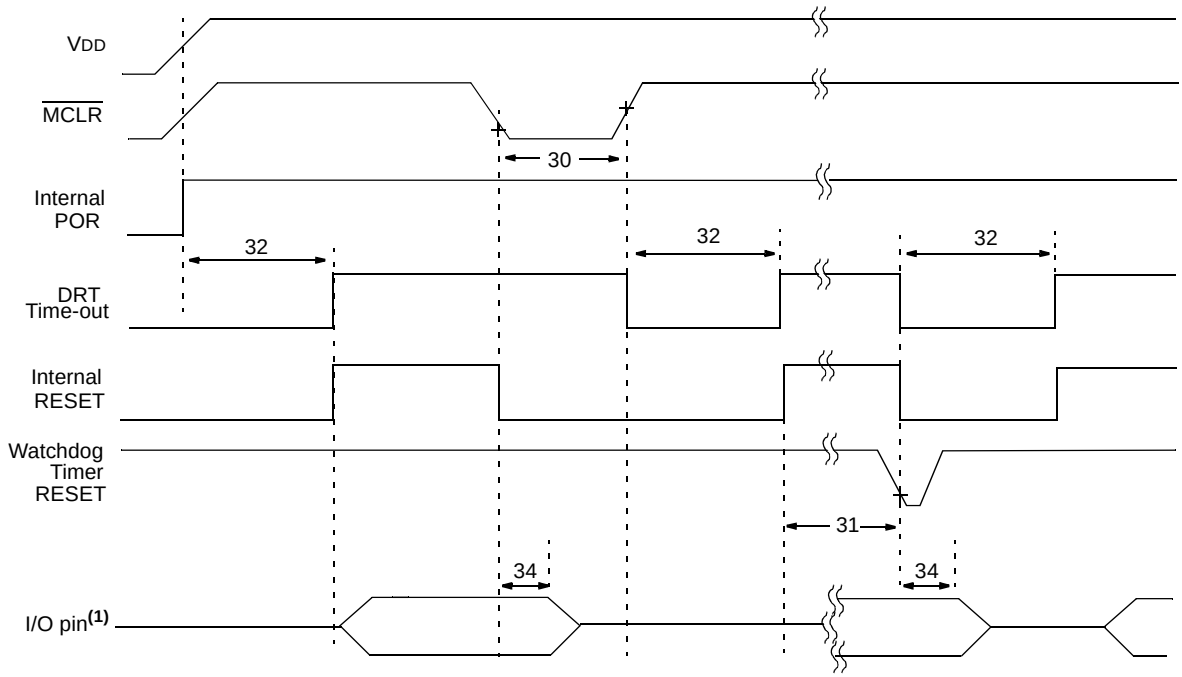
† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

**FIGURE 19-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X-40**




**Note 1:** Please refer to Figure 19-2 for load conditions.

**TABLE 19-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X-40**

| **AC Characteristics** | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)<br>Operating Voltage VDD range is described in Section 19.1. | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 1000* | — | — | ns | VDD = 5.0V |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 32 | TDRT | Device Reset Timer Period | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 34 | Tioz | I/O Hi-impedance from $\overline{\text{MCLR}}$ Low | 100* | 300* | 1000* | ns | |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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