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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c56-xti-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.0 PIC16C5X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC16C5X Product Identification System at the back of this data sheet to specify the correct part number.

For the PIC16C5X family of devices, there are four device types, as indicated in the device number:

- 1. **C**, as in PIC16**C**54C. These devices have EPROM program memory and operate over the standard voltage range.
- LC, as in PIC16LC54A. These devices have EPROM program memory and operate over an extended voltage range.
- 3. **CR**, as in PIC16**CR**54A. These devices have ROM program memory and operate over the standard voltage range.
- 4. LCR, as in PIC16LCR54A. These devices have ROM program memory and operate over an extended voltage range.

2.1 UV Erasable Devices (EPROM)

The UV erasable versions offered in CERDIP packages, are optimal for prototype development and pilot programs.

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's

PICSTART[®] Plus⁽¹⁾ and PRO MATE[®] programmers both support programming of the PIC16C5X. Third party programmers also are available. Refer to the Third Party Guide (DS00104) for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates, or small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

Note 1: PIC16LC54C and PIC16C54A devices require OSC2 not to be connected while programming with PICSTART[®] Plus programmer.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTPSM) Devices

Microchip offers the unique programming service where a few user defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, giving the customer a low cost option for high volume, mature products.

	Pin Number			Pin	Buffer	
Pin Name	DIP	SOIC	SSOP	Туре	Туре	Description
RA0	17	17	19	I/O	TTL	Bi-directional I/O port
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RB0	6	6	7	I/O	TTL	Bi-directional I/O port
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	
RB5	11	11	12	I/O	TTL	
RB6	12	12	13	I/O	TTL	
RB7	13	13	14	I/O	TTL	
TOCKI	3	3	3	I	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in use, to reduce current consumption.
MCLR/Vpp	4	4	4	I	ST	Master clear (RESET) input/programming voltage input. This pin is an active low RESET to the device. Voltage on the MCLR/VPP pin must not exceed VDD to avoid unin- tended entering of Programming mode.
OSC1/CLKIN	16	16	18	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	17	0		Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
Vdd	14	14	15,16	Р	_	Positive supply for logic and I/O pins.
Vss	5	5	5,6	Р	_	Ground reference for logic and I/O pins.

TABLE 3-1:PINOUT DESCRIPTION - PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16CR58,
PIC16CR58

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

NOTES:

6.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 6-1).

The Special Registers can be classified into two sets. The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Details on Page
N/A	TRIS	I/O Cont	I/O Control Registers (TRISA, TRISB, TRISC)								35
N/A	OPTION	Contains	s control b	oits to cor	figure Ti	mer0 and	Timer0/V	VDT pres	caler	11 1111	30
00h	INDF	Uses co	Uses contents of FSR to address data memory (not a physical register)							XXXX XXXX	32
01h	TMR0	Timer0 I	Timer0 Module Register							XXXX XXXX	38
02h ⁽¹⁾	PCL	Low ord	er 8 bits c	of PC						1111 1111	31
03h	STATUS	PA2	PA2 PA1 PA0 TO PD Z DC C						0001 1xxx	29	
04h	FSR	Indirect	Indirect data memory address pointer							1xxx xxxx (3)	32
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	xxxx	35
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	XXXX XXXX	35
07h ⁽²⁾	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	XXXX XXXX	35

|--|

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 6.5 for an explanation of how to access these bits.

2: File address 07h is a General Purpose Register on the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16CR58 and PIC16CR58.

3: These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for MCLR and WDT Reset, the value is 111u uuuu.

7.6 I/O Programming Considerations

7.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 7-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 7-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;

;				PORT	latch	PORT	pins
;							
	BCF	PORTB,	7	;01pp	pppp	11pp	pppp
	BCF	PORTB,	6	;10pp	pppp	11pp	pppp
	MOVLW	H'3F'		;			
	TRIS	PORTB		;10pp	pppp	10pp	pppp
;							

;Note that the user may have expected the pin ;values to be 00pp pppp. The 2nd BCF caused ;RB7 to be latched as the pin value (High).

7.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 7-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.



FIGURE 7-2: SUCCESSIVE I/O OPERATION

CALL	Subroutine Call						
Syntax:	[<i>label</i>] CALL k						
Operands:	$0 \leq k \leq 255$						
Operation:	$\begin{array}{l} (PC) + 1 \rightarrow TOS; \\ k \rightarrow PC < 7:0 >; \\ (STATUS < 6:5 >) \rightarrow PC < 10:9 >; \\ 0 \rightarrow PC < 8 > \end{array}$						
Status Affected:	None						
Encoding:	1001 kkkk kkkk						
Description.	Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two- cycle instruction						
Words:	1						
Cycles:	2						
Example:	HERE CALL THERE						
Before Instruction PC = address (HERE) After Instruction PC = address (THERE) TOS = address (HERE + 1)							

CLRE	Clear f
	Cical I

Syntax:	[label]	CLRF f						
Operands:	$0 \le f \le 31$							
Operation:	$\begin{array}{l} 00h \rightarrow (f); \\ 1 \rightarrow Z \end{array}$							
Status Affected: Z								
Encoding:	0000	011f	ffff					
Description:	The contents of register 'f' are cleared and the Z bit is set.							
Words:	1							
Cycles:	1							
Example:	CLRF	FLAG_RE	G					
Before Instru FLAG_RI After Instructi	ction EG = Ion	0x5A						
FLAG_RI	EG =	0x00						
Z	=	1						

CLRW	Clear W
Syntax:	[label] CLRW
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow (W); \\ 1 \rightarrow Z \end{array}$
Status Affected:	Z
Encoding:	0000 0100 0000
Description:	The W register is cleared. Zero bit (Z) is set.
Words:	1
Cycles:	1
Example:	CLRW
VV = After Instruct W = Z =	= 0x5A tion = 0x00 = 1
CLRWDT	Clear Watchdog Timer
CLRWDT Syntax:	Clear Watchdog Timer
CLRWDT Syntax: Operands:	Clear Watchdog Timer [<i>label</i>] CLRWDT None
CLRWDT Syntax: Operands: Operation:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow \overline{TO};$ $1 \rightarrow \overline{PD}$
CLRWDT Syntax: Operands: Operation: Status Affected:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow \overline{TO};$ $1 \rightarrow \overline{PD}$ $\overline{TO}, \overline{PD}$
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding:	Clear Watchdog Timer[label]CLRWDTNone $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ \overline{TO}, PD 0000 0000
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description:	Clear Watchdog Timer[label] CLRWDTNone $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0100 The CLRWDT instruction resets theWDT. It also resets the prescaler, ifthe prescaler is assigned to theWDT and not Timer0. Status bitsTO and PD are set.
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description: Words:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0000 0100 The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set. 1
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	Clear Watchdog Timer [label] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0000 0100 The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set. 1 1
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0000 0100 The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set. 1 1 CLRWDT

After Instruction		
WDT counter	=	0x00
WDT prescaler	=	0
TO	=	1
PD	=	1

12.2 DC Characteristics: PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial					
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions	
D001	Vdd	Supply Voltage PIC16C5X-RCI PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-HSI	3.0 3.0 4.5 4.5		6.25 6.25 5.5 5.5 6.25	V V V V		
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	2.5	1.5*		V	Device in SLEEP mode	
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset	
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset	
D010	IDD	Supply Current ⁽²⁾ PIC16C5X-RCI ⁽³⁾ PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-HSI PIC16C5X-LPI		1.8 1.8 4.8 4.8 9.0 15	3.3 3.3 10 10 20 40	mA mA mA mA μA	Fosc = 4 MHz, VDD = $5.5V$ Fosc = 4 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 20 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $3.0V$, WDT disabled	
D020	IPD	Power-down Current ⁽²⁾	_	4.0 0.6	14 12	μΑ μΑ	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled	

* These parameters are characterized but not tested.

- † Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 PIC16LCR54A-04I (Commercial, Industrial)				$\begin{array}{llllllllllllllllllllllllllllllllllll$					
PIC16CR54A-04, 10, 20 PIC16CR54A-04I, 10I, 20I (Commercial, Industrial)			$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$						
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions		
	Vdd	Supply Voltage							
D001		PIC16LCR54A	2.0		6.25	V			
D001 D001A		PIC16CR54A	2.5 4.5		6.25 5.5	V V	RC and XT modes HS mode		
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾		1.5*	_	V	Device in SLEEP mode		
D003	Vpor	VDD Start Voltage to ensure Power-on Reset	_	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	Svdd	VDD Rise Rate to ensure Power-on Reset	0.05*		—	V/ms	See Section 5.1 for details on Power-on Reset		
	IDD	Supply Current ⁽²⁾							
D005		PICLCR54A	—	10	20 70	μA μA	Fosc = 32 kHz, VDD = 2.0V Fosc = 32 kHz, VDD = 6.0V		
D005A		PIC16CR54A		2.0 0.8 90 4.8	3.6 1.8 350 10	mA mA μA	RC ⁽³⁾ and XT modes: Fosc = 4.0 MHz, VDD = 6.0V Fosc = 4.0 MHz, VDD = 3.0V Fosc = 200 kHz, VDD = 2.5V HS mode: Fosc = 10 MHz, VDD = 5.5V		
			—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5 V		

Legend: Rows with standard voltage device data only are shaded for improved readability.

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

- 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

PIC16C5X

FIGURE 14-2: TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 20 PF Typical: statistical mean @ 25°C Maximum: mean + 3s (-40°C to 125°C) Minimum: mean – 3s (-40°C to 125°C) 5.5 R = 3.3K5.0 4.5 R = 5K 4.0 3.5 Fosc (MHz) 3.0 R = 10K 2.5 2.0 Measured on DIP Packages, $T = 25^{\circ}C$ 1.5 1.0 R = 100K 0.5 0.0 3.0 3.5 4.0 4.5 5.0 5.5 6.0 VDD (Volts)

FIGURE 14-3:

TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 100 PF



FIGURE 14-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED



FIGURE 14-7: TYPICA

TYPICAL IPD vs. VDD, WATCHDOG ENABLED



FIGURE 14-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED



IPD, with WDT enabled, has two components: The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At -40° C, the latter dominates explaining the apparently anomalous behavior.





15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04 PIC16LC54A-04I (Commercial, Industrial)				ard Ope ting Tem	perating	J Condi ure 	tions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $40^{\circ}C \le TA \le +85^{\circ}C$ for industrial	
PIC16C54A-04, 10, 20 PIC16C54A-04I, 10I, 20I (Commercial, Industrial)				$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$				
Param No.	Symbol	Characteristic/Device	Min	Тур†	Мах	Units	Conditions	
	IPD	Power-down Current ⁽²⁾						
D006		PIC16LC5X	—	2.5	12	μΑ	VDD = 2.5V, WDT enabled, Commercial	
			—	0.25	4.0	μΑ	VDD = 2.5V, WDT disabled, Commercial	
			_	0.25	5.0	μΑ μΑ	VDD = 2.5V, WDT enabled, industrial $VDD = 2.5V$, WDT disabled, Industrial	
D006A		PIC16C5X	_	4.0	12	μΑ	VDD = 3.0V, WDT enabled, Commercial	
			—	0.25	4.0	μA	VDD = 3.0V, WDT disabled, Commercial	
			—	5.0	14	μΑ	VDD = 3.0V, WDT enabled, Industrial	
				0.3	5.0	μA	$v \Box U = 3.0v, v U T uisabled, industrial$	

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .



FIGURE 16-21: PORTA, B AND C IOH vs. VOH, VDD = 5V



17.3 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial, Extended) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial, Extended) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

DC CH	ARACTE	RISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for extended} \end{array}$				
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
D030	VIL	Input Low Voltage I/O Ports I/O Ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss Vss Vss	 	0.8 V 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V V	4.5V <v<sub>DD ≤ 5.5V Otherwise RC mode only⁽³⁾ XT, HS and LP modes</v<sub>
D040	Vih	Input High Voltage I/O ports I/O ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	2.0 0.25 Vdd+0.8 0.85 Vdd 0.85 Vdd 0.85 Vdd 0.85 Vdd 0.7 Vdd	 	Vdd Vdd Vdd Vdd Vdd Vdd Vdd	V V V V V	4.5V < V _{DD} ≤ 5.5V Otherwise RC mode only ⁽³⁾ XT, HS and LP modes
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	—	_	V	
D060	lı∟	Input Leakage Current ^(1,2) I/O ports	-1.0	0.5	+1.0	μA	For VDD \leq 5.5V: VSS \leq VPIN \leq VDD, pin at hi-impedance
		MCLR MCLR T0CKI OSC1	-5.0 -3.0 -3.0	— 0.5 0.5 0.5	+5.0 +3.0 +3.0 —	μΑ μΑ μΑ μΑ	$VPIN = VSS +0.25V$ $VPIN = VDD$ $VSS \le VPIN \le VDD$ $VSS \le VPIN \le VDD,$ $XT, HS and LP modes$
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5 V IOL = 1.6 mA, VDD = 4.5 V, RC mode only
D090	Vон	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	Vdd - 0.7 Vdd - 0.7			V V	IOH = -5.4 mA, VDD = 4.5 V IOH = -1.0 mA, VDD = 4.5 V, RC mode only

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
 - **2:** Negative current is defined as coming out of the pin.
 - 3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics		$\begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for extended} \end{array}$						
Param No.	Symbol	Characteristic	Min Typ† Max Units		Conditions			
2	Тсу	Instruction Cycle Time ⁽²⁾	—	4/Fosc				
3	TosL, TosH	Clock in (OSC1) Low or High	50*		_	ns	XT oscillator	
		Time	20*	—	_	ns	HS oscillator	
			2.0*	—	_	μS	LP oscillator	
4	TosR, TosF	Clock in (OSC1) Rise or Fall	-		25*	ns	XT oscillator	
		Time	—	—	25*	ns	HS oscillator	
			—	—	50*	ns	LP oscillator	

- * These parameters are characterized but not tested.
- † Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- **Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 17-9: TIMER0 CLOCK TIMINGS - PIC16C5X, PIC16CR5X



TABLE 17-4: TIMER0 CLOCK REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Chara	icteristics Operating Tempera	ture 0°C ≤ -40°C ≤ -40°C ≤ -40°C ≤	Ta ≤ +7 Ta ≤ +8 Ta ≤ +1	0°C fo 5°C fo 25°C f	r comm r indust or exter	nercial rial nded
Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions
Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 Tcy + 20*			ns	
	- With Prescaler	10*		_	ns	
TtOL	T0CKI Low Pulse Width - No Prescaler	0.5 Tcy + 20*			ns	
	- With Prescaler	10*	_	_	ns	
Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> * N		_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)
	Symbol Tt0H Tt0L Tt0P	Symbol Characteristic Tt0H T0CKI High Pulse Width - No Prescaler - With Prescaler Tt0L T0CKI Low Pulse Width - No Prescaler - With Prescaler Tt0P T0CKI Period	SymbolCharacteristics $-40^{\circ}C \leq -40^{\circ}C < -40^{\circ}C \leq -40^{\circ}C < -40^{\circ}C $	-40°C \leq TA \leq +8 -40°C \leq TA \leq +1SymbolCharacteristicMinTyptTt0HT0CKI High Pulse Width - No Prescaler0.5 Tcy + 20* With Prescaler10*-Tt0LT0CKI Low Pulse Width - No Prescaler0.5 Tcy + 20* With Prescaler10* With Prescaler10* With Prescaler10* With Prescaler10* Tt0PT0CKI Period20 or Tcy + 40* N-	-40°C \leq TA \leq +85°C fo -40°C \leq TA \leq +125°C fSymbolCharacteristicMinTyp†MaxTt0HT0CKI High Pulse Width - No Prescaler0.5 TCY + 20*With Prescaler10*Tt0LT0CKI Low Pulse Width - No Prescaler0.5 TCY + 20*Tt0LT0CKI Low Pulse Width - No Prescaler0.5 TCY + 20*Tt0PT0CKI Period20 or TCY + 40* N	-40°C \leq TA \leq +85°C for indust -40°C \leq TA \leq +125°C for exterSymbolCharacteristicMinTyp†MaxUnitsTt0HTOCKI High Pulse Width - No Prescaler - With Prescaler0.5 TCY + 20*nsTt0LTOCKI Low Pulse Width - No Prescaler - With Prescaler0.5 TCY + 20*nsTt0LTOCKI Low Pulse Width - No Prescaler - With Prescaler0.5 TCY + 20*nsTt0PTOCKI Period20 or TCY + 40*nsTt0PTOCKI Period20 or TCY + 40* Nns

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-6: TIMER0 CLOCK TIMINGS - PIC16C5X-40



TABLE 19-4: TIMER0 CLOCK REQUIREMENTS PIC16C5X-40

AC CharacteristicsStandard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial							ecified) rcial
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width					
		- No Prescaler	0.5 Tcy + 20*	—	—	ns	
		- With Prescaler	10*	_	_	ns	
41	Tt0L	T0CKI Low Pulse Width					
		- No Prescaler	0.5 Tcy + 20*	—	—	ns	
		- With Prescaler	10*	_	_	ns	
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> * N	_	_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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