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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c56a-04-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTES:

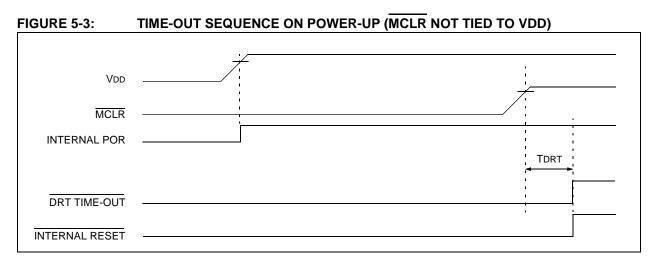
Pin Name	Pi	in Numb	er	Pin	Buffer	Description
Pin Name	DIP	SOIC	SSOP	Туре	Туре	Description
RA0	6	6	5	I/O	TTL	Bi-directional I/O port
RA1	7	7	6	I/O	TTL	
RA2	8	8	7	I/O	TTL	
RA3	9	9	8	I/O	TTL	
RB0	10	10	9	I/O	TTL	Bi-directional I/O port
RB1	11	11	10	I/O	TTL	
RB2	12	12	11	I/O	TTL	
RB3	13	13	12	I/O	TTL	
RB4	14	14	13	I/O	TTL	
RB5	15	15	15	I/O	TTL	
RB6	16	16	16	I/O	TTL	
RB7	17	17	17	I/O	TTL	
RC0	18	18	18	I/O	TTL	Bi-directional I/O port
RC1	19	19	19	I/O	TTL	
RC2	20	20	20	I/O	TTL	
RC3	21	21	21	I/O	TTL	
RC4	22	22	22	I/O	TTL	
RC5	23	23	23	I/O	TTL	
RC6	24	24	24	I/O	TTL	
RC7	25	25	25	I/O	TTL	
TOCKI	1	1	2	Ι	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in use, to reduce current consumption.
MCLR	28	28	28	I	ST	Master clear (RESET) input. This pin is an active low RESET to the device.
OSC1/CLKIN	27	27	27	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	26	26	26	0	_	Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
Vdd	2	2	3,4	Р	_	Positive supply for logic and I/O pins.
Vss	4	4	1,14	Р		Ground reference for logic and I/O pins.
N/C	3,5	3,5		_		Unused, do not connect.

### TABLE 3-2: PINOUT DESCRIPTION - PIC16C55, PIC16C57, PIC16CR57

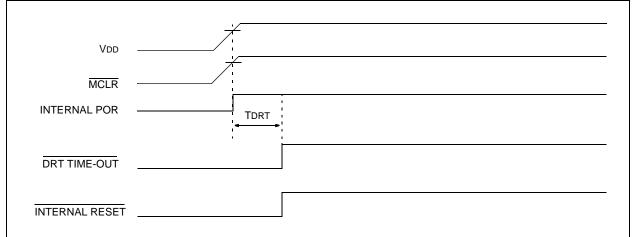
Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

NOTES:

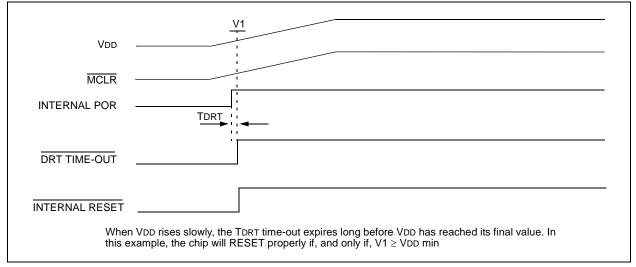
# PIC16C5X



# FIGURE 5-4: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME



# FIGURE 5-5: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): SLOW VDD RISE TIME



### 6.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers and General Purpose Registers.

The Special Function Registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Purpose Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

For the PIC16C54, PIC16CR54, PIC16C56 and PIC16CR56, the register file is composed of 7 Special Function Registers and 25 General Purpose Registers (Figure 6-4).

For the PIC16C55, the register file is composed of 8 Special Function Registers and 24 General Purpose Registers.

For the PIC16C57 and PIC16CR57, the register file is composed of 8 Special Function Registers, 24 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-5).

For the PIC16C58 and PIC16CR58, the register file is composed of 7 Special Function Registers, 25 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-6).

### 6.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the File Select Register (FSR). The FSR Register is described in Section 6.7.

### FIGURE 6-4: PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56 REGISTER



### 12.3 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended						
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions	
D001	Vdd	Supply Voltage PIC16C5X-RCE PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-LPE	3.25 3.25 4.5 4.5 2.5		6.0 6.0 5.5 5.5 6.0	V V V V		
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	—	1.5*	—	V	Device in SLEEP mode	
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset	
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*		_	V/ms	See Section 5.1 for details on Power-on Reset	
D010	IDD	Supply Current <sup>(2)</sup> PIC16C5X-RCE <sup>(3)</sup> PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-HSE PIC16C5X-LPE		1.8 1.8 4.8 4.8 9.0 19	3.3 3.3 10 10 20 55	mA mA mA mA μA	Fosc = 4 MHz, VDD = $5.5V$ Fosc = 4 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 16 MHz, VDD = $5.5V$ Fosc = $32$ kHz, VDD = $3.25V$ , WDT disabled	
D020	Ipd	Power-down Current <sup>(2)</sup>	—	5.0 0.8	22 18	μΑ μΑ	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled	

\* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k $\Omega$ .

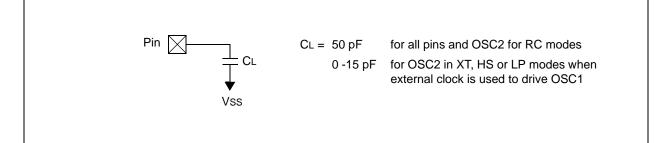
# 13.5 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

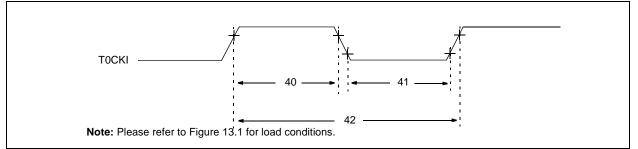
1. TppS2ppS

2. Tp	ρS	
Т		
F	Frequency	T Time
Lowe	ercase letters (pp) and their meanings:	
рр		
2	to	mc MCLR
ck	CLKOUT	osc oscillator
су	cycle time	os OSC1
drt	device reset timer	t0 T0CKI
io	I/O port	wdt watchdog timer
Uppe	ercase letters and their meanings:	
S		
F	Fall	P Period
н	High	R Rise
T	Invalid (Hi-impedance)	V Valid
L	Low	Z Hi-impedance

### FIGURE 13-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16CR54A



### FIGURE 13-5: TIMER0 CLOCK TIMINGS - PIC16CR54A



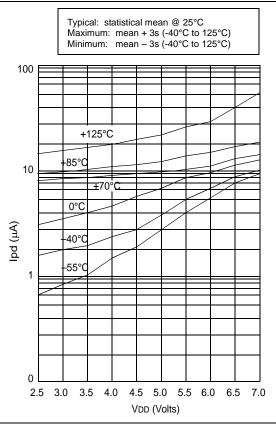
### TABLE 13-4: TIMER0 CLOCK REQUIREMENTS - PIC16CR54A

AC Characteristics			$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^\circ C \leq TA \leq +70^\circ C \mbox{ for commercial} \\ -40^\circ C \leq TA \leq +85^\circ C \mbox{ for industrial} \\ -40^\circ C \leq TA \leq +125^\circ C \mbox{ for extended} \end{array}$							
Param No.	Symbol		Characteristic	Min	Тур†	Max	Units	Conditions		
40	Tt0H	T0CKI High	Pulse Width - No Prescaler - With Prescaler	0.5 Tcy + 20* 10*		_	ns ns			
41	TtOL	T0CKI Low	Pulse Width - No Prescaler - With Prescaler	0.5 Tcy + 20* 10*			ns ns	-		
42	Tt0P	T0CKI Perio	od	20 or <u>Tcy + 40</u> * N		—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)		

These parameters are characterized but not tested.

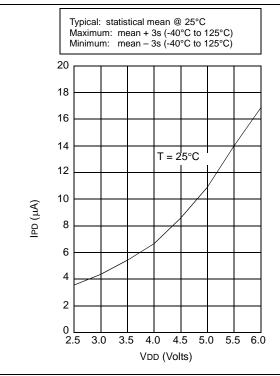
† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

### FIGURE 14-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED

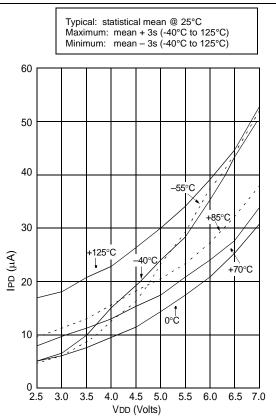


# FIGURE 14-7: T

### TYPICAL IPD vs. VDD, WATCHDOG ENABLED



### FIGURE 14-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED



IPD, with WDT enabled, has two components: The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At  $-40^{\circ}$ C, the latter dominates explaining the apparently anomalous behavior.

# 15.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings <sup>(†)</sup>	
Ambient temperature under bias	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on VDD with respect to Vss	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	–0.6V to (VDD + 0.6V)
Total power dissipation <sup>(1)</sup>	800 mW
Max. current out of Vss pin	150 mA
Max. current into Vod pin	100 mA
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, Iik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)	
Max. output current sunk by any I/O pin	25 mA
Max. output current sourced by any I/O pin	20 mA
Max. output current sourced by a single I/O port (PORTA or B)	50 mA
Max. output current sunk by a single I/O port (PORTA or B)	50 mA
<b>Note 1:</b> Power dissipation is calculated as follows: Pdis = VDD x {IDD - $\sum$ IOH} + $\sum$ {(VD	D-VOH) X IOH} + $\Sigma$ (VOL X IOL)

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 15-1:	EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A
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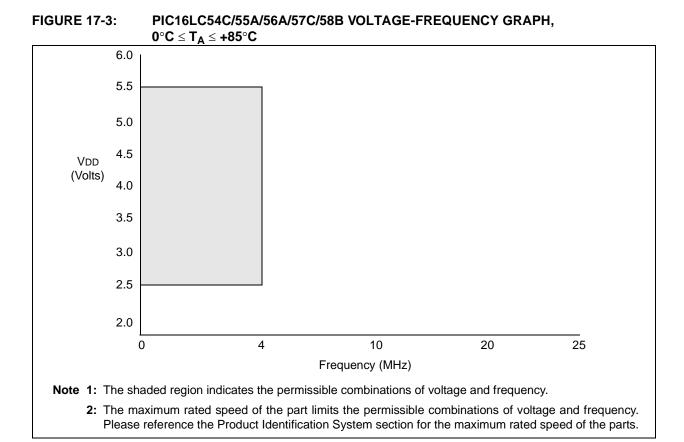
AC Chara	acteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions		
1	Tosc	External CLKIN Period <sup>(1)</sup>	250	_		ns	XT OSC mode		
			500	—	—	ns	XT osc mode (PIC16LV54A)		
			250	—	—	ns	HS osc mode (04)		
			100	—	—	ns	HS osc mode (10)		
			50	—	—	ns	HS osc mode (20)		
			5.0	_		μs	LP OSC mode		
		Oscillator Period <sup>(1)</sup>	250	_	_	ns	RC osc mode		
			500	—	—	ns	RC osc mode (PIC16LV54A)		
			250	—	10,000	ns	XT osc mode		
			500	—	—	ns	XT osc mode (PIC16LV54A)		
			250	—	250	ns	HS osc mode (04)		
			100	—	250	ns	HS osc mode (10)		
			50	—	250	ns	HS osc mode (20)		
			5.0	_	200	μs	LP OSC mode		
2	Тсу	Instruction Cycle Time <sup>(2)</sup>	—	4/Fosc	—	—			
3	TosL, TosH	Clock in (OSC1) Low or	85*	_	—	ns	XT oscillator		
		High Time	20*	—	—	ns	HS oscillator		
			2.0*	—	—	μS	LP oscillator		
4	TosR, TosF	Clock in (OSC1) Rise or	—	_	25*	ns	XT oscillator		
		Fall Time	—	—	25*	ns	HS oscillator		
			—	—	50*	ns	LP oscillator		

\* These parameters are characterized but not tested.

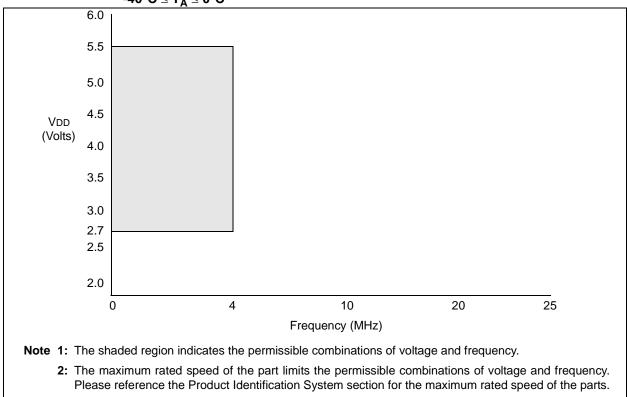
† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TcY) equals four times the input oscillator time base period.







### 17.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial)				$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array} $						
PIC16C5X PIC16CR5X (Commercial, Industrial)				$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^\circ C \leq TA \leq +70^\circ C \mbox{ for commercial} \\ -40^\circ C \leq TA \leq +85^\circ C \mbox{ for industrial} \end{array}$						
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions			
	IPD	Power-down Current <sup>(2)</sup>								
D020		PIC16LC5X		0.25 0.25 1	2 3 5	μΑ μΑ μΑ	VDD = 2.5V, WDT disabled, Commercial $VDD = 2.5V$ , WDT disabled, Industrial $VDD = 2.5V$ , WDT enabled, Commercial			
			_	1.25	8	μA	$V_{DD} = 2.5V, WDT$ enabled, Industrial			
D020A		PIC16C5X	 	0.25 0.25 1.8 2.0 4	4.0 5.0 7.0* 8.0* 12*	μΑ μΑ μΑ μΑ	VDD = 3.0V, WDT disabled, Commercial VDD = 3.0V, WDT disabled, Industrial VDD = 5.5V, WDT disabled, Commercial VDD = 5.5V, WDT disabled, Industrial VDD = 3.0V, WDT enabled, Commercial			
			—	4	14*	μA	VDD = 3.0V, WDT enabled, Industrial			
			_	9.8 12	27* 30*	μΑ μΑ	VDD = 5.5V, WDT enabled, Commercial VDD = 5.5V, WDT enabled, Industrial			

Legend: Rows with standard voltage device data only are shaded for improved readability.

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k $\Omega$ .

# 17.4 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS

2. Tp	pS	
Т		
F	Frequency	T Time
Lowe	ercase letters (pp) and their meanings:	
рр		
2	to	mc MCLR
ck	CLKOUT	osc oscillator
су	cycle time	os OSC1
drt	device reset timer	t0 T0CKI
io	I/O port	wdt watchdog timer
Uppe	ercase letters and their meanings:	
S		
F	Fall	P Period
н	High	R Rise
T	Invalid (Hi-impedance)	V Valid
L	Low	Z Hi-impedance

### FIGURE 17-5: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS -PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B-04, 20





FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 PF, 25°C

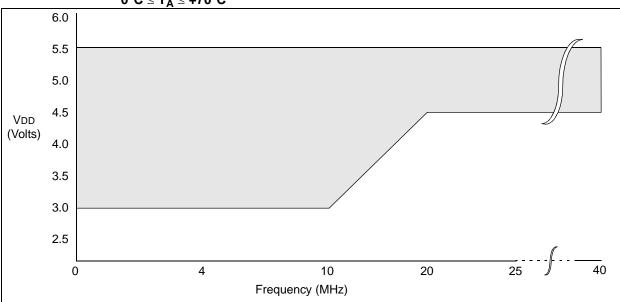




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# PIC16C5X

FIGURE 19-1: PIC16C54C/C55A/C56A/C57C/C58B-40 VOLTAGE-FREQUENCY GRAPH,  $0^{\circ}C \le T_A \le +70^{\circ}C$ 





- **2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
- **3:** Operation between 20 to 40 MHz requires the following:
  - VDD between 4.5V. and 5.5V
  - OSC1 externally driven
  - OSC2 not connected
  - HS mode
  - Commercial temperatures

Devices qualified for 40 MHz operation have -40 designation (ex: PIC16C54C-40/P).

4: For operation between DC and 20 MHz, see Section 17.1.

FIGURE 20-4: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. VDD

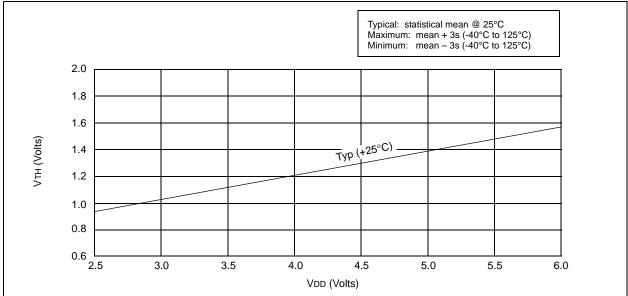
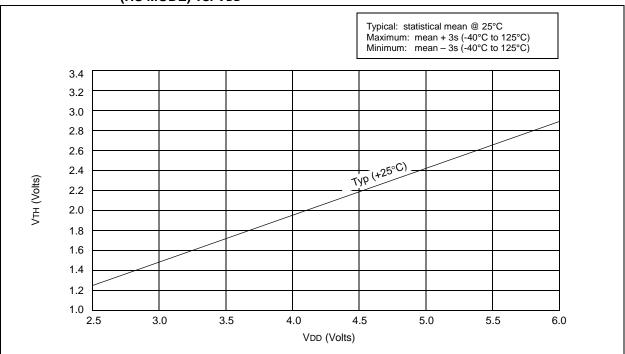


FIGURE 20-5: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (HS MODE) vs. VDD



# 21.0 PACKAGING INFORMATION

## 21.1 Package Marketing Information

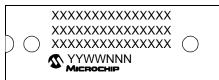
### 18-Lead PDIP



### 28-Lead Skinny PDIP (.300")



### 28-Lead PDIP (.600")



### 18-Lead SOIC



### 28-Lead SOIC

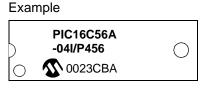


### 20-Lead SSOP



### 28-Lead SSOP

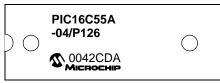




### Example



### Example



## Example



## Example



### Example

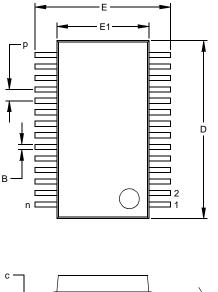


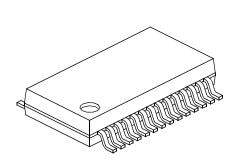
### Example

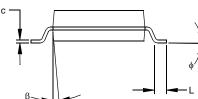


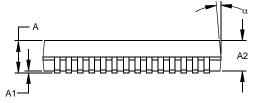
### 28-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









	Units		INCHES		MILLIMETERS*			
Dimensio	n Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28		
Pitch	р		.026			0.65		
Overall Height	А	.068	.073	.078	1.73	1.85	1.98	
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83	
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25	
Overall Width	Е	.299	.309	.319	7.59	7.85	8.10	
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38	
Overall Length	D	.396	.402	.407	10.06	10.20	10.34	
Foot Length	L	.022	.030	.037	0.56	0.75	0.94	
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25	
Foot Angle	ф	0	4	8	0.00	101.60	203.20	
Lead Width	В	.010	.013	.015	0.25	0.32	0.38	
Mold Draft Angle Top	α	0	5	10	0	5	10	
Mold Draft Angle Bottom	β	0	5	10	0	5	10	

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-150 Drawing No. C04-073

## **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	- <u>xx</u>	Ť	<u>/xx</u>	<u>xxx</u>	Exa	nples	S:
Device	Frequency Range/OSC Type           PIC16C54           PIC16C54A           PIC16C54C           PIC16C55A           PIC16C55A           PIC16C55A           PIC16C56A           PIC16C56A           PIC16C57C           PIC16C57C           PIC16C58B           PIC16C58B	Temperature Range	$\begin{array}{c} -(2) \\ \lambda_{T}(2) \\ (2) \\ C_{T}(2) \\ C_{T}(2) \\ 2) \\ -(2) \\ -(2) \\ \lambda_{T}(2) \\ 2) \\ -(2) \\ C_{T}(2) \\ C_{T}(2) \\ -(2) \\ -(2) \\ C_{T}(2) \\ -(2)$	Pattern	a) b) c) d) Note	PDIP QTP PIC16 packa PIC16 cial te dard ' PIC1 temp MHz, #123	C = normal voltage range LC = extended
Frequency Range/ Oscillator Type	04 200 KHz (LI 10 10 MHz (HS 20 20 MHz (HS 40 40 MHz (HS b <sup>(4)</sup> No oscillato *RC/LP/XT/HS a -02 is available for -04/10/20 options	Crystal ystal/Resonator Crystal P) or 2 MHz (XT an P) or 4 MHz (XT an conly) conly) conly) r type for JW packa re for 16C54/55/56/	nd RC) ages <sup>(3)</sup> /57 devices on all other device	S		3:	T = in tape and reel - SOIC and SSOP packages only JW Devices are UV erasable and can be programmed to any device configura- tion. JW Devices meet the electrical requirements of each oscillator type, including LC devices. b = Blank
Temperature Range	$b^{(4)} = 0^{\circ}C$ $I = -40^{\circ}C$ $E = -40^{\circ}C$	to +85°C					
Package	JW = 28-pin DIP <sup>(3)</sup> P = 28-pin SO = 300 m SS = 209 m SP = 28-pin	Waffle Pack 600 mil/18-pin 300 il SOIC il SSOP 300 mil Skinny PD for additional packa	0 mil PDIP DIP				
Pattern		I code (factory spe lank for OTP and W					

### Sales and Support

#### **Data Sheets**

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office

2. The Microchip Worldwide Site (www.microchip.com)