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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c56a-40-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTES:



FIGURE 3-1: PIC16C5X SERIES BLOCK DIAGRAM

4.4 RC Oscillator

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 4-5 shows how the R/C combination is connected to the PIC16C5X. For REXT values below 2.2 k Ω , the oscillator operation may become unstable, or stop completely. For very high REXT values (e.g., 1 M Ω) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping REXT between 3 k Ω and 100 k Ω .

Although the oscillator will operate with no external capacitor (CEXT = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications sections for variation of oscillator frequency due to VDD for given REXT/ CEXT values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic.



Note: If you change from this device to another device, please verify oscillator characteristics in your application.

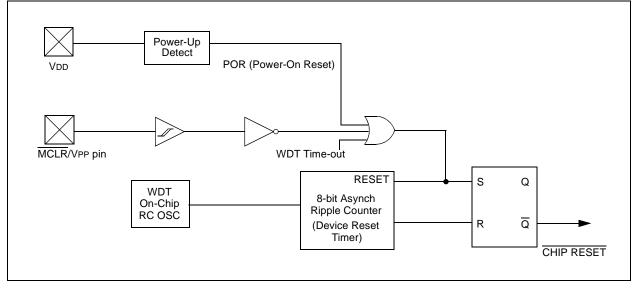
TABLE 5-3: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-On Reset	MCLR or WDT Reset
W	N/A	XXXX XXXX	uuuu uuuu
TRIS	N/A	1111 1111	1111 1111
OPTION	N/A	11 1111	11 1111
INDF	00h	XXXX XXXX	uuuu uuuu
TMR0	01h	XXXX XXXX	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000q quuu
FSR ⁽¹⁾	04h	1xxx xxxx	luuu uuuu
PORTA	05h	xxxx	uuuu
PORTB	06h	XXXX XXXX	uuuu uuuu
PORTC ⁽²⁾	07h	XXXX XXXX	uuuu uuuu
General Purpose Register Files	07-7Fh	XXXX XXXX	սսսս սսսս

Legend: x = unknown u = unchanged - = unimplemented, read as '0'<math>q = see tables in Table 5-1 for possible values.

- Note 1: These values are valid for PIC16C57/CR57/CR58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for MCLR and WDT Reset, the value is 111u uuuu.
 - **2:** General purpose register file on PIC16C54/CR54/C56/CR56/C58/CR58.

FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



6.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not

writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as $000u \ u1uu$ (where u = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 10.0, Instruction Set Summary.

REGISTER 6-1: STATUS REGISTER (ADDRESS: 03h)

	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x	
	PA2	PA1	PA0	TO	PD	Z	DC	С	
	bit 7							bit 0	
bit 7:	PA2: This bit	unused at th	is time.						
		A2 bit as a ge with future pr		e read/write	bit is not recor	mmended, sir	nce this may a	affect upward	
bit 6-5:				-	CR56)(PIC16			58)	
					16C57/CR57, 16C57/CR57,				
		(400h - 5FFh				FIC 10C30/C	N00		
	11 = Page 3	(600h - 7FFh							
	Each page is		deperal pur	ose read/wr	ite bits in devi	ices which do	not use them	for program	
					affect upward				
bit 4:	TO: Time-ou			,	•				
		ver-up, CLRWI ime-out occur		, or sleep i	nstruction				
bit 3:	PD: Power-d	lown bit							
	•	ver-up or by tl ution of the SI							
bit 2:	Z: Zero bit								
		lt of an arithm It of an arithm							
bit 1:	DC: Digit car	ry/borrow bit	(for ADDWF a	nd SUBWF in	structions)				
	ADDWF								
		rom the 4th lo							
	 0 = A carry from the 4th low order bit of the result did not occur SUBWF 								
	1 = A borrow from the 4th low order bit of the result did not occur 0 = A borrow from the 4th low order bit of the result occurred								
bit 0:	•	row bit (for AI			F instructions		_		
	ADDWF 1 = A carry o	ocurred		orrow did n	ot occur	RRF or RLI		, respectively	
	$\pm = \pi \operatorname{carry} 0$	locurrou	/ · ·						

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

6.5.1 PAGING CONSIDERATIONS – PIC16C56/CR56, PIC16C57/CR57 AND PIC16C58/CR58

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS Register will not be updated. Therefore, the next GOTO, CALL or modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA<1:0>).

For example, a NOP at location 1FFh (page 0) increments the PC to 200h (page 1). A GOTO xxx at 200h will return the program to address xxh on page 0 (assuming that PA<1:0> are clear).

To prevent this, the page preselect bits must be updated under program control.

6.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the RESET vector).

The STATUS Register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a GOTO instruction at the RESET vector location will automatically cause the program to jump to page 0.

6.6 Stack

PIC16C5X devices have a 10-bit or 11-bit wide, two-level hardware push/pop stack.

A CALL instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W Register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the RETLW instruction, the PC is loaded with the Top of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC, therefore, paging is not an issue when returning from a subroutine.

8.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
 - Readable and writable
- 8-bit software programmable prescaler
- · Internal or external clock select
- Edge select for external clock

Figure 8-1 is a simplified block diagram of the Timer0 module, while Figure 8-2 shows the electrical structure of the Timer0 input.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 8-3 and Figure 8-4). The user can work around this by writing an adjusted value to the TMR0 register.



Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 8.1.

Note: The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both.

The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 8.2 details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 8-1.



FIGURE 8-2: ELECTRICAL STRUCTURE OF TOCKI PIN



9.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT Reset or Wake-up Reset generates a device RESET.

The $\overline{\text{TO}}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset (Section 6.3).

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 9.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

9.2.1 WDT PERIOD

An 8-bit counter is available as a prescaler for the Timer0 module (Section 8.2), or as a postscaler for the Watchdog Timer (WDT), respectively. For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not

both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio (Section 6.4).

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see Device Characterization).

Under worst case conditions (VDD = Min., Temperature = Max., WDT prescaler = 1:128), it may take several seconds before a WDT time-out occurs.

9.2.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction RESETS the WDT and the prescaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.

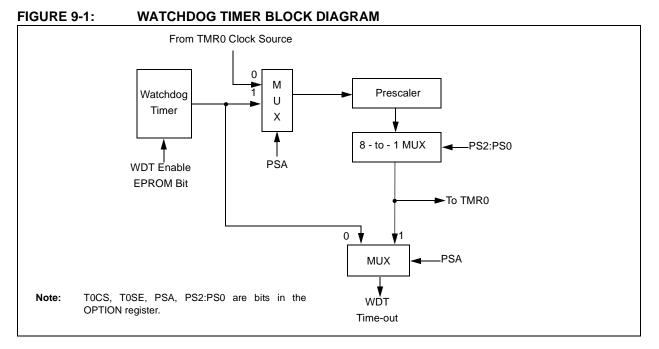


TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	<u>Value</u> on MCLR and WDT Reset
N/A	OPTION	—		Tosc	Tose	PSA	PS2	PS1	PS0	11 1111	11 1111

Legend: u = unchanged, - = unimplemented, read as '0'. Shaded cells not used by Watchdog Timer.

10.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 10-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers in that bank is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 10-1:	OPCODE FIELD
	DESCRIPTIONS

	DESCRIPTIONS
Field	Description
f	Register file address (0x00 to 0x1F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with $x = 0$. It is the recommended form of use for com-
	patibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
TO	Time-out bit
PD	Power-down bit
dest	Destination, either the W register or the specified register file location
[]	Options
()	Contents
\rightarrow	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time would be 1 μ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time would be 2 μ s.

Figure 10-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations							
<u>11 6</u>	5	4 0					
OPCODE	d	f (FILE #)					
d = 1 for destination	d = 0 for destination W d = 1 for destination f f = 5-bit file register address						
Bit-oriented file registe	r ope	erations					
11 8	7	5 4 0					
OPCODE	b (Bl	IT #) f (FILE #)					
Literal and control ope	f = 5-bit file register addressLiteral and control operations (except GOTO)						
11	8	7 0					
OPCODE		k (literal)					
k = 8-bit immedia	k = 8-bit immediate value						
Literal and control operations - GOTO instruction							
11	9	8 0					
OPCODE		k (literal)					
k = 9-bit immediate value							

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PIC16C5X

IORLW	Inclusive OR literal with W
Syntax:	[<i>label</i>] IORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .OR. (k) \rightarrow (W)
Status Affected:	Z
Encoding:	1101 kkkk kkkk
Description:	The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W regis- ter.
Words:	1
Cycles:	1
Example:	IORLW 0x35
Before Instru W = After Instruc W = Z =	0x9A tion

IORWF	Inclusive OR W with f
Syntax:	[<i>label</i>] IORWF f,d
Operands:	$\begin{array}{l} 0\leq f\leq 31\\ d\in [0,1] \end{array}$
Operation:	(W).OR. (f) \rightarrow (dest)
Status Affected:	Z
Encoding:	0001 00df ffff
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
Words:	1
Cycles:	1
Example:	IORWF RESULT, 0
Before Instru RESUL W After Instruct RESUL W Z	Γ = 0x13 = 0x91 tion

MOVF	Move f				
Syntax:	[<i>label</i>] MOVF f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$				
Operation:	$(f) \rightarrow (dest)$				
Status Affected:	Z				
Encoding:	0010 00df ffff				
Description:	The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.				
Words:	1				
Cycles:	1				
Example:	MOVF FSR, 0				
After Instruct W =	tion - value in FSR register				

MOVLW	Move Literal to W					
Syntax:	[label]	MOVLW	k			
Operands:	$0 \leq k \leq 2$	55				
Operation:	$k \rightarrow (W)$					
Status Affected:	None					
Encoding:	1100	kkkk	kkkk			
Description:	The eigh the W re		'k' is loaded	d into		
Words:	1					
Cycles:	1					
Example:	MOVLW	0x5A				
After Instruction W = 0x5A						

TABLE 11-1: DEVELOPMENT TOOLS FROM MICROCHIP

MPLA® Integrated V		
MPLAB [®] C17 C complex I	> > > > > > > > > >	
MPLAB [®] C18 C compiler Implement Implement </th <th>> > > > > > > ></th> <th></th>	> > > > > > > >	
MPASM™ Assembler/ MPLINK™ Object Linker C	> > >	
MPLAB® ICE In-Circuit Emulator //		>
ICEPIC** In-Circuit Emulator ✓ <td< th=""><th></th><th></th></td<>		
MPLAB® ICD In-Circuit *	· · ·	
PICSTART® Plus Entry Level	> 	
PRO MATE® II		
PICDEM™ 1 Demonstration </th <td></td> <td>></td>		>
PICDEM™ 2 Demonstration	>	
PICDEMTM 3 Demonstration Board Image: Control of the constration Image: Control of the constration PICDEMTM 14 Demonstration Image: Control of the constration Image: Control of the constration Image: Control of the constration PICDEMTM 17 Demonstration Image: Control of the constration ReeLoo® Transponder Kit Image: Control of the control of the constration Image: Control of the cont	>	
PICDEM TM 14A Demonstration Board PICDEM TM 17 Demonstration Board KEELoa [®] Evaluation Kit KEELoa [®] Transponder Kit microlD TM Programmer's Kit 125 kHz microlD TM	· ·	
	· ·	
		>
		>
		>
		>
125 kHz Anticollision microlD TM Developer's Kit		>
13.56 MHz Anticollision microlD TM Developer's Kit		>
MCP2510 CAN Developer's Kit		

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15.4 DC Characteristics: PIC16C54A-04, 10, 20, PIC16LC54A-04, PIC16LV54A-02 (Commercial) PIC16C54A-04I, 10I, 20I, PIC16LC54A-04I, PIC16LV54A-02I (Industrial) PIC16C54A-04I, 10I, 20I, PIC16LC54A-04I, PIC16LV54A-02I (Industrial) PIC16C54A-04E, 10E, 20E, PIC16LC54A-04E (Extended)

DC CH	ARACTE	RISTICS	Standard O Operating T		re 0°C ≤ 1 -40°C ≤ 1 -20°C ≤ 1	TA ≤ +70 TA ≤ +85 TA ≤ +85	s otherwise specified) ^{I°} C for commercial ^{I°} C for industrial [°] C for industrial-PIC16LV54A-02I 5°C for extended
Param No.	Symbol		Min	Тур†	Мах	Units	Conditions
D030	VIL	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes
D040	VIH	Input High Voltage I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	0.2 VDD + 1 2.0 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD	V V V V V V	For all V _{DD} ⁽⁴⁾ 4.0V < V _{DD} ≤ 5.5V ⁽⁴⁾ RC mode only ⁽³⁾ XT, HS and LP modes
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	_	—	V	
D060	IIL	Input Leakage Current ^(1,2) I/O ports MCLR MCLR TOCKI OSC1	-1.0 -5.0 -3.0 -3.0	0.5 0.5 0.5 0.5	+1.0 +5.0 +3.0 +3.0 —	μΑ μΑ μΑ μΑ μΑ	For VDD \leq 5.5V: VSS \leq VPIN \leq VDD, pin at hi-impedance VPIN = VSS +0.25V VPIN = VDD VSS \leq VPIN \leq VDD VSS \leq VPIN \leq VDD, XT, HS and LP modes
D080	VOL	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5 V IOL = 1.6 mA, VDD = 4.5 V, RC mode only
	VOH	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	Vdd - 0.7 Vdd - 0.7			V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, RC mode only

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

*

FIGURE 16-18: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

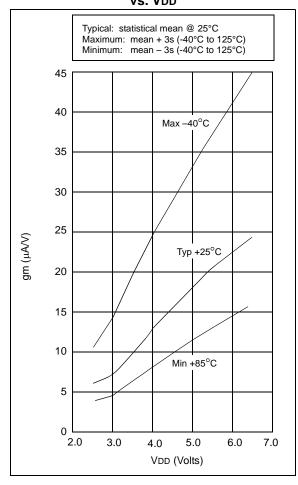
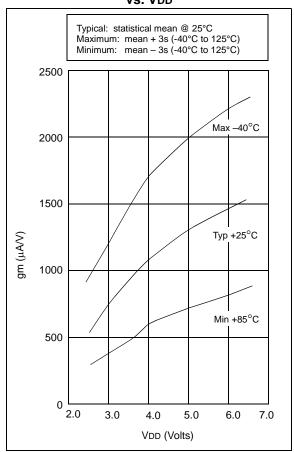


FIGURE 16-19:

TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD



17.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial)				Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrialStandard Operating Conditions (unless otherwise specified)						
PIC16C5X PIC16CR5X (Commercial, Industrial)				$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified O Operating Temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial $-40^{\circ}C \leq TA \leq +85^{\circ}C$ for industrial A of A $						
Param No.	Symbol	Characteristic/Device	Min Typ† Max Units			Units	Conditions			
	Vdd	Supply Voltage								
D001		PIC16LC5X	2.5 2.7 2.5		5.5 5.5 5.5	V V V	$\begin{array}{l} -40^{\circ}C \leq TA \leq +\ 85^{\circ}C,\ 16LCR5X \\ -40^{\circ}C \leq TA \leq 0^{\circ}C,\ 16LC5X \\ 0^{\circ}C \leq TA \leq +\ 85^{\circ}C\ 16LC5X \end{array}$			
D001A		PIC16C5X	3.0 4.5	_	5.5 5.5	V V	RC, XT, LP and HS mode from 0 - 10 MHz from 10 - 20 MHz			
D002	Vdr	RAM Data Retention Volt- age ⁽¹⁾	—	1.5*	_	V	Device in SLEEP mode			
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset			
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset			

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

FIGURE 17-9: TIMER0 CLOCK TIMINGS - PIC16C5X, PIC16CR5X

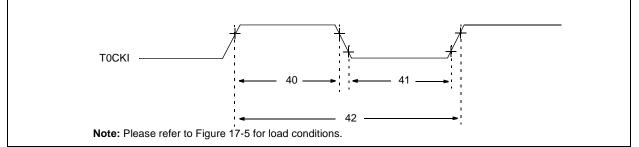


TABLE 17-4: TIMER0 CLOCK REQUIREMENTS - PIC16C5X, PIC16CR5X

ļ	AC CharacteristicsStandard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 Tcy + 20*		_	ns		
		- With Prescaler	10*	_	—	ns		
41	TtOL	T0CKI Low Pulse Width - No Prescaler	0.5 Tcy + 20*	_	_	ns		
		- With Prescaler	10*	_	_	ns		
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> * N	_	_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)	

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

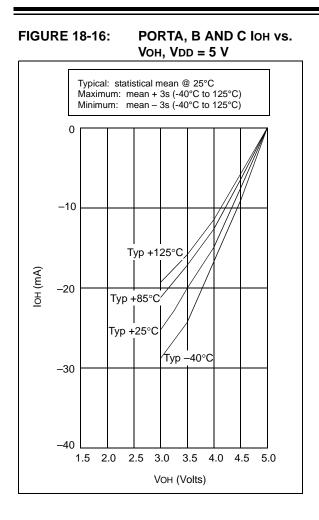
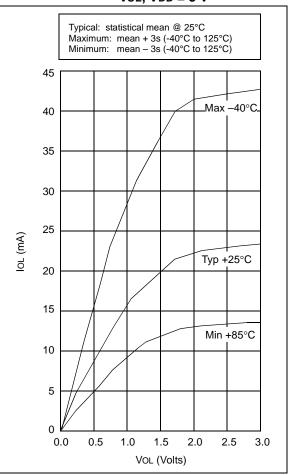


FIGURE 18-17: PORTA, B AND C IOL vs. Vol, VDD = 3 V



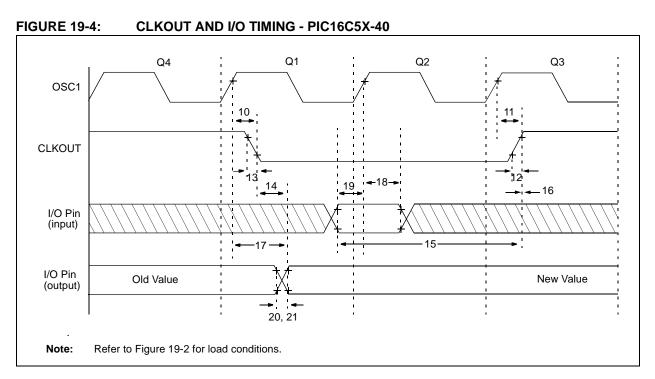


TABLE 19-2 :	CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X-40

AC Char	acteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$	otherwise spectrum D°C for commerce	•		
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ^(1,2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ^(1,2)	—	15	30**	ns
12	TckR	CLKOUT rise time ^(1,2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time ^(1,2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ^(1,2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT ^(1,2)	0.25 TCY+30*	—	_	ns
16	TckH2iol	Port in hold after CLKOUT ^(1,2)	0*	—	_	ns
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽²⁾	—	—	100	ns
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽²⁾	—	10	25**	ns

* These parameters are characterized but not tested.

- ** These parameters are design targets and are not tested. No characterization data available at this time.
- † Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Refer to Figure 19-2 for load conditions.

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FIGURE 19-6: TIMER0 CLOCK TIMINGS - PIC16C5X-40

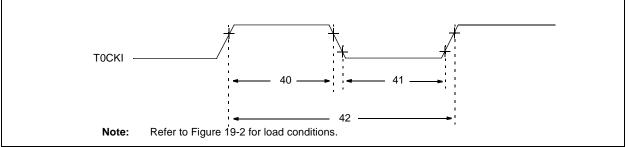


TABLE 19-4: TIMER0 CLOCK REQUIREMENTS PIC16C5X-40

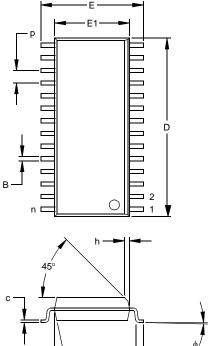
A	C Charac	teristics Standard Operati Operating Temper	U (,
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width					
		- No Prescaler	0.5 Tcy + 20*	—		ns	
		- With Prescaler	10*		—	ns	
41	Tt0L	T0CKI Low Pulse Width					
		- No Prescaler	0.5 TCY + 20*	—		ns	
		- With Prescaler	10*		—	ns	
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> * N	_	_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)

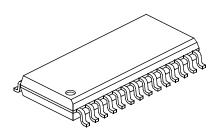
* These parameters are characterized but not tested.

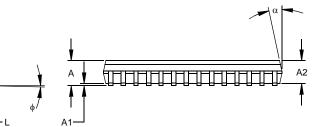
† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

28-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging







	Units		INCHES*		MILLIMETERS			
Dimensi	on Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28		
Pitch	р		.050			1.27		
Overall Height	А	.093	.099	.104	2.36	2.50	2.64	
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39	
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30	
Overall Width	E	.394	.407	.420	10.01	10.34	10.67	
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59	
Overall Length	D	.695	.704	.712	17.65	17.87	18.08	
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74	
Foot Length	L	.016	.033	.050	0.41	0.84	1.27	
Foot Angle Top	φ	0	4	8	0	4	8	
Lead Thickness	С	.009	.011	.013	0.23	0.28	0.33	
Lead Width	В	.014	.017	.020	0.36	0.42	0.51	
Mold Draft Angle Top	α	0	12	15	0	12	15	
Mold Draft Angle Bottom	β	0	12	15	0	12	15	

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013 Drawing No. C04-052

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	- <u>xx</u>	Ť	<u>/xx</u>	<u>xxx</u>	Exa	nples	S:
Device	Frequency Range/OSC Type PIC16C54 PIC16C54A PIC16C54C PIC16C55A PIC16C55A PIC16C55A PIC16C56A PIC16C56A PIC16C57C PIC16C57C PIC16C58B PIC16C58B	Temperature Range	$\begin{array}{c} -(2) \\ \lambda_{T}(2) \\ (2) \\ C_{T}(2) \\ C_{T}(2) \\ 2) \\ -(2) \\ -(2) \\ \lambda_{T}(2) \\ 2) \\ -(2) \\ C_{T}(2) \\ C_{T}(2) \\ -(2) \\ -(2) \\ C_{T}(2) \\ -(2)$	Pattern	a) b) c) d) Note	PDIP QTP PIC16 packa PIC16 cial te dard ' PIC1 temp MHz, #123	C = normal voltage range LC = extended
Frequency Range/ Oscillator Type	04 200 KHz (LI 10 10 MHz (HS 20 20 MHz (HS 40 40 MHz (HS b ⁽⁴⁾ No oscillato *RC/LP/XT/HS a -02 is available for -04/10/20 options	Crystal ystal/Resonator Crystal P) or 2 MHz (XT an P) or 4 MHz (XT an conly) conly) conly) r type for JW packa re for 16C54/55/56/	nd RC) ages ⁽³⁾ /57 devices on all other device	S		3:	T = in tape and reel - SOIC and SSOP packages only JW Devices are UV erasable and can be programmed to any device configura- tion. JW Devices meet the electrical requirements of each oscillator type, including LC devices. b = Blank
Temperature Range	$b^{(4)} = 0^{\circ}C$ $I = -40^{\circ}C$ $E = -40^{\circ}C$	to +85°C					
Package	JW = 28-pin DIP ⁽³⁾ P = 28-pin SO = 300 m SS = 209 m SP = 28-pin	Waffle Pack 600 mil/18-pin 300 600 mil/18-pin 300 il SOIC il SSOP 300 mil Skinny PD for additional packa	0 mil PDIP DIP				
Pattern		I code (factory spe lank for OTP and W					

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office

2. The Microchip Worldwide Site (www.microchip.com)