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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c56a-40-ss

4.0 OSCILLATOR CONFIGURATIONS

4.1 Oscillator Types

PIC16C5Xs can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:
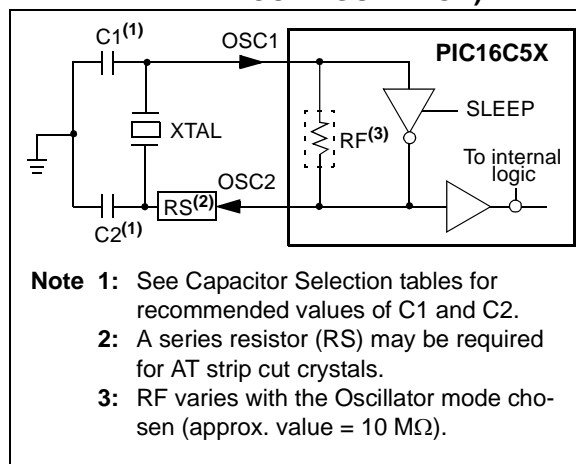
1. LP: Low Power Crystal
2. XT: Crystal/Resonator
3. HS: High Speed Crystal/Resonator
4. RC: Resistor/Capacitor

> **Note:** Not all oscillator selections available for all parts. See Section 9.1.
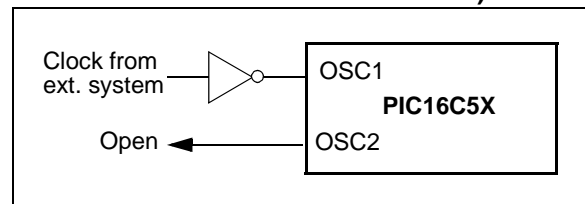
4.2 Crystal Oscillator/Ceramic Resonators

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 4-1). The PIC16C5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 4-2).

FIGURE 4-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)

Note 1: See Capacitor Selection tables for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF varies with the Oscillator mode chosen (approx. value = 10 MΩ).

FIGURE 4-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

TABLE 4-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC16C5X, PIC16CR5X

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	68-100 pF	68-100 pF
	2.0 MHz	15-33 pF	15-33 pF
	4.0 MHz	10-22 pF	10-22 pF
HS	8.0 MHz	10-22 pF	10-22 pF
	16.0 MHz	10 pF	10 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 4-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC16C5X, PIC16CR5X

Osc Type	Crystal Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz[1]	15 pF	15 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Note 1: For V_{DD} > 4.5V, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

> **Note:** If you change from this device to another device, please verify oscillator characteristics in your application.

NOTES:

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6.5   Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.

For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0> (Figure 6-7, Figure 6-8 and Figure 6-9).

For the PIC16C56, PIC16CR56, PIC16C57, PIC16CR57, PIC16C58 and PIC16CR58, a page number must be supplied as well. Bit5 and bit6 of the STATUS Register provide page information to bit9 and bit10 of the PC (Figure 6-8 and Figure 6-9).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 6-7 and Figure 6-8).

Instructions where the PCL is the destination, or modify PCL instructions, include MOVWF PCL, ADDWF PCL, and BSF PCL,5.
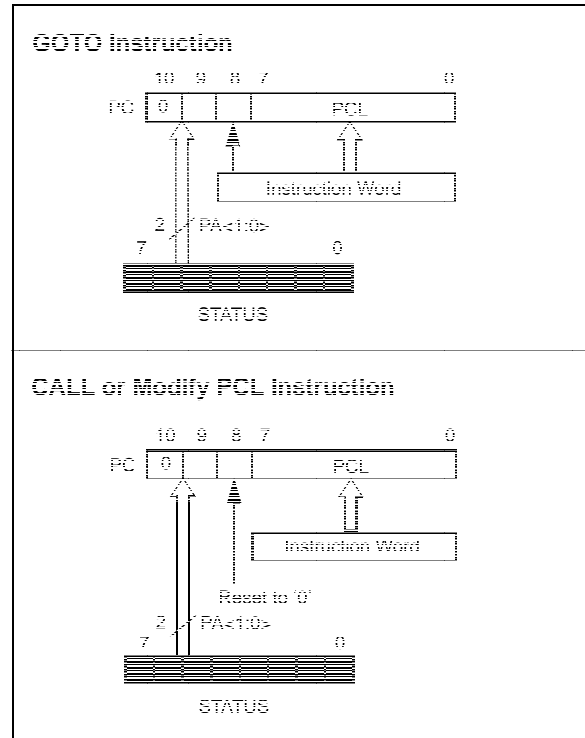
For the PIC16C56, PIC16CR56, PIC16C57, PIC16CR57, PIC16C58 and PIC16CR58, a page number again must be supplied. Bit5 and bit6 of the STATUS Register provide page information to bit9 and bit10 of the PC (Figure 6-8 and Figure 6-9).

> **Note:** Because PC<8> is cleared in the CALL instruction, or any modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).
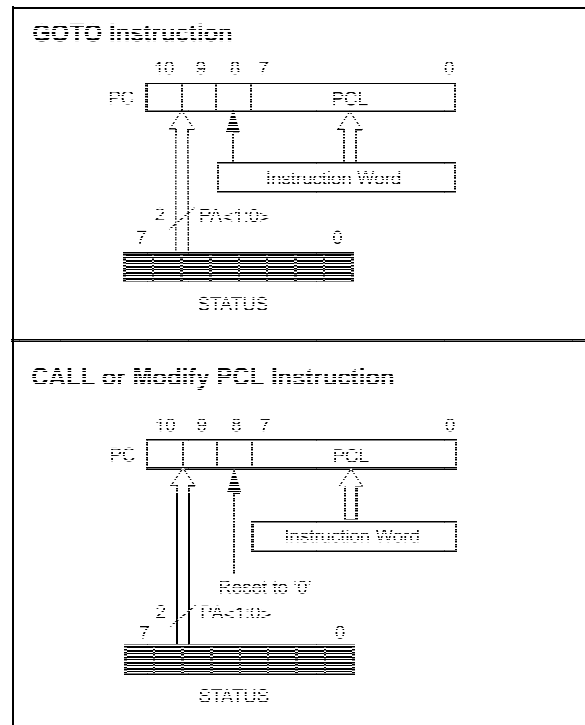
FIGURE 6-7:   LOADING OF PC BRANCH INSTRUCTIONS - PIC16C54, PIC16CR54, PIC16C55
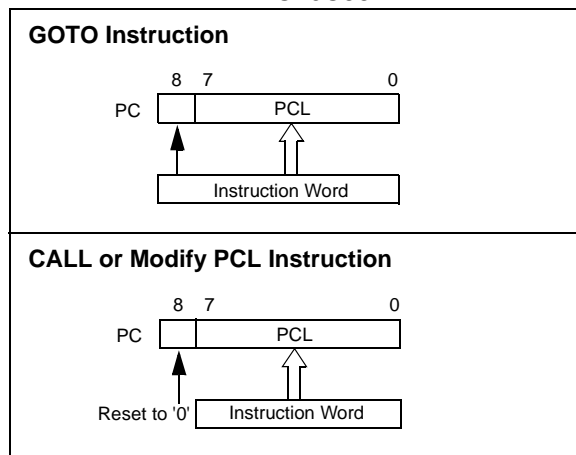
FIGURE 6-8:   LOADING OF PC BRANCH INSTRUCTIONS - PIC16C56/PIC16CR56

FIGURE 6-9:   LOADING OF PC BRANCH INSTRUCTIONS - PIC16C57/PIC16CR57, AND PIC16C58/ PIC16CR58

NOTES:

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7.6   I/O Programming Considerations

7.6.1   BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The `BCF` and `BSF` instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a `BSF` operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 7-1 shows the effect of two sequential read-modify-write instructions (e.g., `BCF`, `BSF`, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 7-1:   READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                  PORT latch  PORT pins
;                  ----------  ----------
  BCF   PORTB, 7  ;01pp pppp   11pp pppp
  BCF   PORTB, 6  ;10pp pppp   11pp pppp
  MOVLW H'3F'      ;
  TRIS  PORTB     ;10pp pppp   10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

7.6.2   SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 7-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a `NOP` or another instruction not accessing this I/O port.

FIGURE 7-2:   SUCCESSIVE I/O OPERATION

This example shows a write to PORTB followed by a read from PORTB.

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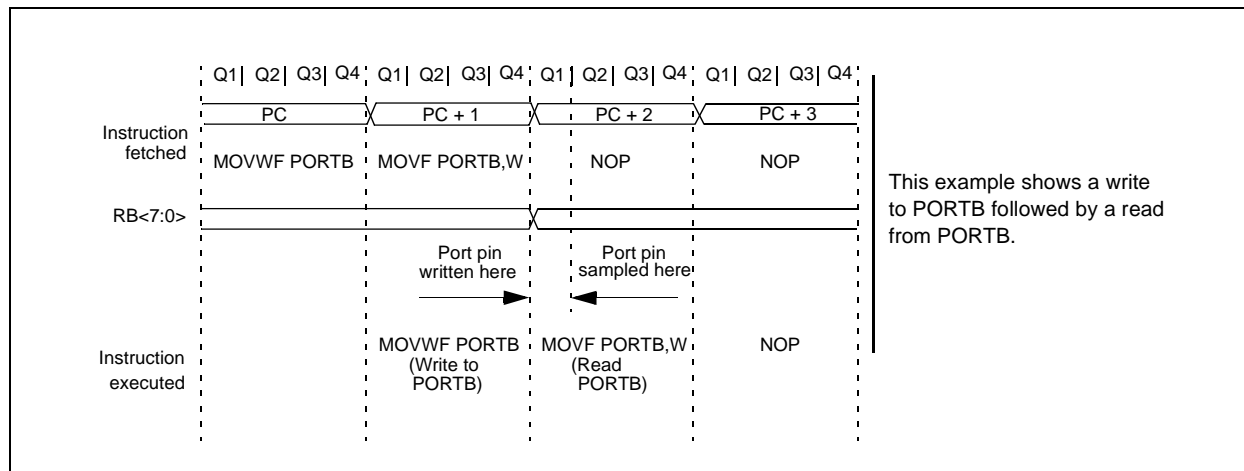
9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC16C5X family of microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator Selection (Section 4.0)
- RESET (Section 5.0)
- Power-On Reset (Section 5.1)
- Device Reset Timer (Section 5.2)
- Watchdog Timer (WDT) (Section 9.2)
- SLEEP (Section 9.3)
- Code protection (Section 9.4)
- ID locations (Section 9.5)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in RESET until the crystal oscillator is stable. With this timer on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake up from SLEEP through external RESET or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

PIC16C5X

TABLE 10-2: INSTRUCTION SET SUMMARY

Mnemonic, Operands		Description	Cycles	12-Bit Opcode MSb	LSb	Status Affected	Notes
ADDWF	f,d	Add W and f	1	0001 11df	ffff	C,DC,Z	1,2,4
ANDWF	f,d	AND W with f	1	0001 01df	ffff	Z	2,4
CLRF	f	Clear f	1	0000 011f	ffff	Z	4
CLRW	–	Clear W	1	0000 0100	0000	Z	
COMF	f, d	Complement f	1	0010 01df	ffff	Z	
DECF	f, d	Decrement f	1	0000 11df	ffff	Z	2,4
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	0010 11df	ffff	None	2,4
INCF	f, d	Increment f	1	0010 10df	ffff	Z	2,4
INCFSZ	f, d	Increment f, Skip if 0	1(2)	0011 11df	ffff	None	2,4
IORWF	f, d	Inclusive OR W with f	1	0001 00df	ffff	Z	2,4
MOVF	f, d	Move f	1	0010 00df	ffff	Z	2,4
MOVWF	f	Move W to f	1	0000 001f	ffff	None	1,4
NOP	–	No Operation	1	0000 0000	0000	None	
RLF	f, d	Rotate left f through Carry	1	0011 01df	ffff	C	2,4
RRF	f, d	Rotate right f through Carry	1	0011 00df	ffff	C	2,4
SUBWF	f, d	Subtract W from f	1	0000 10df	ffff	C,DC,Z	1,2,4
SWAPF	f, d	Swap f	1	0011 10df	ffff	None	2,4
XORWF	f, d	Exclusive OR W with f	1	0001 10df	ffff	Z	2,4
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF	f, b	Bit Clear f	1	0100 bbbf	ffff	None	2,4
BSF	f, b	Bit Set f	1	0101 bbbf	ffff	None	2,4
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	0110 bbbf	ffff	None	
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	0111 bbbf	ffff	None	
LITERAL AND CONTROL OPERATIONS							
ANDLW	k	AND literal with W	1	1110 kkkk	kkkk	Z	
CALL	k	Call subroutine	2	1001 kkkk	kkkk	None	1
CLRWDT	k	Clear Watchdog Timer	1	0000 0000	0100	$\overline{TO}, \overline{PD}$	
GOTO	k	Unconditional branch	2	101k kkkk	kkkk	None	
IORLW	k	Inclusive OR Literal with W	1	1101 kkkk	kkkk	Z	
MOVLW	k	Move Literal to W	1	1100 kkkk	kkkk	None	
OPTION	k	Load OPTION register	1	0000 0000	0010	None	
RETLW	k	Return, place Literal in W	2	1000 kkkk	kkkk	None	
SLEEP	–	Go into standby mode	1	0000 0000	0011	$\overline{TO}, \overline{PD}$	
TRIS	f	Load TRIS register	1	0000 0000	0fff	None	3
XORLW	k	Exclusive OR Literal to W	1	1111 kkkk	kkkk	Z	

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO (see Section 6.5 for more on program counter).

2: When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

3: The instruction TRIS f, where f = 5, 6 or 7 causes the contents of the W register to be written to the tristate latches of PORTA, B or C respectively. A '1' forces the pin to a hi-impedance state and disables the output buffers.

4: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

SUBWF	Subtract W from f
Syntax:	[*label*] SUBWF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	$(f) - (W) \rightarrow (dest)$
Status Affected:	C, DC, Z
Encoding:	`0000` `10df` `ffff`
Description:	Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1

Example 1:   SUBWF   REG1, 1

    Before Instruction
      REG1   =   3
      W   =   2
      C   =   ?
    After Instruction
      REG1   =   1
      W   =   2
      C   =   1   ; result is positive

Example 2:

    Before Instruction
      REG1   =   2
      W   =   2
      C   =   ?
    After Instruction
      REG1   =   0
      W   =   2
      C   =   1   ; result is zero

Example 3:

    Before Instruction
      REG1   =   1
      W   =   2
      C   =   ?
    After Instruction
      REG1   =   0xFF
      W   =   2
      C   =   0   ; result is negative

SWAPF	Swap Nibbles in f
Syntax:	[*label*] SWAPF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	$(f<3:0>) \rightarrow (dest<7:4>);$ $(f<7:4>) \rightarrow (dest<3:0>)$
Status Affected:	None
Encoding:	`0011` `10df` `ffff`
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.
Words:	1
Cycles:	1

Example   SWAPF REG1, 0

    Before Instruction
      REG1   =   0xA5
    After Instruction
      REG1   =   0xA5
      W   =   0x5A

TRIS	Load TRIS Register
Syntax:	[*label*] TRIS f
Operands:	f = 5, 6 or 7
Operation:	$(W) \rightarrow$ TRIS register f
Status Affected:	None
Encoding:	`0000` `0000` `0fff`
Description:	TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register.
Words:	1
Cycles:	1

Example   TRIS   PORTB

    Before Instruction
      W   =   0xA5
    After Instruction
      TRISB   =   0xA5

PIC16C5X

13.2   DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

PIC16CR54A-04E, 10E, 20E (Extended)							Standard Operating Conditions (unless otherwise specified) Operating Temperature −40°C ≤ TA ≤ +125°C for extended
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	**Supply Voltage** RC, XT and LP modes HS mode	3.25 4.5	— —	6.0 5.5	V V	
D002	VDR	**RAM Data Retention Voltage**[1]	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	**Supply Current**[2] RC[3] and XT modes HS mode HS mode	— — —	1.8 4.8 9.0	3.3 10 20	mA mA mA	FOSC = 4.0 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 16 MHz, VDD = 5.5V
D020	IPD	**Power-down Current**[2]	— —	5.0 0.8	22 18	μA μA	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled

*   These parameters are characterized but not tested.

†   Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

    2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

        a)   The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

        b)   For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

    3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

14.0   DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

 "Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean – 3σ) respectively, where σ is a standard deviation, over the whole temperature range.

FIGURE 14-1:   TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE
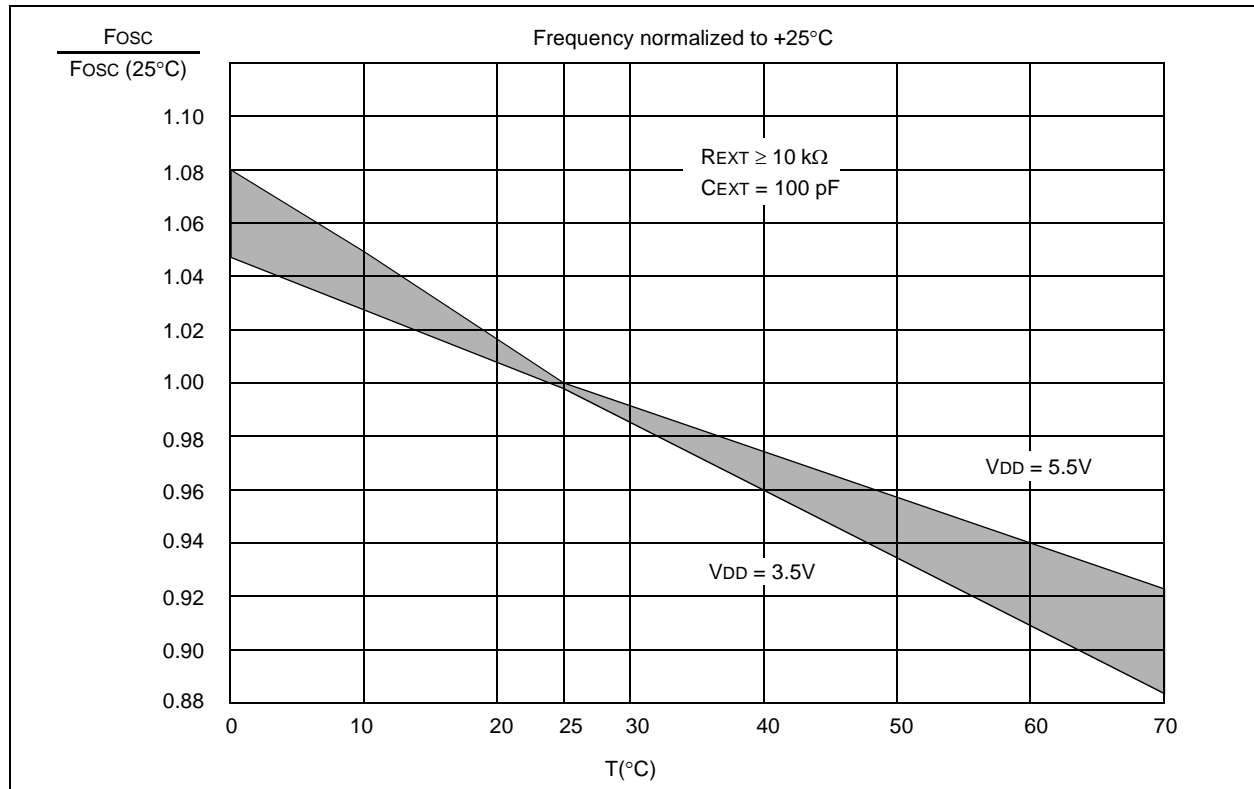
TABLE 14-1:   RC OSCILLATOR FREQUENCIES

C_{EXT}	R_{EXT}	Average F_{OSC} @ 5 V, 25°C	
20 pF	3.3K	5 MHz	$\pm$ 27%
	5K	3.8 MHz	$\pm$ 21%
	10K	2.2 MHz	$\pm$ 21%
	100K	262 kHz	$\pm$ 31%
100 pF	3.3K	1.6 MHz	$\pm$ 13%
	5K	1.2 MHz	$\pm$ 13%
	10K	684 kHz	$\pm$ 18%
	100K	71 kHz	$\pm$ 25%
300 pF	3.3K	660 kHz	$\pm$ 10%
	5.0K	484 kHz	$\pm$ 14%
	10K	267 kHz	$\pm$ 15%
	100K	29 kHz	$\pm$ 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is $\pm$3 standard deviations from the average value for V_{DD} = 5V.

PIC16C5X

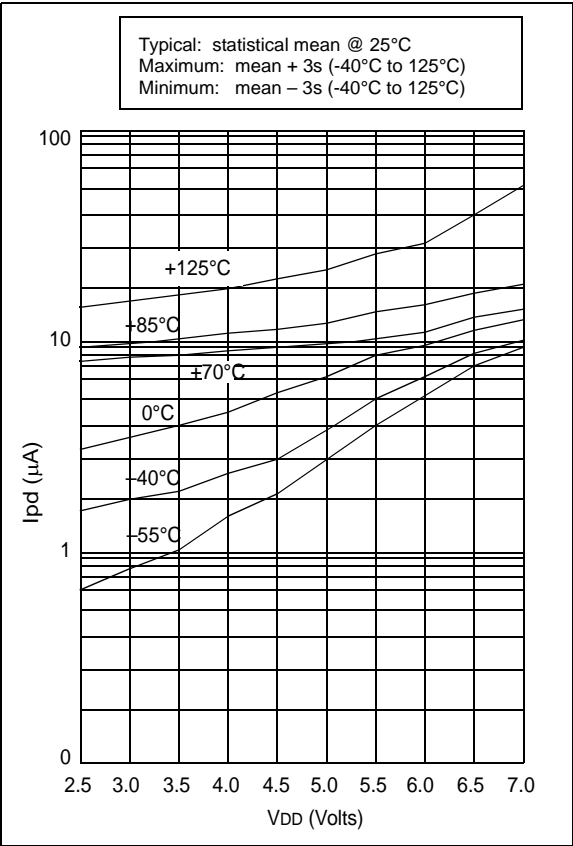**FIGURE 14-6:** **MAXIMUM IPD vs. VDD, WATCHDOG DISABLED**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

FIGURE 14-8: **MAXIMUM IPD vs. VDD, WATCHDOG ENABLED**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

IPD, with WDT enabled, has two components:
The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At –40°C, the latter dominates explaining the apparently anomalous behavior.

FIGURE 14-7: **TYPICAL IPD vs. VDD, WATCHDOG ENABLED**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

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15.4   DC Characteristics: PIC16C54A-04, 10, 20, PIC16LC54A-04, PIC16LV54A-02 (Commercial)
　　　　　　　　　　　　　　　　　PIC16C54A-04I, 10I, 20I, PIC16LC54A-04I, PIC16LV54A-02I (Industrial)
　　　　　　　　　　　　　　　　　PIC16C54A-04E, 10E, 20E, PIC16LC54A-04E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature　　$0°C \leq T_A \leq +70°C$ for commercial 　　　　　　　　　　　　$-40°C \leq T_A \leq +85°C$ for industrial 　　　　　　　　　　　　$-20°C \leq T_A \leq +85°C$ for industrial-PIC16LV54A-02I 　　　　　　　　　　　　$-40°C \leq T_A \leq +125°C$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	VIL	**Input Low Voltage** I/O ports $\overline{MCLR}$ (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	 Vss Vss Vss Vss Vss	 — — — — —	 0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	 V V V V	 Pin at hi-impedance RC mode only[3] XT, HS and LP modes
D040	VIH	**Input High Voltage** I/O ports I/O ports $\overline{MCLR}$ (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	 0.2 VDD + 1 2.0 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD	 — — — — — —	 VDD VDD VDD VDD VDD VDD	 V V V V V V	 For all VDD[4] $4.0V < V_{DD} \leq 5.5V$[4] RC mode only[3] XT, HS and LP modes
D050	VHYS	**Hysteresis of Schmitt Trigger inputs**	0.15 VDD*	—	—	V	
D060	IIL	**Input Leakage Current[1,2]** I/O ports $\overline{MCLR}$ $\overline{MCLR}$ T0CKI OSC1	 -1.0 -5.0 — -3.0 -3.0	 0.5 — 0.5 0.5 0.5	 +1.0 +5.0 +3.0 +3.0 —	 µA µA µA µA µA	**For VDD $\leq$ 5.5V:** VSS $\leq$ VPIN $\leq$ VDD, pin at hi-impedance VPIN = VSS +0.25V VPIN = VDD VSS $\leq$ VPIN $\leq$ VDD VSS $\leq$ VPIN $\leq$ VDD, XT, HS and LP modes
D080	VOL	**Output Low Voltage** I/O ports OSC2/CLKOUT	 — —	 — —	 0.6 0.6	 V V	 IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, RC mode only
	VOH	**Output High Voltage[2]** I/O ports OSC2/CLKOUT	 VDD - 0.7 VDD - 0.7	 — —	 — —	 V V	 IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, RC mode only

*　These parameters are characterized but not tested.

†　Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
　　　2: Negative current is defined as coming out of the pin.
　　　3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

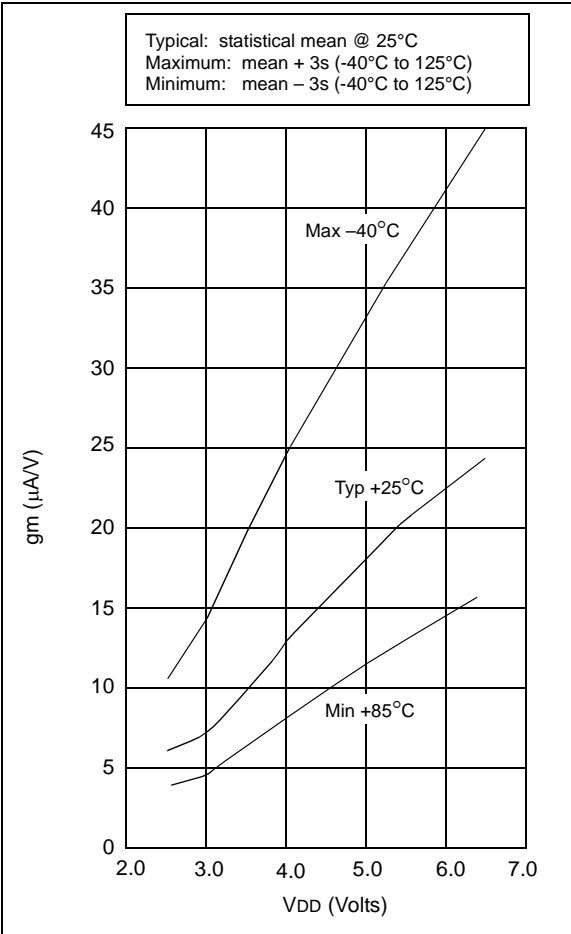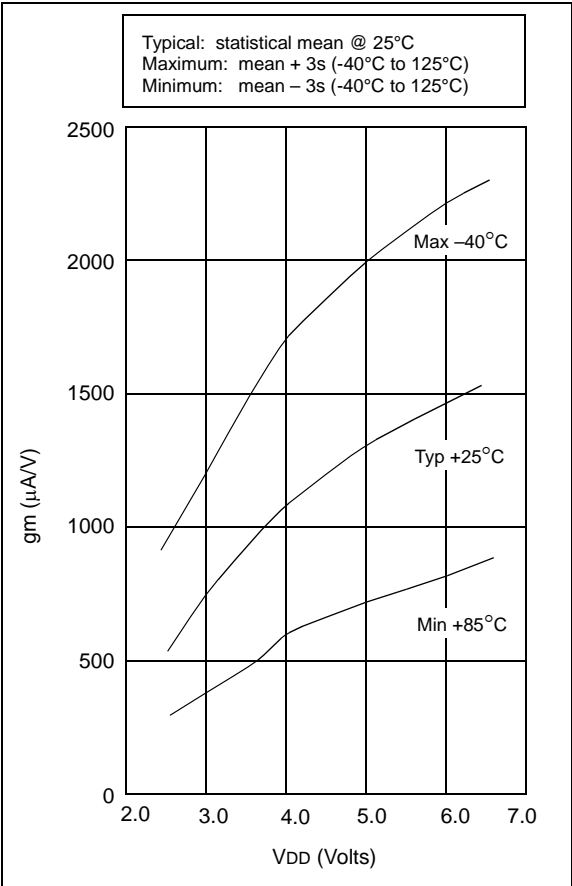**FIGURE 16-18:** **TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD**

FIGURE 16-19: **TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

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17.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial)
PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial)
PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial)
PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial)						**Standard Operating Conditions** (unless otherwise specified) Operating Temperature $\quad$ 0°C $\leq$ TA $\leq$ +70°C for commercial $\quad$ −40°C $\leq$ TA $\leq$ +85°C for industrial	
PIC16C5X PIC16CR5X (Commercial, Industrial)						**Standard Operating Conditions** (unless otherwise specified) Operating Temperature $\quad$ 0°C $\leq$ TA $\leq$ +70°C for commercial $\quad$ −40°C $\leq$ TA $\leq$ +85°C for industrial	
Param No.	**Symbol**	**Characteristic/Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	IPD	**Power-down Current**[2]					
D020		PIC16LC5X	—	0.25	2	μA	VDD = 2.5V, WDT disabled, Commercial
			—	0.25	3	μA	VDD = 2.5V, WDT disabled, Industrial
			—	1	5	μA	VDD = 2.5V, WDT enabled, Commercial
			—	1.25	8	μA	VDD = 2.5V, WDT enabled, Industrial
D020A		PIC16C5X	—	0.25	4.0	μA	VDD = 3.0V, WDT disabled, Commercial
			—	0.25	5.0	μA	VDD = 3.0V, WDT disabled, Industrial
			—	1.8	7.0*	μA	VDD = 5.5V, WDT disabled, Commercial
			—	2.0	8.0*	μA	VDD = 5.5V, WDT disabled, Industrial
			—	4	12*	μA	VDD = 3.0V, WDT enabled, Commercial
			—	4	14*	μA	VDD = 3.0V, WDT enabled, Industrial
			—	9.8	27*	μA	VDD = 5.5V, WDT enabled, Commercial
			—	12	30*	μA	VDD = 5.5V, WDT enabled, Industrial

Legend: Rows with standard voltage device data only are shaded for improved readability.
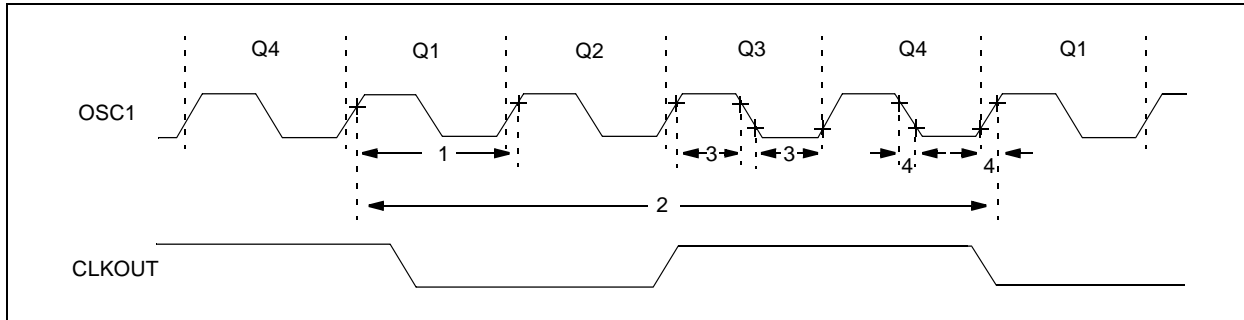
* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula:
IR = VDD/2REXT (mA) with REXT in kΩ.

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17.5 Timing Diagrams and Specifications

FIGURE 17-6: **EXTERNAL CLOCK TIMING - PIC16C5X, PIC16CR5X**

TABLE 17-1: **EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X**

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial −40°C ≤ TA ≤ +85°C for industrial −40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency[1]	DC	—	4.0	MHz	XT OSC mode
			DC	—	4.0	MHz	HS OSC mode (04)
			DC	—	20	MHz	HS OSC mode (20)
			DC	—	200	kHz	LP OSC mode
		Oscillator Frequency[1]	DC	—	4.0	MHz	RC OSC mode
			0.45	—	4.0	MHz	XT OSC mode
			4.0	—	4.0	MHz	HS OSC mode (04)
			4.0	—	20	MHz	HS OSC mode (20)
			5.0	—	200	kHz	LP OSC mode
1	TOSC	External CLKIN Period[1]	250	—	—	ns	XT OSC mode
			250	—	—	ns	HS OSC mode (04)
			50	—	—	ns	HS OSC mode (20)
			5.0	—	—	μs	LP OSC mode
		Oscillator Period[1]	250	—	—	ns	RC OSC mode
			250	—	2,200	ns	XT OSC mode
			250	—	250	ns	HS OSC mode (04)
			50	—	250	ns	HS OSC mode (20)
			5.0	—	200	μs	LP OSC mode

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial −40°C ≤ TA ≤ +85°C for industrial −40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
2	Tcy	Instruction Cycle Time[2]	—	4/F$_{OSC}$	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

*   These parameters are characterized but not tested.

†   Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

  2: Instruction cycle period (T$_{CY}$) equals four times the input oscillator time base period.

FIGURE 19-4: CLKOUT AND I/O TIMING - PIC16C5X-40

Note: Refer to Figure 19-2 for load conditions.
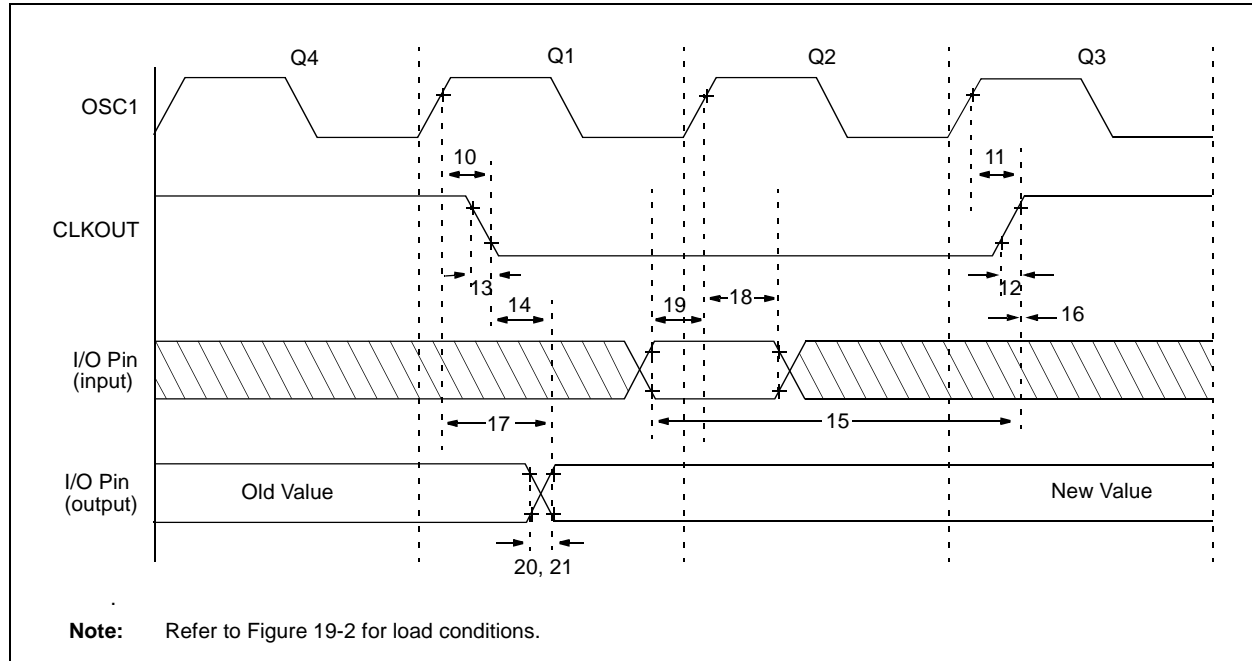
TABLE 19-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X-40

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \leq T_A \leq +70°C$ for commercial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓[1,2]	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑[1,2]	—	15	30**	ns
12	TckR	CLKOUT rise time[1,2]	—	5.0	15**	ns
13	TckF	CLKOUT fall time[1,2]	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid[1,2]	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑[1,2]	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑[1,2]	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid[2]	—	—	100	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time[2]	—	10	25**	ns
21	TioF	Port output fall time[2]	—	10	25**	ns

*   These parameters are characterized but not tested.

**   These parameters are design targets and are not tested. No characterization data available at this time.

†   Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1:   Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.
    2:   Refer to Figure 19-2 for load conditions.

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FIGURE 19-5: **RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X-40**

Note 1: Please refer to Figure 19-2 for load conditions.
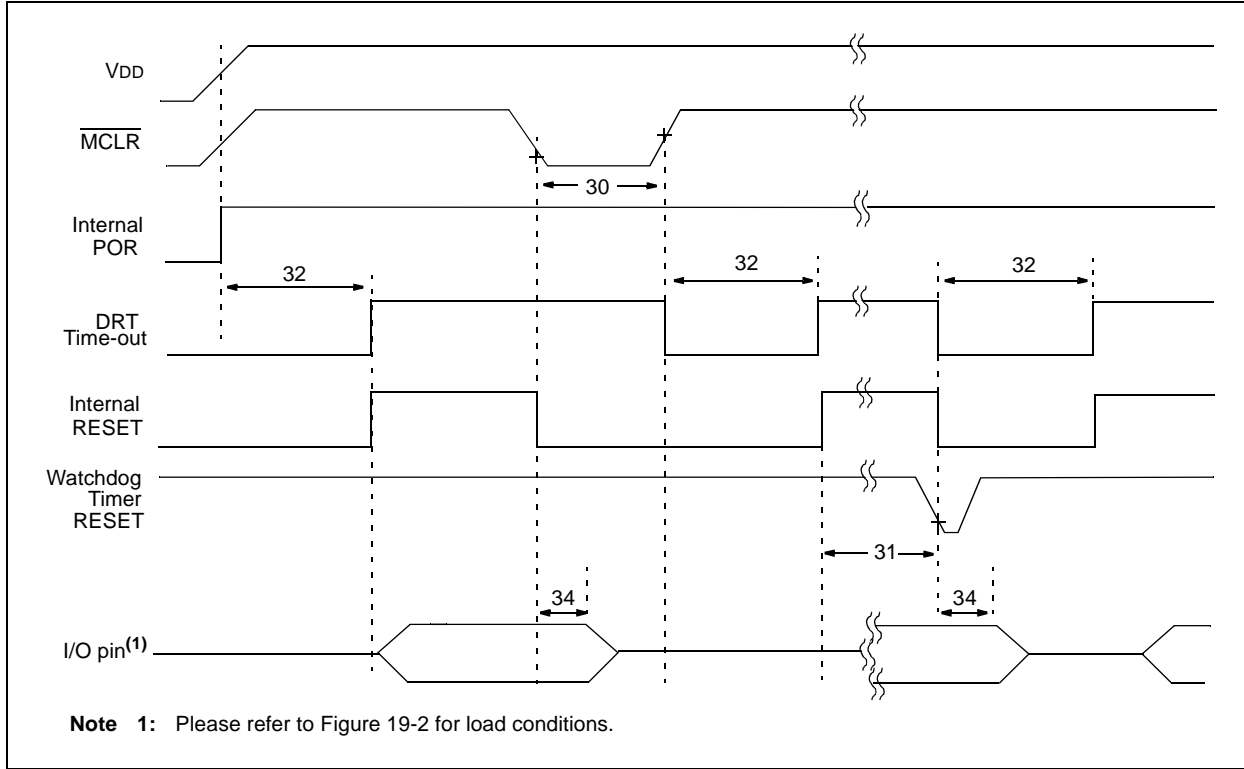
TABLE 19-3: **RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X-40**

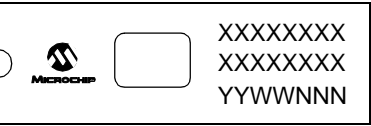| AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \leq T_A \leq +70°C$ (commercial) Operating Voltage V_{DD} range is described in Section 19.1.						
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	1000*	—	—	ns	V_{DD} = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	V_{DD} = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	V_{DD} = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from $\overline{MCLR}$ Low	100*	300*	1000*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
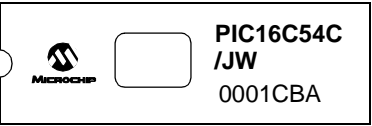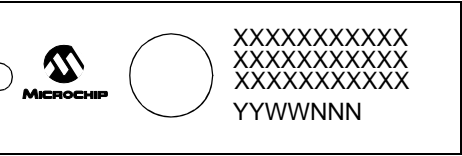
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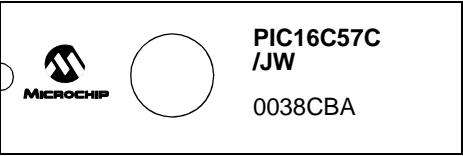## Package Marking Information (Cont'd)

18-Lead CERDIP Windowed

```
XXXXXXX
XXXXXXX
YYWWNNN
```

Example

```
PIC16C54C
/JW
0001CBA
```

28-Lead CERDIP Windowed

```
XXXXXXXXXX
XXXXXXXXXX
XXXXXXXXXX
YYWWNNN
```

Example

```
PIC16C57C
/JW
0038CBA
```

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

1. Check any `CALL`, `GOTO` or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.

2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.

3. Eliminate any special function register page switching. Redefine data variables to reallocate them.

4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.

5. Change RESET vector to proper value for processor used.

6. Remove any use of the `ADDLW`, `RETURN` and `SUBLW` instructions.

7. Rewrite any code segments that use interrupts.

APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.

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