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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

2 0 0 0 0	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c56at-04-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A twostage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle except for program branches.

The PIC16C54/CR54 and PIC16C55 address 512 x 12 of program memory, the PIC16C56/CR56 address 1K x 12 of program memory, and the PIC16C57/CR57 and PIC16C58/CR58 address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly. The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 (for PIC16C54/56/58) and Table 3-2 (for PIC16C55/57).

NOTES:

# 7.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., MOVF PORTB, W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

## 7.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used (RA<3:0>). Bits 7-4 are unimplemented and read as '0's.

# 7.2 PORTB

PORTB is an 8-bit I/O Register (PORTB<7:0>).

# 7.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16CR56, PIC16CR56, PIC16CS8 and PIC16CR58.

# 7.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the TRIS f instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

Note:	A read of the ports reads the pins, not the
	output data latches. That is, if an output
	driver on a pin is enabled and driven high,
	but the external system is holding it low, a
	read of the port will indicate that the pin is
	low.

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

TABLE 7-1:	SUMMARY OF PORT REGISTERS

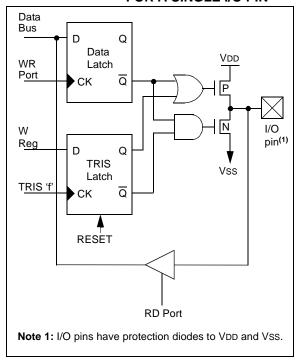
#### Value on Value on Bit 4 Bit 3 Bit 1 Bit 0 MCLR and Address Name Bit 7 Bit 6 Bit 5 Bit 2 Power-On Reset WDT Reset TRIS N/A I/O Control Registers (TRISA, TRISB, TRISC) 1111 1111 1111 1111 05h PORTA RA3 RA2 RA1 RA0 \_ \_ \_ \_ xxxx \_ \_ \_ \_ uuuu PORTB 06h RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0 XXXX XXXX uuuu uuuu 07h PORTC RC7 RC6 RC5 RC4 RC3 RC2 RC1 RC0 XXXX XXXX uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'

## 7.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 7-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

#### FIGURE 7-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



#### CONFIGURATION WORD FOR PIC16C54/C55/C56/C57 **REGISTER 9-2:**

			İ				İ	СР	WDTE	FOSC1	FOSC0
		_	_	_				CP	WDIE	FUSCI	
bit 11											bit 0
bit 11-4:	Unimple	mented	Read as '	0'							
bit 3:	CP: Cod	e protecti	on bit.								
		e protecti									
	0 = Code	e protectio	on on								
bit 2:	WDTE: \	Vatchdog	timer ena	ble bit							
	1 = WDT	enabled									
	0 = WDT	disabled									
bit 1-0:	FOSC1:I	FOSC0: (	Oscillator s	election b	oits <sup>(2)</sup>						
	00 = LF	oscillato	or								
	01 = X	T oscillato	or								
		S oscillato									
	11 = R	C oscillate	or								
Note 1.	Refer to t	ha PIC16	C5X Prog	rammina	Specificat	ions (Liter	atura Num	her DS3	190) to d	otormino l	now to
			iration wor	0	opeemear				, 100) to u		1011 10
2:		•	orts XT, R		oscillator	onlv.					
						- 1					
Legend:											

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

NOTES:

# 11.0 DEVELOPMENT SUPPORT

The PIC<sup>®</sup> microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB<sup>®</sup> IDE Software
- Assemblers/Compilers/Linkers
  - MPASM<sup>™</sup> Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/
  - MPLIB<sup>™</sup> Object Librarian
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - ICEPIC<sup>™</sup> In-Circuit Emulator
- In-Circuit Debugger
- MPLAB ICD
- Device Programmers
  - PRO MATE<sup>®</sup> II Universal Device Programmer
- PICSTART<sup>®</sup> Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
  - PICDEM<sup>™</sup>1 Demonstration Board
  - PICDEM 2 Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - KEELOQ<sup>®</sup> Demonstration Board

## 11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows<sup>®</sup>-based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

# 11.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel<sup>®</sup> standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

## 11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

#### 13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LC	PIC16LCR54A-04 PIC16LCR54A-04I (Commercial, Industrial)				$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$							
PIC16CR54A-04, 10, 20 PIC16CR54A-04I, 10I, 20I (Commercial, Industrial)			$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$									
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions					
	IPD	Power-down Current <sup>(2)</sup>										
D006		PIC16LCR54A-Commercial		1.0 2.0 3.0 5.0	6.0 8.0* 15 25	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled					
D006A		PIC16CR54A-Commercial		1.0 2.0 3.0 5.0	6.0 8.0* 15 25	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled					
D007		PIC16LCR54A-Industrial		1.0 2.0 3.0 3.0 5.0	8.0 10* 20* 18 45	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 4.0V, WDT enabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled					
D007A		PIC16CR54A-Industrial		1.0 2.0 3.0 3.0 5.0	8.0 10* 20* 18 45	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 4.0V, WDT enabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled					

Legend: Rows with standard voltage device data only are shaded for improved readability.

- \* These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.
- **Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
  - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
    - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
    - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
  - 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k $\Omega$ .

# PIC16C5X

# **FIGURE 14-2: TYPICAL RC OSC** FREQUENCY vs. VDD, CEXT = 20 PF Typical: statistical mean @ 25°C Maximum: mean + 3s (-40°C to 125°C) Minimum: mean – 3s (-40°C to 125°C) 5.5 R = 3.3K5.0 4.5 R = 5K 4.0 3.5 Fosc (MHz) 3.0 R = 10K 2.5 2.0 Measured on DIP Packages, $T = 25^{\circ}C$ 1.5 1.0 R = 100K 0.5 0.0 3.0 3.5 4.0 4.5 5.0 5.5 6.0 VDD (Volts)

#### FIGURE 14-3:

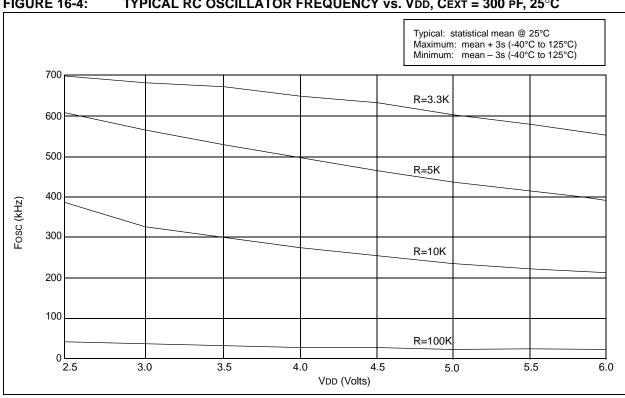
#### TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 100 PF





#### FIGURE 14-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED

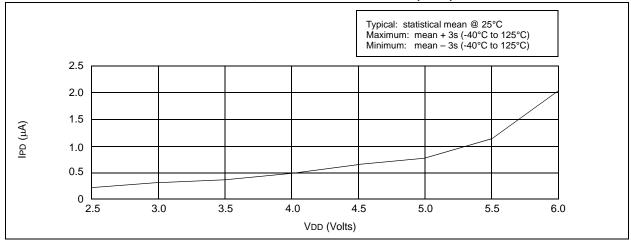




#### **FIGURE 16-4:** TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 PF, 25°C

# PIC16C5X

## FIGURE 16-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)







## 17.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrialStandard Operating Conditions (unless otherwise specified)							
PIC16C5X PIC16CR5X (Commercial, Industrial)				Standard Operating Conditions (unless otherwise specifOperating Temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ for comme $-40^{\circ}C \leq TA \leq +85^{\circ}C$ for industriation						
Param No.	Symbol	Characteristic/Device	Min Typ† Max Units			Units	Conditions			
	Vdd	Supply Voltage								
D001		PIC16LC5X	2.5 2.7 2.5		5.5 5.5 5.5	V V V	$\begin{array}{l} -40^{\circ}C \leq TA \leq +\ 85^{\circ}C,\ 16LCR5X \\ -40^{\circ}C \leq TA \leq 0^{\circ}C,\ 16LC5X \\ 0^{\circ}C \leq TA \leq +\ 85^{\circ}C\ 16LC5X \end{array}$			
D001A		PIC16C5X	3.0 4.5	_	5.5 5.5	V V	RC, XT, LP and HS mode from 0 - 10 MHz from 10 - 20 MHz			
D002	Vdr	RAM Data Retention Volt- age <sup>(1)</sup>	—	1.5*	—	V	Device in SLEEP mode			
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset			
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset			

Legend: Rows with standard voltage device data only are shaded for improved readability.

\* These parameters are characterized but not tested.

- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
  - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
    - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
    - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
  - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k $\Omega$ .

#### 17.3 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial, Extended) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial, Extended) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

DC CHARACTERISTICS		Standard Operat Operating Tempe	$\begin{array}{l} \mbox{nditions (unless otherwise specified)} \\ 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for extended} \end{array}$				
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
D030	VIL	Input Low Voltage I/O Ports I/O Ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss Vss Vss	  	0.8 V 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V V	4.5V <v<sub>DD ≤ 5.5V Otherwise RC mode only<sup>(3)</sup> XT, HS and LP modes</v<sub>
D040	Viн	Input High Voltage I/O ports I/O ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	2.0 0.25 Vdd+0.8 0.85 Vdd 0.85 Vdd 0.85 Vdd 0.85 Vdd 0.7 Vdd	 	Vdd Vdd Vdd Vdd Vdd Vdd Vdd	V V V V V	4.5V < VDD ≤ 5.5V Otherwise RC mode only <sup>(3)</sup> XT, HS and LP modes
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	—	_	V	
D060	Ιι∟	Input Leakage Current <sup>(1,2)</sup> I/O ports MCLR MCLR T0CKI OSC1	-1.0 -5.0 -3.0 -3.0	0.5 — 0.5 0.5 0.5	+1.0 +5.0 +3.0 +3.0 —	μΑ μΑ μΑ μΑ μΑ	For VDD $\leq$ 5.5V: VSS $\leq$ VPIN $\leq$ VDD, pin at hi-impedance VPIN = VSS +0.25V VPIN = VDD VSS $\leq$ VPIN $\leq$ VDD VSS $\leq$ VPIN $\leq$ VDD, XT, HS and LP modes
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.6 0.6	V V	IOL = 8.7  mA, VDD = 4.5V IOL = 1.6  mA, VDD = 4.5V, RC mode only
D090	Vон	Output High Voltage <sup>(2)</sup> I/O ports OSC2/CLKOUT	Vdd - 0.7 Vdd - 0.7	_	_	V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, RC mode only

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
  - **2:** Negative current is defined as coming out of the pin.
  - 3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.



#### FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 PF, 25°C





# 19.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)<sup>(1)</sup>

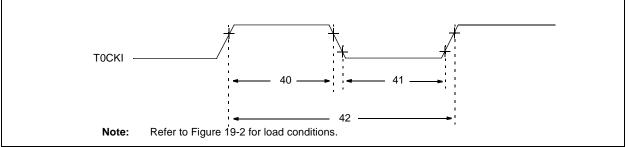
				ard Ope ing Tem	-		tions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial		
Param No.	Symbol	Characteristic		Characteristic		Min Typ† Max		Units	Conditions
D001	Vdd	Supply Voltage	4.5	-	5.5	V	HS mode from 20 - 40 MHz		
D002	Vdr	RAM Data Retention Voltage <sup>(2)</sup>		1.5*	—	V	Device in SLEEP mode		
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	SVDD	VDD Rise Rate to ensure Power- on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset		
D010	Idd	Supply Current <sup>(3)</sup>	_	5.2 6.8	12.3 16	mA mA	Fosc = 40 MHz, $VDD$ = 4.5V, HS mode Fosc = 40 MHz, $VDD$ = 5.5V, HS mode		
D020	IPD	Power-down Current <sup>(3)</sup>	_	1.8 9.8	7.0 27*	μΑ μΑ	VDD = 5.5V, WDT disabled, Commercial VDD = 5.5V, WDT enabled, Commercial		

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- **Note 1:** Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected, HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 19.1.
  - **2:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
  - **3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
    - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
    - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

# FIGURE 19-6: TIMER0 CLOCK TIMINGS - PIC16C5X-40



#### TABLE 19-4: TIMER0 CLOCK REQUIREMENTS PIC16C5X-40

A	AC Charac	toristics	Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial							
Param No.	Symbol	Characteristic	Characteristic Min			Units	Conditions			
40	Tt0H	T0CKI High Pulse Width								
		- No Prescaler	0.5 Tcy + 20*	—		ns				
		- With Prescaler	10*		—	ns				
41	Tt0L	T0CKI Low Pulse Width								
		- No Prescaler	0.5 TCY + 20*	—		ns				
		- With Prescaler	10*	_	—	ns				
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> * N	_	_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)			

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

# 20.0 DEVICE CHARACTERIZATION - PIC16LC54C 40MHz

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean +  $3\sigma$ ) or (mean -  $3\sigma$ ) respectively, where  $\sigma$  is a standard deviation, over the whole temperature range.

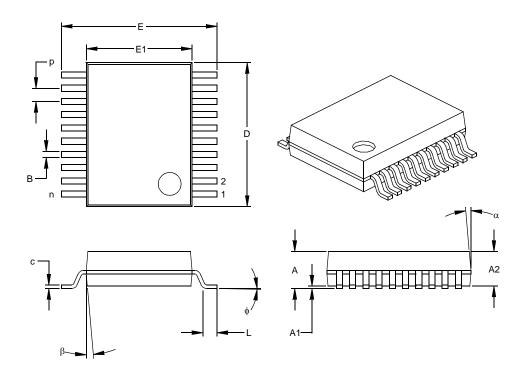




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#### 20-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES*		MILLIMETERS			
Dimensio	on Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		20			20		
Pitch	р		.026			0.65		
Overall Height	Α	.068	.073	.078	1.73	1.85	1.98	
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83	
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25	
Overall Width	Е	.299	.309	.322	7.59	7.85	8.18	
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38	
Overall Length	D	.278	.284	.289	7.06	7.20	7.34	
Foot Length	L	.022	.030	.037	0.56	0.75	0.94	
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25	
Foot Angle	ф	0	4	8	0.00	101.60	203.20	
Lead Width	В	.010	.013	.015	0.25	0.32	0.38	
Mold Draft Angle Top	α	0	5	10	0	5	10	
Mold Draft Angle Bottom	β	0	5	10	0	5	10	

\* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-150 Drawing No. C04-072

# 28-Lead Ceramic Dual In-line with Window (JW) - 600 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units				MILLIMETERS			
Dimensior	Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28		
Pitch	р		.100			2.54		
Top to Seating Plane	Α	.195	.210	.225	4.95	5.33	5.72	
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19	
Standoff	A1	.015	.038	.060	0.38	0.95	1.52	
Shoulder to Shoulder Width	Е	.595	.600	.625	15.11	15.24	15.88	
Ceramic Pkg. Width	E1	.514	.520	.526	13.06	13.21	13.36	
Overall Length	D	1.430	1.460	1.490	36.32	37.08	37.85	
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81	
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30	
Upper Lead Width	B1	.050	.058	.065	1.27	1.46	1.65	
Lower Lead Width	В	.016	.020	.023	0.41	0.51	0.58	
Overall Row Spacing §	eB	.610	.660	.710	15.49	16.76	18.03	
Window Diameter	W	.270	.280	.290	6.86	7.11	7.37	

Sontolling Parameter
 Significant Characteristic
 JEDEC Equivalent: MO-103
 Drawing No. C04-013

# APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

- 1. Check any CALL, GOTO or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
- 2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change RESET vector to proper value for processor used.
- 6. Remove any use of the ADDLW, RETURN and SUBLW instructions.
- 7. Rewrite any code segments that use interrupts.

# APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.