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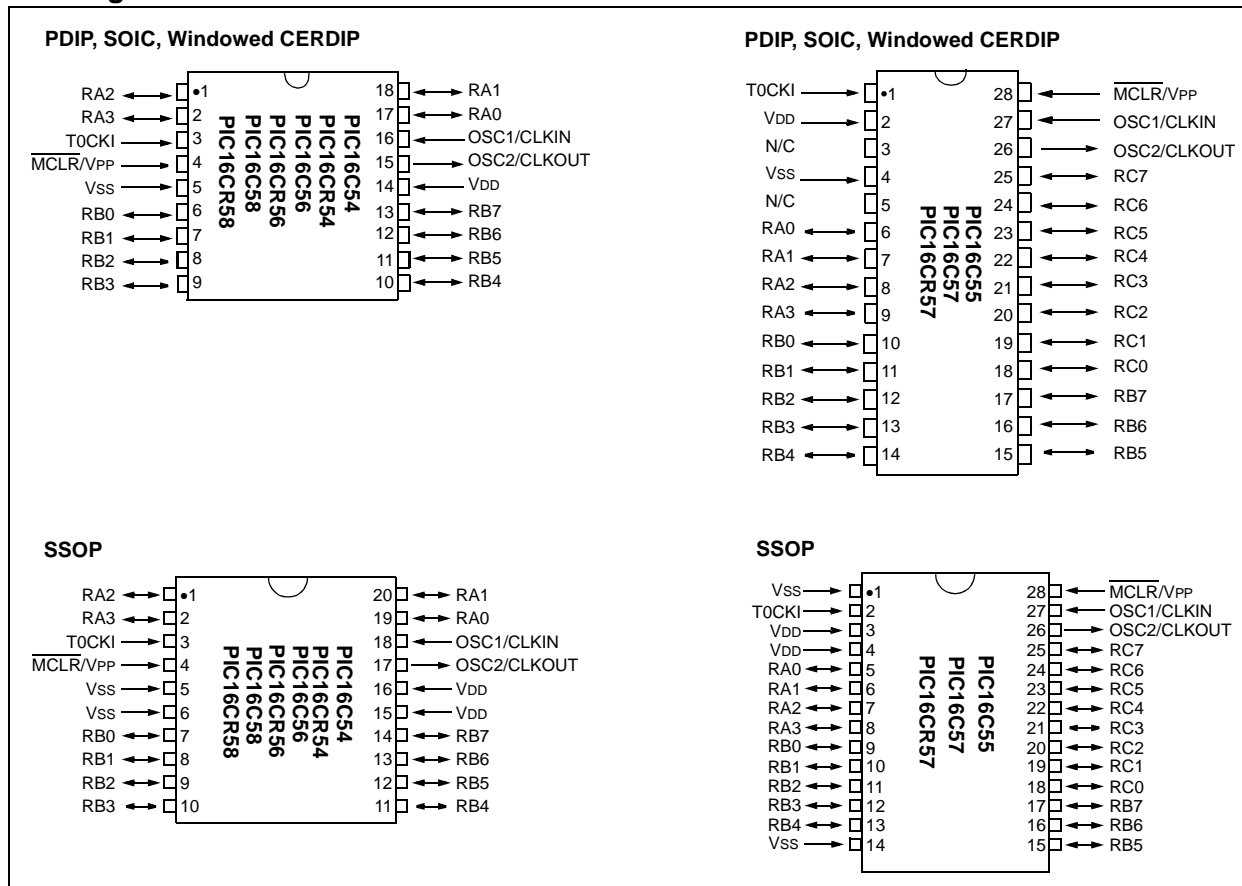
Applications of "**Embedded - Microcontrollers**"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c56t-hsi-so

PIC16C5X

Pin Diagrams

PDIP, SOIC, Windowed CERDIP

PIC16C54 / PIC16CR54 / PIC16C56 / PIC16CR56 / PIC16CR58

```
RA2      →  •1        18  ↔  RA1
RA3      ↔   2        17  ↔  RA0
T0CKI    →   3        16  →  OSC1/CLKIN
MCLR/VPP →   4        15  →  OSC2/CLKOUT
VSS      →   5        14  →  VDD
RB0      ↔   6        13  ↔  RB7
RB1      ↔   7        12  ↔  RB6
RB2      ↔   8        11  ↔  RB5
RB3      ↔   9        10  ↔  RB4
```

PDIP, SOIC, Windowed CERDIP

PIC16C55 / PIC16C57 / PIC16CR57

```
T0CKI    →   •1       28  ←  MCLR/VPP
VDD      →    2       27  ←  OSC1/CLKIN
N/C      →    3       26  →  OSC2/CLKOUT
VSS      →    4       25  ↔  RC7
N/C      →    5       24  ↔  RC6
RA0      ↔    6       23  ↔  RC5
RA1      ↔    7       22  ↔  RC4
RA2      ↔    8       21  ↔  RC3
RA3      ↔    9       20  ↔  RC2
RB0      ↔   10       19  ↔  RC1
RB1      ↔   11       18  ↔  RC0
RB2      ↔   12       17  ↔  RB7
RB3      ↔   13       16  ↔  RB6
RB4      ↔   14       15  ↔  RB5
```

SSOP

PIC16C54 / PIC16CR54 / PIC16C56 / PIC16CR56 / PIC16CR58

```
RA2      ↔   •1       20  ↔  RA1
RA3      ↔    2       19  ↔  RA0
T0CKI    →    3       18  →  OSC1/CLKIN
MCLR/VPP →    4       17  →  OSC2/CLKOUT
VSS      →    5       16  →  VDD
VSS      →    6       15  →  VDD
RB0      ↔    7       14  ↔  RB7
RB1      ↔    8       13  ↔  RB6
RB2      ↔    9       12  ↔  RB5
RB3      ↔   10       11  ↔  RB4
```

SSOP

PIC16C55 / PIC16C57 / PIC16CR57

```
VSS      →   •1       28  ←  MCLR/VPP
T0CKI    →    2       27  →  OSC1/CLKIN
VDD      →    3       26  →  OSC2/CLKOUT
VDD      →    4       25  ↔  RC7
RA0      ↔    5       24  ↔  RC6
RA1      ↔    6       23  ↔  RC5
RA2      ↔    7       22  ↔  RC4
RA3      ↔    8       21  ↔  RC3
RB0      ↔    9       20  ↔  RC2
RB1      ↔   10       19  ↔  RC1
RB2      ↔   11       18  ↔  RC0
RB3      ↔   12       17  ↔  RB7
RB4      ↔   13       16  ↔  RB6
VSS      →   14       15  ↔  RB5
```

Device Differences

Device	Voltage Range	Oscillator Selection (Program)	Oscillator	Process Technology (Microns)	ROM Equivalent	MCLR Filter
PIC16C54	2.5-6.25	Factory	See **Note 1**	1.2	PIC16CR54A	No
PIC16C54A	2.0-6.25	User	See **Note 1**	0.9	—	No
PIC16C54C	2.5-5.5	User	See **Note 1**	0.7	PIC16CR54C	Yes
PIC16C55	2.5-6.25	Factory	See **Note 1**	1.7	—	No
PIC16C55A	2.5-5.5	User	See **Note 1**	0.7	—	Yes
PIC16C56	2.5-6.25	Factory	See **Note 1**	1.7	—	No
PIC16C56A	2.5-5.5	User	See **Note 1**	0.7	PIC16CR56A	Yes
PIC16C57	2.5-6.25	Factory	See **Note 1**	1.2	—	No
PIC16C57C	2.5-5.5	User	See **Note 1**	0.7	PIC16CR57C	Yes
PIC16C58B	2.5-5.5	User	See **Note 1**	0.7	PIC16CR58B	Yes
PIC16CR54A	2.5-6.25	Factory	See **Note 1**	1.2	N/A	Yes
PIC16CR54C	2.5-5.5	Factory	See **Note 1**	0.7	N/A	Yes
PIC16CR56A	2.5-5.5	Factory	See **Note 1**	0.7	N/A	Yes
PIC16CR57C	2.5-5.5	Factory	See **Note 1**	0.7	N/A	Yes
PIC16CR58B	2.5-5.5	Factory	See **Note 1**	0.7	N/A	Yes

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

Note: The table shown above shows the generic names of the PIC16C5X devices. For device varieties, please refer to Section 2.0.

Preliminary

PIC16C5X

TABLE 1-1:   PIC16C5X FAMILY OF DEVICES

Features	PIC16C54	PIC16CR54	PIC16C55	PIC16C56	PIC16CR56
Maximum Operation Frequency	40 MHz	20 MHz	40 MHz	40 MHz	20 MHz
EPROM Program Memory (x12 words)	512	—	512	1K	—
ROM Program Memory (x12 words)	—	512	—	—	1K
RAM Data Memory (bytes)	25	25	24	25	25
Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0
I/O Pins	12	12	20	12	12
Number of Instructions	33	33	33	33	33
Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PIC® Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.

Features	PIC16C57	PIC16CR57	PIC16C58	PIC16CR58
Maximum Operation Frequency	40 MHz	20 MHz	40 MHz	20 MHz
EPROM Program Memory (x12 words)	2K	—	2K	—
ROM Program Memory (x12 words)	—	2K	—	2K
RAM Data Memory (bytes)	72	72	73	73
Timer Module(s)	TMR0	TMR0	TMR0	TMR0
I/O Pins	20	20	12	12
Number of Instructions	33	33	33	33
Packages	28-pin DIP, SOIC; 28-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PIC® Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.

Preliminary

3.0   ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle except for program branches.

The PIC16C54/CR54 and PIC16C55 address 512 x 12 of program memory, the PIC16C56/CR56 address 1K x 12 of program memory, and the PIC16C57/CR57 and PIC16C58/CR58 address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 (for PIC16C54/56/58) and Table 3-2 (for PIC16C55/57).

6.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as 000u u1uu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 10.0, Instruction Set Summary.

REGISTER 6-1: STATUS REGISTER (ADDRESS: 03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
PA2	PA1	PA0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C

bit 7   bit 0

bit 7: **PA2**: This bit unused at this time.

Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

bit 6-5: **PA<1:0>**: Program page preselect bits (PIC16C56/CR56)(PIC16C57/CR57)(PIC16C58/CR58)

00 = Page 0 (000h - 1FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58
01 = Page 1 (200h - 3FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58
10 = Page 2 (400h - 5FFh) - PIC16C57/CR57, PIC16C58/CR58
11 = Page 3 (600h - 7FFh) - PIC16C57/CR57, PIC16C58/CR58
Each page is 512 words.
Using the PA<1:0> bits as general purpose read/write bits in devices which do not use them for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: **$\overline{\text{TO}}$**: Time-out bit

1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3: **$\overline{\text{PD}}$**: Power-down bit

1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2: **Z**: Zero bit

1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/borrow bit (for ADDWF and SUBWF instructions)
ADDWF
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
SUBWF
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/borrow bit (for ADDWF, SUBWF and RRF, RLF instructions)

ADDWF	**SUBWF**	**RRF or RLF**
1 = A carry occurred	1 = A borrow did not occur	Loaded with LSb or MSb, respectively
0 = A carry did not occur	0 = A borrow occurred	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared x = bit is unknown

NOTES:

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NOTES:

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SUBWF	Subtract W from f
Syntax:	[*label*] SUBWF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	$(f) - (W) \rightarrow (dest)$
Status Affected:	C, DC, Z
Encoding:	`0000` `10df` `ffff`
Description:	Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1

Example 1:   SUBWF   REG1, 1

    Before Instruction
      REG1   =   3
      W   =   2
      C   =   ?
    After Instruction
      REG1   =   1
      W   =   2
      C   =   1   ; result is positive

Example 2:

    Before Instruction
      REG1   =   2
      W   =   2
      C   =   ?
    After Instruction
      REG1   =   0
      W   =   2
      C   =   1   ; result is zero

Example 3:

    Before Instruction
      REG1   =   1
      W   =   2
      C   =   ?
    After Instruction
      REG1   =   0xFF
      W   =   2
      C   =   0   ; result is negative

SWAPF	Swap Nibbles in f
Syntax:	[*label*] SWAPF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	$(f<3:0>) \rightarrow (dest<7:4>)$; $(f<7:4>) \rightarrow (dest<3:0>)$
Status Affected:	None
Encoding:	`0011` `10df` `ffff`
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.
Words:	1
Cycles:	1

Example   SWAPF REG1, 0

    Before Instruction
      REG1   =   0xA5
    After Instruction
      REG1   =   0xA5
      W   =   0x5A

TRIS	Load TRIS Register
Syntax:	[*label*] TRIS f
Operands:	f = 5, 6 or 7
Operation:	$(W) \rightarrow$ TRIS register f
Status Affected:	None
Encoding:	`0000` `0000` `0fff`
Description:	TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register.
Words:	1
Cycles:	1

Example   TRIS   PORTB

    Before Instruction
      W   =   0xA5
    After Instruction
      TRISB   =   0xA5

NOTES:

PIC16C5X

FIGURE 12-5: TIMER0 CLOCK TIMINGS - PIC16C54/55/56/57

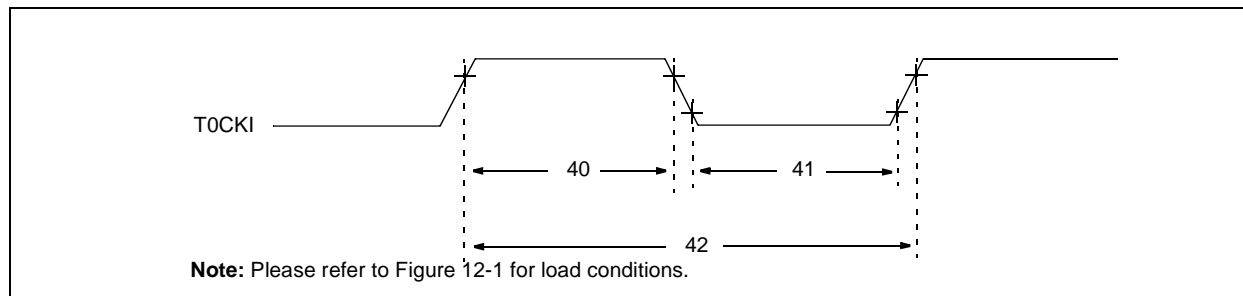**Note:** Please refer to Figure 12-1 for load conditions.

TABLE 12-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \leq T_A \leq +70°C$ for commercial $-40°C \leq T_A \leq +85°C$ for industrial $-40°C \leq T_A \leq +125°C$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width					
		- No Prescaler	$0.5\ T_{CY} + 20$*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width					
		- No Prescaler	$0.5\ T_{CY} + 20$*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

13.3 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial)
PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \leq T_A \leq +70°C$ for commercial $-40°C \leq T_A \leq +85°C$ for industrial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	V_{IL}	**Input Low Voltage** I/O ports $\overline{MCLR}$ (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	 VSS VSS VSS VSS VSS	 — — — — —	 0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD	 V V V V V	 Pin at hi-impedance RC mode only[3] XT, HS and LP modes
D040	V_{IH}	**Input High Voltage** I/O ports I/O ports $\overline{MCLR}$ (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	 2.0 0.6 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD	 — — — — — —	 VDD VDD VDD VDD VDD VDD	 V V V V V V	 VDD = 3.0V to 5.5V[4] Full VDD range[4] RC mode only[3] XT, HS and LP modes
D050	V_{HYS}	**Hysteresis of Schmitt Trigger inputs**	0.15 VDD*	—	—	V	
D060	I_{IL}	**Input Leakage Current**[1,2] I/O ports MCLR MCLR T0CKI OSC1	 −1.0 −5.0 — −3.0 −3.0	 — — 0.5 0.5 0.5	 +1.0 — +5.0 +3.0 +3.0	 μA μA μA μA μA	**For VDD ≤ 5.5V:** VSS ≤ VPIN ≤ VDD, pin at hi-impedance VPIN = VSS + 0.25V VPIN = VDD VSS ≤ VPIN ≤ VDD VSS ≤ VPIN ≤ VDD, XT, HS and LP modes
D080	V_{OL}	**Output Low Voltage** I/O ports OSC2/CLKOUT	 — —	 — —	 0.5 0.5	 V V	 IOL = 10 mA, VDD = 6.0V IOL = 1.9 mA, VDD = 6.0V, RC mode only
D090	V_{OH}	**Output High Voltage**[2] I/O ports OSC2/CLKOUT	 VDD − 0.5 VDD − 0.5	 — —	 — —	 V V	 IOH = −4.0 mA, VDD = 6.0V IOH = −0.8 mA, VDD = 6.0V, RC mode only

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

TABLE 13-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial −40°C ≤ TA ≤ +85°C for industrial −40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
1	TOSC	External CLKIN Period[1]	250	—	—	ns	XT OSC mode
			250	—	—	ns	HS OSC mode (04)
			100	—	—	ns	HS OSC mode (10)
			50	—	—	ns	HS OSC mode (20)
			5.0	—	—	μs	LP OSC mode
		Oscillator Period[1]	250	—	—	ns	RC OSC mode
			250	—	10,000	ns	XT OSC mode
			250	—	250	ns	HS OSC mode (04)
			100	—	250	ns	HS OSC mode (10)
			50	—	250	ns	HS OSC mode (20)
			5.0	—	200	μs	LP OSC mode
2	Tcy	Instruction Cycle Time[2]	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

*   These parameters are characterized but not tested.

†   Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

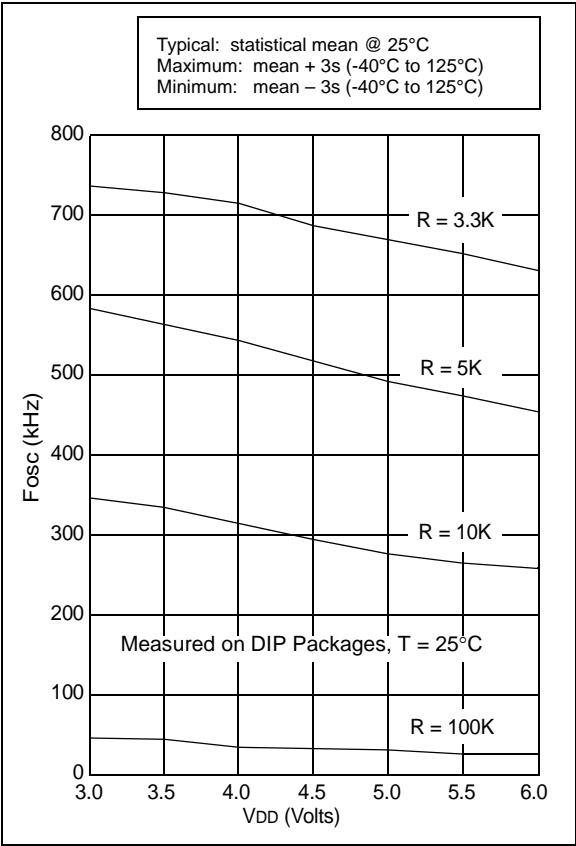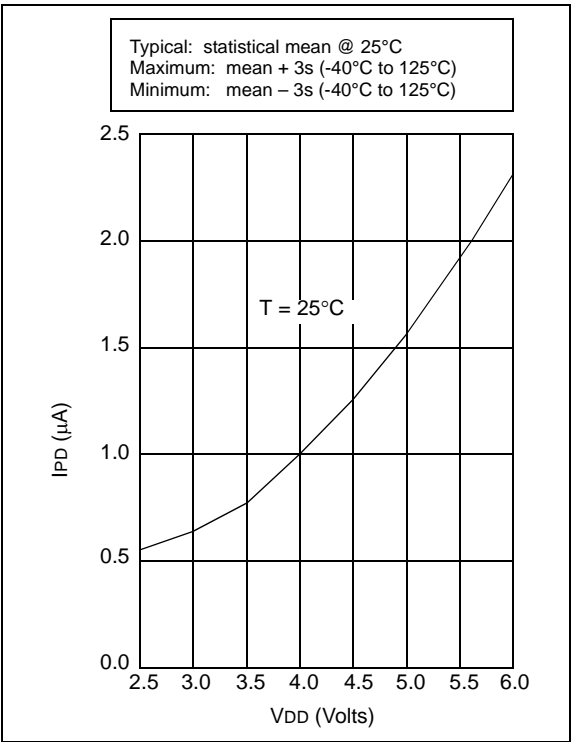**FIGURE 14-4:** **TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 300 PF**

FIGURE 14-5: **TYPICAL IPD vs. VDD, WATCHDOG DISABLED**

17.0 ELECTRICAL CHARACTERISTICS - PIC16LC54A

Absolute Maximum Ratings[†]

Ambient temperature under bias..−55°C to +125°C

Storage temperature .... −65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ....0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS}...0 to +14V

Voltage on all other pins with respect to V_{SS} .... −0.6V to (V_{DD} + 0.6V)

Total power dissipation[1] ....800 mW

Max. current out of V_{SS} pin ....150 mA

Max. current into V_{DD} pin ....100 mA

Max. current into an input pin (T0CKI only) ....±500 µA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})..±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ....±20 mA

Max. output current sunk by any I/O pin ....25 mA

Max. output current sourced by any I/O pin ....20 mA

Max. output current sourced by a single I/O (Port A, B or C) ....50 mA

Max. output current sunk by a single I/O (Port A, B or C) ....50 mA

Note 1: Power dissipation is calculated as follows: Pdis = V_{DD} x {I_{DD} - $\sum I_{OH}$} + $\sum$ {(V_{DD}-V_{OH}) x I_{OH}} + $\sum$(V_{OL} x I_{OL})

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
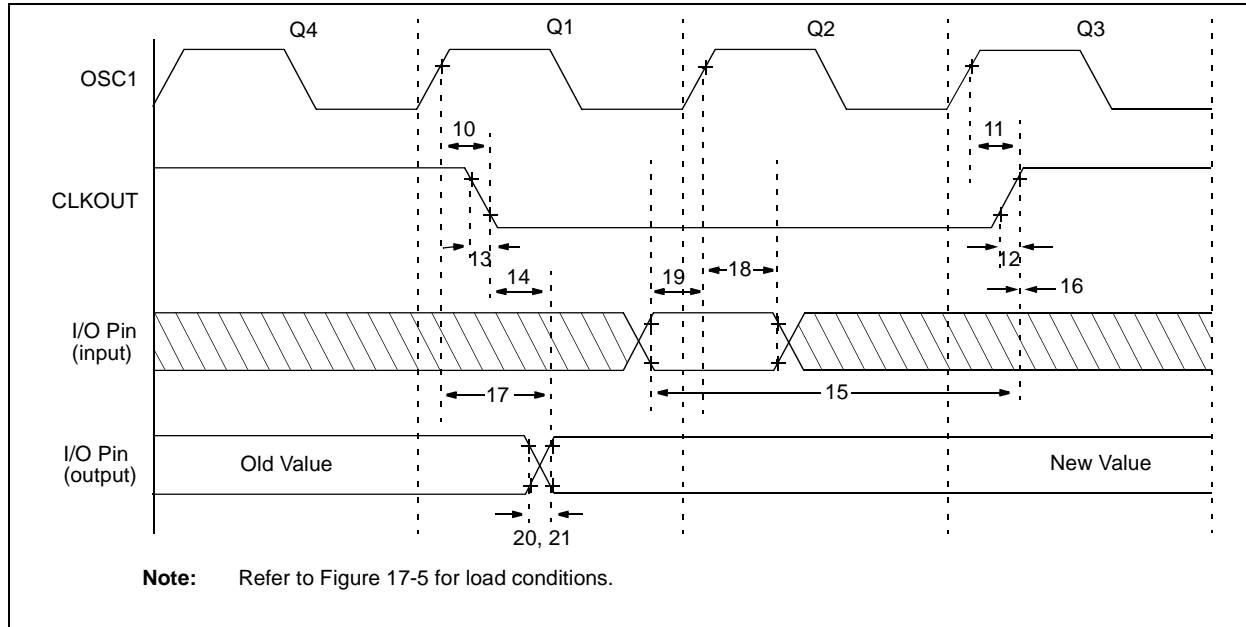
FIGURE 17-7: CLKOUT AND I/O TIMING - PIC16C5X, PIC16CR5X

Note: Refer to Figure 17-5 for load conditions.

TABLE 17-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \leq T_A \leq +70°C$ for commercial $-40°C \leq T_A \leq +85°C$ for industrial $-40°C \leq T_A \leq +125°C$ for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓[1]	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑[1]	—	15	30**	ns
12	TckR	CLKOUT rise time[1]	—	5.0	15**	ns
13	TckF	CLKOUT fall time[1]	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid[1]	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑[1]	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑[1]	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid[2]	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time[2]	—	10	25**	ns
21	TioF	Port output fall time[2]	—	10	25**	ns

*   These parameters are characterized but not tested.

**   These parameters are design targets and are not tested. No characterization data available at this time.

†   Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.
    2: Refer to Figure 17-5 for load conditions.

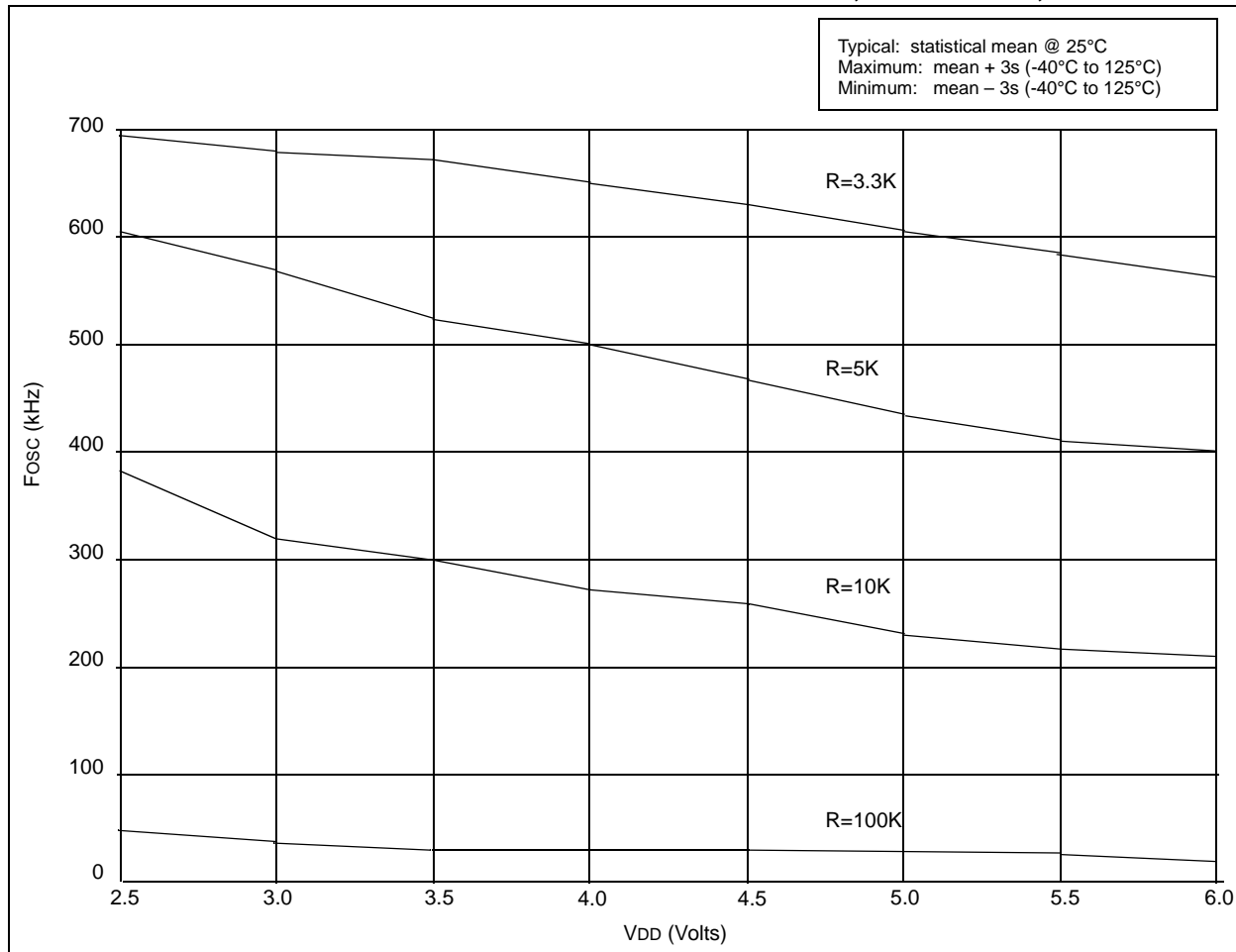**FIGURE 18-4:** **TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 PF, 25°C**

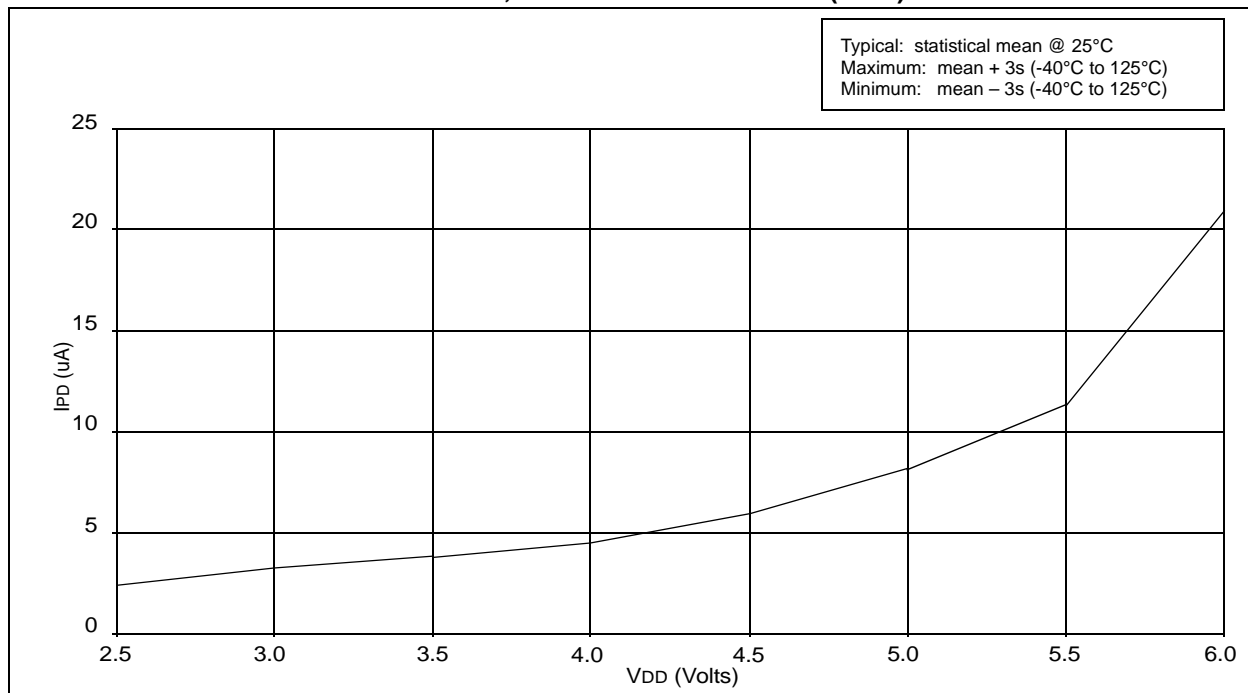**FIGURE 18-5:** **TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)**

PIC16C5X

FIGURE 18-6: **TYPICAL I**PD **vs. V**DD**, WATCHDOG ENABLED (25°C)**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

IPD (uA)

VDD (Volts)
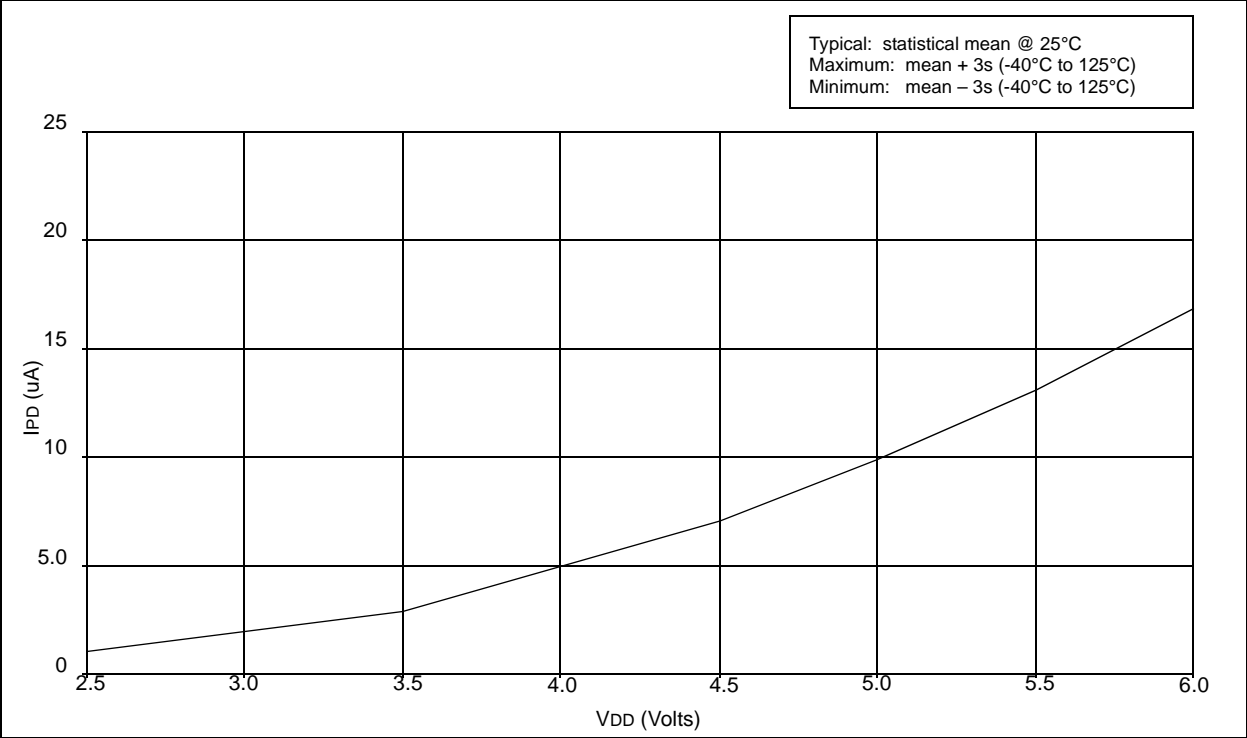
FIGURE 18-7: **TYPICAL I**PD **vs. V**DD**, WATCHDOG ENABLED (−40°C, 85°C)**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

IPD (uA)

(-40°C)

(+85°C)

VDD (Volts)

Preliminary
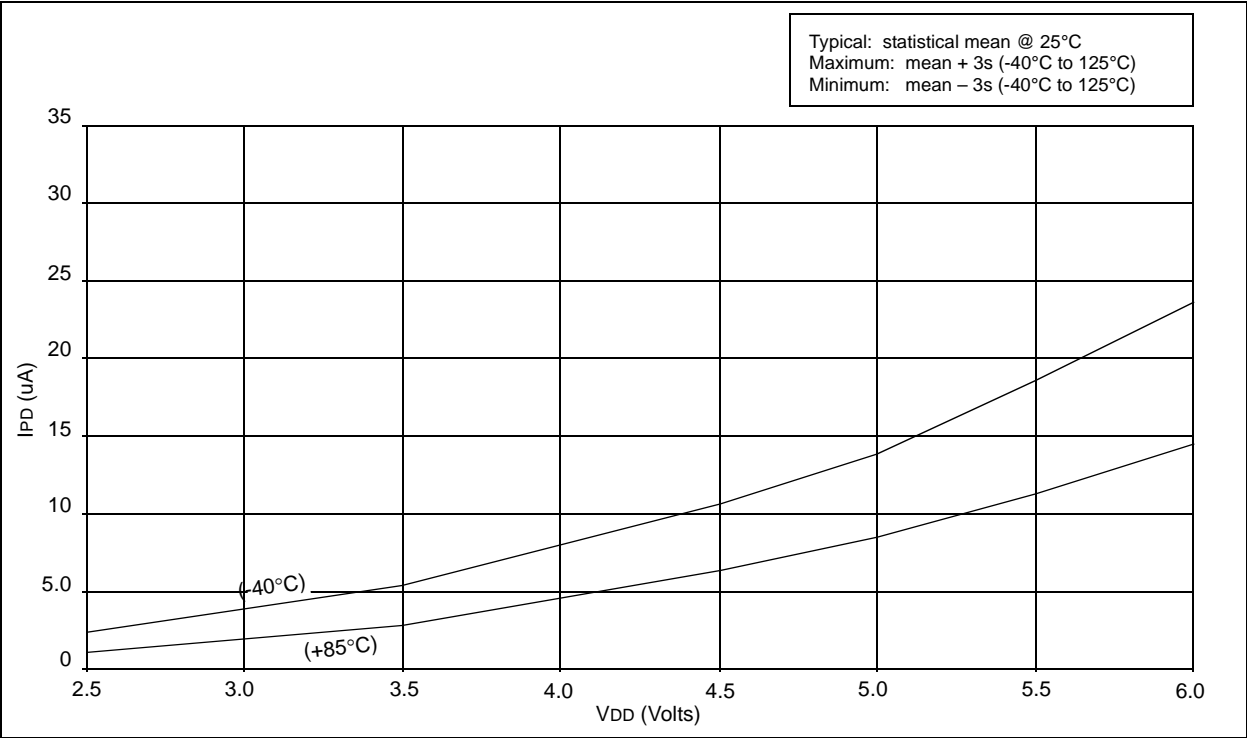
FIGURE 20-2: **TYPICAL I**PD **vs. V**DD**, WATCHDOG ENABLED (25°C)**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)
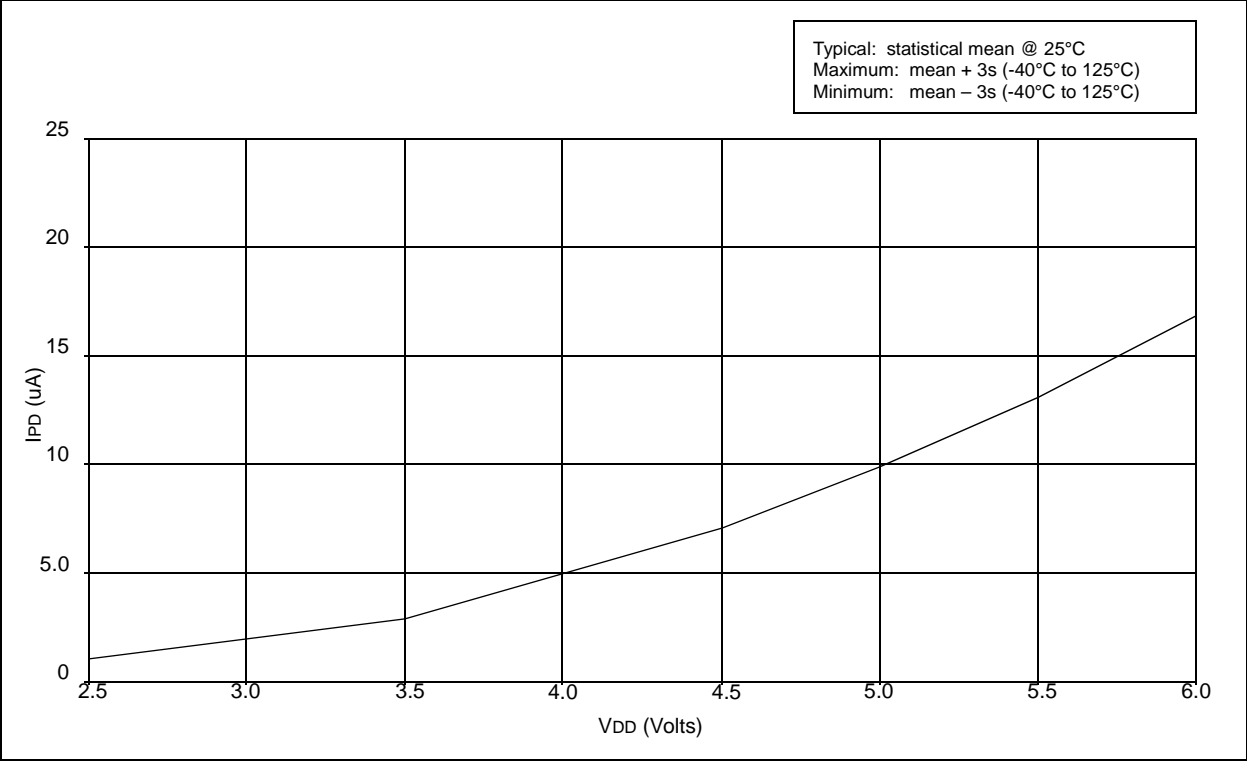
FIGURE 20-3: **TYPICAL I**PD **vs. V**DD**, WATCHDOG ENABLED (−40°C, 85°C)**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Preliminary
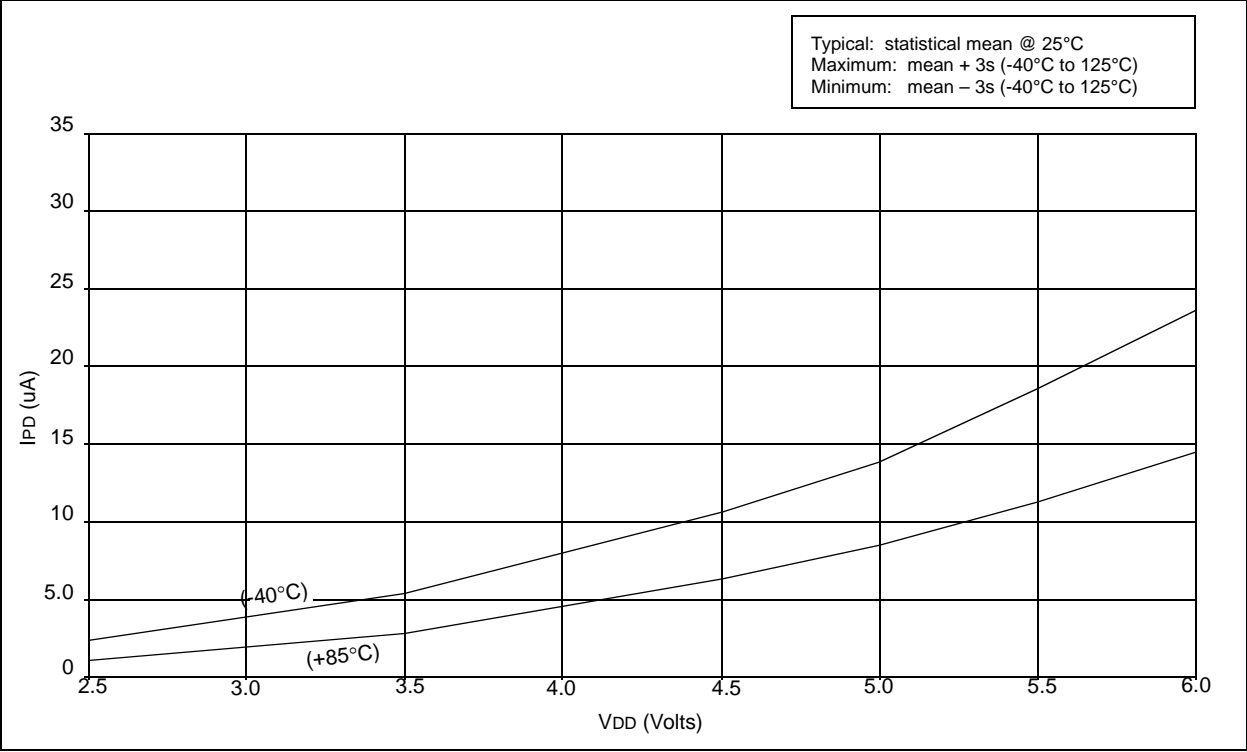
PIC16C5X

FIGURE 20-9:   IOL vs. VOL, VDD = 5 V

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Max –40°C

Typ +25°C

Min +85°C

IOL (mA)

VOL (Volts)

NOTES:

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