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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57-10-so

Email: info@E-XFL.COM

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Table of Contents

4.0		-
1.0	General Description	5
2.0	PIC16C5X Device Varieties	7
3.0	Architectural Overview	9
4.0	Oscillator Configurations	. 15
5.0	Reset	. 19
6.0	Memory Organization	. 25
7.0	I/O Ports	. 35
8.0	Timer0 Module and TMR0 Register	. 37
9.0	Special Features of the CPU	. 43
10.0	Instruction Set Summary	. 49
11.0	Development Support	. 61
12.0	Electrical Characteristics - PIC16C54/55/56/57	. 67
13.0	Electrical Characteristics - PIC16CR54A	. 79
14.0	Device Characterization - PIC16C54/55/56/57/CR54A	. 91
15.0	Electrical Characteristics - PIC16C54A	103
16.0	Device Characterization - PIC16C54A	117
17.0	Electrical Characteristics - PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B	131
18.0	Device Characterization - PIC16C54C/CR54C/C55A/C56A/CR56A/CR56A/CR57C/CR57C/C58B/CR58B	145
19.0	Electrical Characteristics - PIC16C54C/C55A/C56A/C57C/C58B 40MHz	155
20.0	Device Characterization - PIC16C54C/C55A/C56A/C57C/C58B 40MHz	165
21.0	Packaging Information	171
Appe	ndix A: Compatibility	182
On-L	ne Support	187
Read	er Response	188
Produ	uct Identification System	189

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4.0 OSCILLATOR CONFIGURATIONS

4.1 Oscillator Types

PIC16C5Xs can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- 1. LP: Low Power Crystal
- 2. XT: Crystal/Resonator
- 3. HS: High Speed Crystal/Resonator
- 4. RC: Resistor/Capacitor

Note: Not all oscillator selections available for all parts. See Section 9.1.

4.2 Crystal Oscillator/Ceramic Resonators

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 4-1). The PIC16C5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 4-2).

FIGURE 4-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



FIGURE 4-2:

EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)



TABLE 4-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS -PIC16C5X, PIC16CR5X

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	68-100 pF	68-100 pF
	2.0 MHz	15-33 pF	15-33 pF
	4.0 MHz	10-22 pF	10-22 pF
HS	8.0 MHz	10-22 pF	10-22 pF
	16.0 MHz	10 pF	10 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 4-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR -PIC16C5X. PIC16CR5X

Osc Type	Crystal Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz ⁽¹⁾	15 pF	15 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Note 1: For VDD > 4.5V, C1 = C2 \approx 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

Note: If you change from this device to another device, please verify oscillator characteristics in your application.

4.4 RC Oscillator

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 4-5 shows how the R/C combination is connected to the PIC16C5X. For REXT values below 2.2 k Ω , the oscillator operation may become unstable, or stop completely. For very high REXT values (e.g., 1 M Ω) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping REXT between 3 k Ω and 100 k Ω .

Although the oscillator will operate with no external capacitor (CEXT = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications sections for variation of oscillator frequency due to VDD for given REXT/ CEXT values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic.



Note: If you change from this device to another device, please verify oscillator characteristics in your application.

8.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

8.1.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 8-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

8.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 8-5 shows the delay from the external clock edge to the timer incrementing.



the error in measuring the interval between two edges on Timer0 input = ± 4 Tosc max.

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CALL	Subroutine Call			
Syntax:	[<i>label</i>] CALL k			
Operands:	$0 \le k \le 255$			
Operation:	$\begin{array}{l} (PC) + 1 \rightarrow TOS; \\ k \rightarrow PC < 7:0 >; \\ (STATUS < 6:5 >) \rightarrow PC < 10:9 >; \\ 0 \rightarrow PC < 8 > \end{array}$			
Status Affected:	None			
Encoding:	1001 kkkk kkkk			
Description.	Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two- cycle instruction.			
Words:	1			
Cycles:	2			
Example:	HERE CALL THERE			
Before Instruction PC = address (HERE) After Instruction PC = address (THERE) TOS = address (HERE + 1)				

CLRE	Clear f
	Cical I

Syntax:	[label]	CLRF f		
Operands:	$0 \le f \le 31$			
Operation:	$\begin{array}{l} 00h \rightarrow (f); \\ 1 \rightarrow Z \end{array}$			
Status Affected:	Z			
Encoding:	0000	011f	ffff	
Description:	The cont cleared a	ents of re and the Z	gister 'f' a bit is set.	are
Words:	1			
Cycles:	1			
Example:	CLRF	FLAG_RE	G	
Before Instruction FLAG_REG = 0x5A After Instruction				
FLAG_RI	EG =	0x00		
Z	=	1		

CLRW	Clear W
Syntax:	[label] CLRW
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow (W); \\ 1 \rightarrow Z \end{array}$
Status Affected:	Z
Encoding:	0000 0100 0000
Description:	The W register is cleared. Zero bit (Z) is set.
Words:	1
Cycles:	1
Example:	CLRW
VV = After Instruct W = Z =	= 0x5A tion = 0x00 = 1
CLRWDT	Clear Watchdog Timer
CLRWDT Syntax:	Clear Watchdog Timer
CLRWDT Syntax: Operands:	Clear Watchdog Timer [<i>label</i>] CLRWDT None
CLRWDT Syntax: Operands: Operation:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow \overline{TO};$ $1 \rightarrow \overline{PD}$
CLRWDT Syntax: Operands: Operation: Status Affected:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow \overline{TO};$ $1 \rightarrow \overline{PD}$ $\overline{TO}, \overline{PD}$
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding:	Clear Watchdog Timer[label]CLRWDTNone $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ \overline{TO}, PD 0000 0000
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description:	Clear Watchdog Timer[label] CLRWDTNone $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0100 The CLRWDT instruction resets theWDT. It also resets the prescaler, ifthe prescaler is assigned to theWDT and not Timer0. Status bitsTO and PD are set.
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description: Words:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0000 0100 The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set. 1
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	Clear Watchdog Timer [label] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0000 0100 The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set. 1 1
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0000 0100 The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set. 1 1 CLRWDT

After Instruction		
WDT counter	=	0x00
WDT prescaler	=	0
TO	=	1
PD	=	1

MOVWF	Move W	to f		
Syntax:	[label]	MOVWF	f	
Operands:	$0 \le f \le 31$			
Operation:	$(W) \rightarrow (f)$			
Status Affected:	None			
Encoding:	0000	001f	ffff	
Description:	Move dat register '	ta from th ".	e W regis	ster to
Words:	1			
Cycles:	1			
Example:	MOVWF	TEMP_RE	lG	
Before Instru TEMP_F W After Instructi TEMP_F W	ction REG = on REG = =	0xFF 0x4F 0x4F 0x4F 0x4F		

NOP	No Operation			
Syntax:	[label] NOP			
Operands:	None			
Operation:	No operation			
Status Affected:	None			
Encoding:	0000	0000	0000]
Description:	No operation.			
Words:	1			
Cycles:	1			
Example:	NOP			

OPTION	Load OI		egister	
Syntax:	[label]	OPTIO	N	
Operands:	None			
Operation:	$(W) \rightarrow C$	PTION		
Status Affected:	None			
Encoding:	0000	0000	0010	
Description:	The cont loaded in	tent of the	e W regis PTION re	ter is gister.
Words:	1			
Cycles:	1			
Example	OPTION			
Before Instruction				
W	= 0x	07		
After Instruction				
OPTION	= 0x	07		

RETLW	Return w	ith Liter	al in W			
Syntax:	[label]	RETLW	k			
Operands:	$0 \leq k \leq 25$	5				
Operation:	$k \rightarrow (W);$ TOS $\rightarrow P$	С				
Status Affected:	None					
Encoding:	1000	kkkk	kkkk			
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.					
Words:	1					
Cycles:	2					
Example:	CALL TAN	BLE ;W ;tal ;val ;W r ;val	contair ole offs lue. now has lue.	ns set table		
TABLE	ADDWF PC RETLW k: RETLW k:	C ;W = 1 ;Beg 2 ; n ; En	= offset gin tabl nd of ta	le le able		
Before Instru	ction					
W	= 0x0)7				
After Instruct	ion .	(1.5				
VV	= valu	ue of k8				

PIC16C5X

RLF	Rotate Left f through Carry						
Syntax:	[label] RLF	f,c				
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$						
Operation:	See d	escript	ion be	elow			
Status Affected:	С						
Encoding:	0011	. 01	df	ffff			
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.						
Words:	1						
Cycles:	1						
Example:	RLF	REG	£1,0				
Before Instru REG1 C After Instruct	ction = = ion	1110 0	0110	0			
REG1	=	1110	0110	C			
W	=	1100	1100	C			
С	=	1					

RRF	Rotate Right f through Carry					
Syntax:	[<i>label</i>] RRF f,d					
Operands:	$\begin{array}{l} 0\leq f\leq 31\\ d\in [0,1] \end{array}$					
Operation:	See description below					
Status Affected:	С					
Encoding:	0011 00df ffff					
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.					
Words:	1					
Cycles:	1					
Example:	RRF REG1,0					
Before Instru REG1 C	uction = 1110 0110 = 0					
REG1	= 1110 0110					
W C	= 0111 0011 = 0					

SLEEP	Enter SLEEP Mode						
Syntax:	[label]	SLEEP					
Operands:	None						
Operation:	$\begin{array}{l} 00h \rightarrow WDT; \\ 0 \rightarrow WDT \ prescaler; \ if \ assigned \\ 1 \rightarrow \overline{TO}; \\ 0 \rightarrow \overline{PD} \end{array}$						
Status Affected:	TO, PD						
Encoding:	0000	0000	0011				
Description:	Time-out status bit (TO) is set. The power-down status bit (PD) is cleared. The WDT and its pres- caler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more dotails						
Words:	1						
Cycles:	1						
Example:	SLEEP						

SUBWF	Subtr	act V	V from	f			
Syntax:	[label]	S	UBWF	f,d			
Operands:	$0 \le f \le d \in [0]$	≦ 31 (,1]					
Operation:	(f) – (^v	$W) \rightarrow$	(dest)				
Status Affected:	C, DC	;, Z					
Encoding:	0000) 1	LOdf	ffff			
Description:	Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.						
Words:	1						
Cycles:	1						
Example 1:	SUBW	F	REG1,	1			
Before Instruct REG1 W C After Instructi REG1 W C Example 2: Before Instructi REG1 W C After Instructi	ction = = on = = ction = = on	3 2 ? 1 2 1 2 ?	; resu	ılt is posi	tive		
REG1	=	0					
W	=	2					
С	=	1	; resu	ult is zero			
Example 3: Before Inst REG1 W C After Instructi	ructior = = = on	ו 1 2 ?					
REG1	=	0xFl	F				
W	=	2					
С	=	0	; resu	ılt is nega	ative		

SWAPF	Swap Nibbles in f				
Syntax:	[label] SWAPF f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$				
Operation:	$(f<3:0>) \rightarrow (dest<7:4>);$ $(f<7:4>) \rightarrow (dest<3:0>)$				
Status Affected:	None				
Encoding:	0011 10df ffff				
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.				
Words:	1				
Cycles:	1				
Example	SWAPF REG1, 0				
REG1 After Instructi REG1 W	= 0xA5 ion = 0xA5 = 0x5A				
TRIS	Load TRIS Register				
Syntax:	[<i>label</i>] TRIS f				
Operands:	f = 5, 6 or 7				
Operation:	$(W) \rightarrow TRIS$ register f				
Status Affected:	None				
Encoding:	0000 0000 0fff				
Description:	TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register.				
Words:	1				
Cycles:	1				
Example	TRIS PORTB				
Before Instruction W = 0xA5 After Instruction TRISB = 0xA5					

11.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB[®] IDE Software
- Assemblers/Compilers/Linkers
 - MPASM[™] Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK™ Object Linker/
 - MPLIB[™] Object Librarian
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - ICEPIC[™] In-Circuit Emulator
- In-Circuit Debugger
- MPLAB ICD
- Device Programmers
 - PRO MATE[®] II Universal Device Programmer
- PICSTART[®] Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
 - PICDEM[™]1 Demonstration Board
 - PICDEM 2 Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 17 Demonstration Board
 - KEELOQ[®] Demonstration Board

11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows[®]-based application that contains:

- An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file
 - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

11.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

12.1 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial)

PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial				
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions
D001	Vdd	Supply Voltage PIC16C5X-RC PIC16C5X-XT PIC16C5X-10 PIC16C5X-HS	3.0 3.0 4.5 4.5		6.25 6.25 5.5 5.5	V V V V	
D002	Vdr	PIC16C5X-LP RAM Data Retention Voltage ⁽¹⁾	2.5	 1.5*	6.25 —	V V	Device in SLEEP Mode
D003	Vpor	VDD Start Voltage to ensure Power-on Reset		Vss		V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*		—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current ⁽²⁾ PIC16C5X-RC ⁽³⁾ PIC16C5X-XT PIC16C5X-10 PIC16C5X-HS PIC16C5X-HS PIC16C5X-LP		1.8 1.8 4.8 9.0 15	3.3 3.3 10 10 20 32	mA mA mA mA μA	Fosc = 4 MHz, VDD = $5.5V$ Fosc = 4 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 20 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $3.0V$, WDT disabled
D020	IPD	Power-down Current ⁽²⁾		4.0 0.6	12 9	μΑ μΑ	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

13.6 Timing Diagrams and Specifications



FIGURE 13-2: EXTERNAL CLOCK TIMING - PIC16CR54A

TABLE 13-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A

AC Chara	cteristics	$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \ \ for \ commercial \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \ \ for \ industrial \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \ \ for \ extended \\ \end{array} $					
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
	Fosc	External CLKIN Frequency ⁽¹⁾	DC		4.0	MHz	XT OSC mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency ⁽¹⁾	DC		4.0	MHz	RC osc mode
			0.1	—	4.0	MHz	XT OSC mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	10	MHz	HS osc mode (10)
			4.0	—	20	MHz	HS osc mode (20)
			5.0		200	kHz	LP osc mode

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

AC Chara	cteristics	$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^\circ C \leq TA \leq +70^\circ C \ \ for \ commercial \\ -40^\circ C \leq TA \leq +85^\circ C \ \ for \ industrial \\ -40^\circ C \leq TA \leq +125^\circ C \ \ for \ extended \\ \end{array} $					
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
1	Tosc	External CLKIN Period ⁽¹⁾	250	—	—	ns	XT OSC mode
			250	—		ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—		μS	LP osc mode
		Oscillator Period ⁽¹⁾	250		_	ns	RC OSC mode
			250	—	10,000	ns	XT OSC mode
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	μS	LP osc mode
2	Тсу	Instruction Cycle Time ⁽²⁾	—	4/Fosc	_		
3	TosL, TosH	Clock in (OSC1) Low or High	50*		_	ns	XT oscillator
		Time	20*	—	—	ns	HS oscillator
			2.0*	—	—	μS	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall	_	_	25*	ns	XT oscillator
		lime	—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

TABLE 13-1:	EXTERNAL CLOCK TIMING REQUIREMENT	S - PIC16CR54A

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

14.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.





TABLE 14-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Average Fosc @ 5 V, 25°C				
20 pF	3.3K	5 MHz	± 27%			
	5K	3.8 MHz	± 21%			
	10K	2.2 MHz	± 21%			
	100K	262 kHz	± 31%			
100 pF	3.3K	1.6 MHz	± 13%			
	5K	1.2 MHz	± 13%			
	10K	684 kHz	± 18%			
	100K	71 kHz	± 25%			
300 pF	3.3K	660 kHz	± 10%			
	5.0K	484 kHz	± 14%			
	10K	267 kHz	± 15%			
	100K	29 kHz	± 19%			

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviations from the average value for VDD = 5V.



TABLE 15-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54A

	Standard Operating Conditions (unless otherwise specified)							
	Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial							
	AC Chara	acteristics	-40°C ≤	$TA \le +8$	85°C fo	or indus	trial	
			–20°C ≤	$TA \leq +8$	85°C fc	or indus	trial - PIC16LV54A-02I	
			-40°C ≤	TA ≤ +1	25°C	for exte	nded	
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
40	Tt0H	T0CKI High Pulse Width						
		- No Prescaler	0.5 TCY + 20*	—	—	ns		
		- With Prescaler	10*			ns		
41	Tt0L	T0CKI Low Pulse Width						
		- No Prescaler	0.5 TCY + 20*	—	—	ns		
		- With Prescaler	10*			ns		
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> *	_	_	ns	Whichever is greater.	
			N				N = Prescale Value	
							(1, 2, 4,, 256)	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

16.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.



FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

TABLE 16-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Average Fosc @ 5 V, 25°C				
20 pF	3.3K	5 MHz	± 27%			
	5K	3.8 MHz	± 21%			
	10K	2.2 MHz	± 21%			
	100K	262 kHz	± 31%			
100 pF	3.3K	1.6 MHz	± 13%			
	5K	1.2 MHz	± 13%			
	10K	684 kHz	± 18%			
	100K	71 kHz	± 25%			
300 pF	3.3K	660 kHz	± 10%			
	5.0K	484 kHz	± 14%			
	10K	267 kHz	± 15%			
	100K	29 kHz	± 19%			

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for VDD = 5V.

17.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial) PIC16C5X PIC16CR5X (Commercial, Industrial)								
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions	
	Vdd	Supply Voltage						
D001		PIC16LC5X	2.5 2.7 2.5		5.5 5.5 5.5	V V V	$\begin{array}{l} -40^{\circ}C \leq TA \leq +\ 85^{\circ}C,\ 16LCR5X \\ -40^{\circ}C \leq TA \leq 0^{\circ}C,\ 16LC5X \\ 0^{\circ}C \leq TA \leq +\ 85^{\circ}C \ 16LC5X \end{array}$	
D001A		PIC16C5X	3.0 4.5		5.5 5.5	V V	RC, XT, LP and HS mode from 0 - 10 MHz from 10 - 20 MHz	
D002	Vdr	RAM Data Retention Volt- age ⁽¹⁾	-	1.5*	-	V	Device in SLEEP mode	
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	_	Vss	—	V	See Section 5.1 for details on Power-on Reset	
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	_	V/ms	See Section 5.1 for details on Power-on Reset	

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

$\begin{tabular}{ c c c c c } \label{eq:AC Characteristics} AC Characteristics & Standard Operating Conditions (unless otherwise specified) \\ Operating Temperature & 0°C \leq TA \leq +70°C \mbox{ for commercial} \\ -40°C \leq TA \leq +85°C \mbox{ for industrial} \\ -40°C \leq TA \leq +125°C \mbox{ for extended} \end{tabular}$					1)		
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions
2	Тсу	Instruction Cycle Time ⁽²⁾	—	4/Fosc			
3	TosL, TosH Clock	Clock in (OSC1) Low or High Time	50*		_	ns	XT oscillator
			20*	—	_	ns	HS oscillator
			2.0*	—	_	μS	LP oscillator
4	4 TosR, TosF Clock in Time	Clock in (OSC1) Rise or Fall Time	_		25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	_	50*	ns	LP oscillator

- * These parameters are characterized but not tested.
- † Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- **Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.









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TABLE 19-2:	CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X-40

AC Chara	acteristics	Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial						
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units		
10	TosH2ckL	OSC1↑ to CLKOUT↓ ^(1,2)		15	30**	ns		
11	TosH2ckH	OSC1↑ to CLKOUT↑ ^(1,2)	—	15	30**	ns		
12	TckR	CLKOUT rise time ^(1,2)	—	5.0	15**	ns		
13	TckF	CLKOUT fall time ^(1,2)	—	5.0	15**	ns		
14	TckL2ioV	CLKOUT↓ to Port out valid ^(1,2)	—		40**	ns		
15	TioV2ckH	Port in valid before CLKOUT ^(1,2)	0.25 TCY+30*	—	—	ns		
16	TckH2iol	Port in hold after CLKOUT ^(1,2)	0*	—	—	ns		
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽²⁾	—	—	100	ns		
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns		
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns		
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns		
21	TioF	Port output fall time ⁽²⁾		10	25**	ns		

* These parameters are characterized but not tested.

- ** These parameters are design targets and are not tested. No characterization data available at this time.
- † Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Refer to Figure 19-2 for load conditions.

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FIGURE 20-9: IOL vs. VOL, VDD = 5 V

