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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57-10i-so

Email: info@E-XFL.COM

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3.1 **Clocking Scheme/Instruction** Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2 and Example 3-1.

3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).



FIGURE 3-2: **CLOCK/INSTRUCTION CYCLE**

EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



is "flushed" from the pipeline, while the new instruction is being fetched and then executed.

5.0 RESET

PIC16C5X devices may be RESET in one of the following ways:

- Power-On Reset (POR)
- MCLR Reset (normal operation)
- MCLR Wake-up Reset (from SLEEP)
- WDT Reset (normal operation)
- WDT Wake-up Reset (from SLEEP)

Table 5-1 shows these RESET conditions for the PCL and STATUS registers.

Some registers are not affected in any RESET condition. Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-On Reset (POR), MCLR or WDT Reset. A MCLR or WDT wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP. The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits (STATUS <4:3>) are set or cleared depending on the different RESET conditions (Table 5-1). These bits may be used to determine the nature of the RESET.

Table 5-3 lists a full description of RESET states of all registers. Figure 5-1 shows a simplified block diagram of the On-chip Reset circuit.

TABLE 5-1: STATUS BITS AND THEIR SIGNIFICANCE

Condition	то	PD		
Power-On Reset	1	1		
MCLR Reset (normal operation)	u	u		
MCLR Wake-up (from SLEEP)	1	0		
WDT Reset (normal operation)	0	1		
WDT Wake-up (from SLEEP)	0	0		

Legend: u = unchanged, x = unknown, - = unimplemented read as '0'.

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH RESET

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	<u>Value</u> on MCLR and WDT Reset
03h	STATUS	PA2	PA1	PA0	TO	PD	Z	DC	С	0001 1xxx	000q quuu

Legend: u = unchanged, x = unknown, q = see Table 5-1 for possible values.

5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the MCLR/VPP pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is <u>RESET</u>. The DRT timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where MCLR is not tied to VDD is shown in Figure 5-3. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset TDRT msec after MCLR goes high.

In Figure 5-4, the on-chip Power-On Reset feature is being used (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the MCLR/VPP pin, and when the MCLR/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

Note: When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the <u>Embedded Control Handbook</u>.

The POR circuit does not produce an internal RESET when VDD declines.

FIGURE 5-2:

EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 k Ω will limit any current flowing into \overline{MCLR} from external capacitor C in the event of \overline{MCLR} pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

6.5.1 PAGING CONSIDERATIONS – PIC16C56/CR56, PIC16C57/CR57 AND PIC16C58/CR58

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS Register will not be updated. Therefore, the next GOTO, CALL or modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA<1:0>).

For example, a NOP at location 1FFh (page 0) increments the PC to 200h (page 1). A GOTO xxx at 200h will return the program to address xxh on page 0 (assuming that PA<1:0> are clear).

To prevent this, the page preselect bits must be updated under program control.

6.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the RESET vector).

The STATUS Register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a GOTO instruction at the RESET vector location will automatically cause the program to jump to page 0.

6.6 Stack

PIC16C5X devices have a 10-bit or 11-bit wide, two-level hardware push/pop stack.

A CALL instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W Register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the RETLW instruction, the PC is loaded with the Top of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC, therefore, paging is not an issue when returning from a subroutine.

8.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
 - Readable and writable
- 8-bit software programmable prescaler
- · Internal or external clock select
- Edge select for external clock

Figure 8-1 is a simplified block diagram of the Timer0 module, while Figure 8-2 shows the electrical structure of the Timer0 input.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 8-3 and Figure 8-4). The user can work around this by writing an adjusted value to the TMR0 register.



Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 8.1.

Note: The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both.

The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 8.2 details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 8-1.



FIGURE 8-2: ELECTRICAL STRUCTURE OF TOCKI PIN







FIGURE 8-4: TIMER0 TIMING: INTERNAL CLOCK/PRESCALER 1:2



TABLE 8-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	<u>Value</u> on MCLR and WDT Reset
01h	TMR0	Timer0 -	8-bit real	-time cloc	ck/counter					xxxx xxxx	uuuu uuuu
N/A	OPTION	_	_	TOCS	TOSE	PSA	PS2	PS1	PS0	11 1111	11 1111

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells not used by Timer0.

9.1 Configuration Bits

Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. Nine bits are code protection bits for the PIC16C54A, PIC16CR54A, PIC16C55A, PIC16C56A, PIC16CR56A, PIC16CR57C, PIC16CR57C, PIC16CR57C,

PIC16C58B, and PIC16CR58B devices (Register 9-1). One bit is for code protection for the PIC16C54, PIC16C55, PIC16C56 and PIC16C57 devices (Register 9-2).

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" diagrams in the back of this data sheet).

REGISTER 9-1: CONFIGURATION WORD FOR PIC16C54A/CR54A/C54C/CR54C/C55A/C56A/ CR56A/C57C/CR57C/C58B/CR58B

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0
bit 11											bit 0

bit 11-3: CP: Code Protection Bit

- 1 = Code protection off
 - 0 =Code protection on
- bit 2: WDTE: Watchdog timer enable bit
 - 1 = WDT enabled
 - 0 = WDT disabled

bit 1-0: FOSC1:FOSC0: Oscillator Selection Bit

- 00 = LP oscillator
- 01 = XT oscillator
- 10 = HS oscillator
- 11 = RC oscillator

Note 1: Refer to the PIC16C5X Programming Specification (Literature Number DS30190) to determine how to access the configuration word.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

10.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 10-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers in that bank is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 10-1:	OPCODE FIELD
	DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x1F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1)
	The assembler will generate code with $x = 0$.
	It is the recommended form of use for com-
	patibility with all Microchip software tools.
d	Destination select;
	d = 0 (store result in W)
	d = 1 (store result in file register 'f')
	Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
TO	Time-out bit
PD	Power-down bit
dest	Destination, either the W register or the
	specified register file location
[]	Options
()	Contents
\rightarrow	Assigned to
< >	Register bit field
E	In the set of
italics	User defined term (font is courier)

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time would be 1 μ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time would be 2 μ s.

Figure 10-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations										
<u>11 6</u>	5	4 0								
OPCODE	d	f (FILE #)								
d = 0 for destination d = 1 for destination f = 5-bit file registe	d = 0 for destination W d = 1 for destination f f = 5-bit file register address									
Bit-oriented file register	r ope	erations								
11 8	7	5 4 0								
OPCODE	b (Bl	IT #) f (FILE #)								
Literal and control ope	ratio	ns (except GOTO)								
<u>11</u>	8	7 0								
OPCODE		k (literal)								
k = 8-bit immediat	e va	lue								
Literal and control operations - GOTO instruction										
11	9	8 0								
OPCODE		k (literal)								
k = 9-bit immediate value										

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12.2 DC Characteristics: PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

PIC16C (Indus	54/55/56/ trial)	57-RCI, XTI, 10I, HSI, LPI	Stand Opera	Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial					
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions		
D001	Vdd	Supply Voltage PIC16C5X-RCI PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-HSI	3.0 3.0 4.5 4.5		6.25 6.25 5.5 5.5 6.25	V V V V			
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	2.5	1.5*		V	Device in SLEEP mode		
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset		
D010	IDD	Supply Current ⁽²⁾ PIC16C5X-RCI ⁽³⁾ PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-HSI PIC16C5X-LPI		1.8 1.8 4.8 9.0 15	3.3 3.3 10 10 20 40	mA mA mA mA μA	Fosc = 4 MHz, VDD = $5.5V$ Fosc = 4 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 20 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $3.0V$, WDT disabled		
D020	IPD	Power-down Current ⁽²⁾	_	4.0 0.6	14 12	μΑ μΑ	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled		

* These parameters are characterized but not tested.

- † Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

FIGURE 12-5: TIMER0 CLOCK TIMINGS - PIC16C54/55/56/57



TABLE 12-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54/55/56/57

AC Ch	AC CharacteristicsStandard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended								
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions		
40	Tt0H	TOCKI High Pulse Width - No Prescaler - With Prescaler	0.5 Tcy + 20* 10*		_	ns ns			
41	TtOL	T0CKI Low Pulse Width - No Prescaler - With Prescaler	0.5 Tcy + 20* 10*			ns ns			
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> * N	_	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)		

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04 PIC16LC54A-04I (Commercial, Industrial)				ard Ope ting Tem	perating	J Condi ure 	tions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $40^{\circ}C \le TA \le +85^{\circ}C$ for industrial		
PIC16C54A-04, 10, 20 PIC16C54A-04I, 10I, 20I (Commercial, Industrial)			Standa Operat	Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial					
Param No.	Symbol	Characteristic/Device	Min Typ† Max Units Conditions						
	IPD	Power-down Current ⁽²⁾							
D006		PIC16LC5X	—	2.5	12	μΑ	VDD = 2.5V, WDT enabled, Commercial		
			—	0.25	4.0	μΑ	VDD = 2.5V, WDT disabled, Commercial		
			_	0.25	5.0	μΑ μΑ	VDD = 2.5V, WDT enabled, industrial $VDD = 2.5V$, WDT disabled, Industrial		
D006A		PIC16C5X	_	4.0	12	μΑ	VDD = 3.0V, WDT enabled, Commercial		
			—	0.25	4.0	μA	VDD = 3.0V, WDT disabled, Commercial		
			—	5.0	14	μΑ	VDD = 3.0V, WDT enabled, Industrial		
				0.3	5.0	μA	$v \Box U = 3.0v, v U T uisabled, industrial$		

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

15.6 Timing Diagrams and Specifications

FIGURE 15-2: EXTERNAL CLOCK TIMING - PIC16C54A



TABLE 15-1:	EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

AC Chara	acteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
	Fosc	External CLKIN Fre-	DC		4.0	MHz	XT OSC mode	
		quency ⁽¹⁾	DC	—	2.0	MHz	XT osc mode (PIC16LV54A)	
			DC	—	4.0	MHz	HS osc mode (04)	
			DC	—	10	MHz	HS osc mode (10)	
			DC	—	20	MHz	HS osc mode (20)	
			DC	—	200	kHz	LP osc mode	
		Oscillator Frequency ⁽¹⁾	DC	_	4.0	MHz	RC osc mode	
			DC	—	2.0	MHz	RC osc mode (PIC16LV54A)	
			0.1	—	4.0	MHz	XT osc mode	
			0.1	—	2.0	MHz	XT osc mode (PIC16LV54A)	
			4.0	—	4.0	MHz	HS osc mode (04)	
			4.0	—	10	MHz	HS osc mode (10)	
			4.0	—	20	MHz	HS osc mode (20)	
			5.0		200	kHz	LP osc mode	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.
 - Instruction cycle period (TcY) equals four times the input oscillator time base period.



FIGURE 16-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 PF, 25°C

PIC16C5X

FIGURE 16-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)







FIGURE 16-18: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD



FIGURE 16-19:

TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD



19.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)⁽¹⁾

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial						
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions	
D030	VIL	Input Low Voltage I/O Ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1	Vss Vss Vss Vss		0.8 0.15 VDD 0.15 VDD 0.2 VDD	V V V V	4.5V <vdd <math="">\leq 5.5V HS, 20 MHz \leq Fosc \leq 40 MHz</vdd>	
D040	Viн	Input High Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1	2.0 0.85 Vdd 0.85 Vdd 0.85 Vdd		Vdd Vdd Vdd Vdd	V V V V	4.5V < VDD ≤ 5.5V HS, 20 MHz ≤ Fosc ≤ 40 MHz	
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	—	—	V		
D060	ΙιL	Input Leakage Current ^(2,3) I/O ports MCLR MCLR	-1.0 -5.0 —	0.5 — 0.5	+1.0 +5.0 +3.0	μΑ μΑ μΑ	For VDD \leq 5.5V: VSS \leq VPIN \leq VDD, pin at hi-impedance VPIN = VSS +0.25V VPIN = VDD	
		T0CKI OSC1	-3.0 -3.0	0.5 0.5	+3.0	μA μA	$\begin{array}{l} Vss \leq VPIN \leq VDD \\ Vss \leq VPIN \leq VDD, \textbf{HS} \end{array}$	
D080	Vol	Output Low Voltage I/O ports	_	_	0.6	V	IOL = 8.7 mA, VDD = 4.5V	
D090	Vон	Output High Voltage ⁽³⁾ I/O ports	Vdd - 0.7	_	_	V	Іон = -5.4 mA, Vdd = 4.5V	

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected and HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 17.3.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

NOTES:

18-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging



	Units		INCHES*		MILLIMETERS			
Dimension	MIN	NOM	MAX	MIN	NOM	MAX		
Number of Pins	n		18			18		
Pitch	р		.050			1.27		
Overall Height	Α	.093	.099	.104	2.36	2.50	2.64	
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39	
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30	
Overall Width	E	.394	.407	.420	10.01	10.34	10.67	
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59	
Overall Length	D	.446	.454	.462	11.33	11.53	11.73	
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74	
Foot Length	L	.016	.033	.050	0.41	0.84	1.27	
Foot Angle	¢	0	4	8	0	4	8	
Lead Thickness	С	.009	.011	.012	0.23	0.27	0.30	
Lead Width	В	.014	.017	.020	0.36	0.42	0.51	
Mold Draft Angle Top	α	0	12	15	0	12	15	
Mold Draft Angle Bottom	β	0	12	15	0	12	15	

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013 Drawing No. C04-051

18-Lead Ceramic Dual In-line with Window (JW) - 300 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		INCHES*		MILLIMETERS			
Dimension	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		18			18	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	.880	.900	.920	22.35	22.86	23.37
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.055	.060	1.27	1.40	1.52
Lower Lead Width	В	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing §	eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length		.190	.200	.210	4.83	5.08	5.33

* Controlling Parameter § Significant Characteristic JEDEC Equivalent: MO-036

Drawing No. C04-010

APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

- 1. Check any CALL, GOTO or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
- 2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change RESET vector to proper value for processor used.
- 6. Remove any use of the ADDLW, RETURN and SUBLW instructions.
- 7. Rewrite any code segments that use interrupts.

APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.