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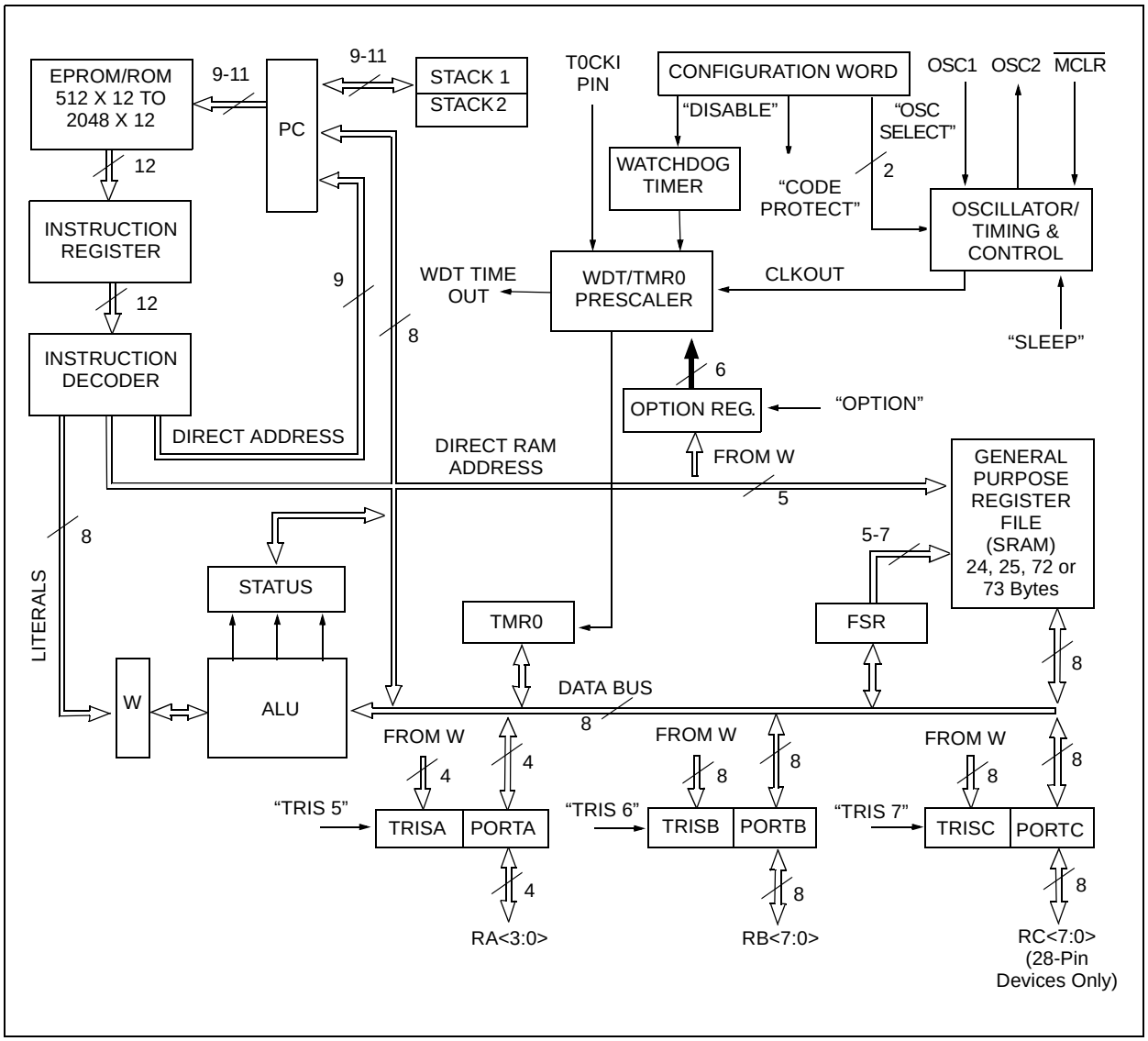
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 20 |
| Program Memory Size | 3KB (2K x 12) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 72 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.600", 15.24mm) |
| Supplier Device Package | 28-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16c57-hse-p |

**FIGURE 3-1: PIC16C5X SERIES BLOCK DIAGRAM**



## 3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2 and Example 3-1.

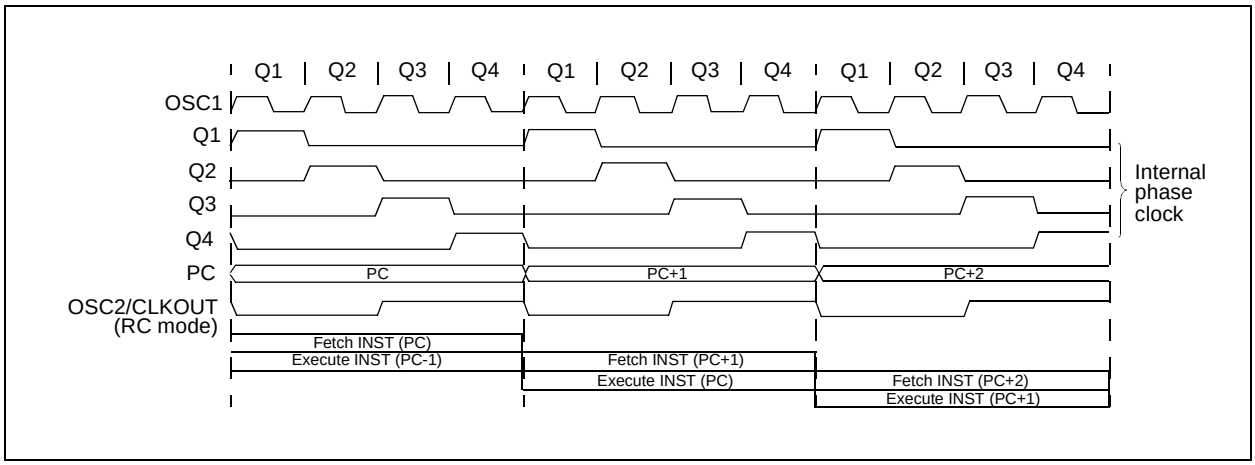
## 3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., `GOTO`), then two cycles are required to complete the instruction (Example 3-1).

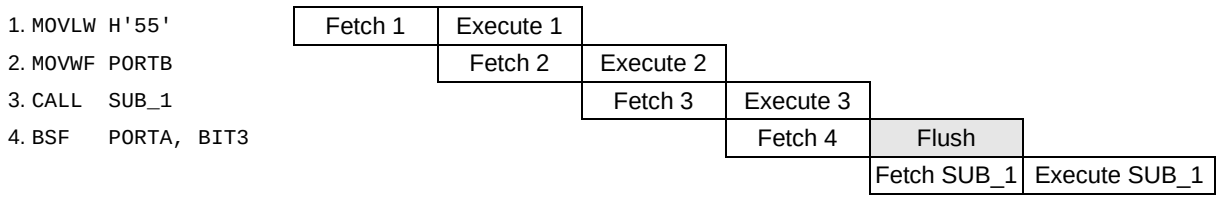
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

**FIGURE 3-2: CLOCK/INSTRUCTION CYCLE**




**EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW**




All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is “flushed” from the pipeline, while the new instruction is being fetched and then executed.

## 6.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers and General Purpose Registers.

The Special Function Registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Purpose Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

For the PIC16C54, PIC16CR54, PIC16C56 and PIC16CR56, the register file is composed of 7 Special Function Registers and 25 General Purpose Registers (Figure 6-4).

For the PIC16C55, the register file is composed of 8 Special Function Registers and 24 General Purpose Registers.

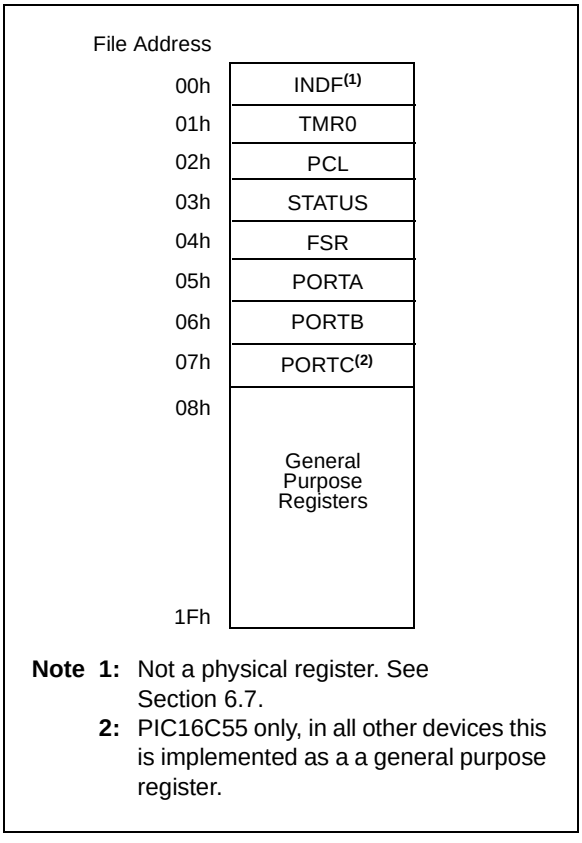
For the PIC16C57 and PIC16CR57, the register file is composed of 8 Special Function Registers, 24 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-5).

For the PIC16C58 and PIC16CR58, the register file is composed of 7 Special Function Registers, 25 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-6).

### 6.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the File Select Register (FSR). The FSR Register is described in Section 6.7.

**FIGURE 6-4: PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56 REGISTER FILE MAP**




**Note 1:** Not a physical register. See Section 6.7.

**2:** PIC16C55 only, in all other devices this is implemented as a a general purpose register.

**ADDWF** **Add W and f**

Syntax: [ *label* ] ADDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

| 0001 | 11df | ffff |
|---|---|---|

Description: Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ADDWF  TEMP_REG, 0
```
Before Instruction
W = 0x17
TEMP_REG = 0xC2
After Instruction
W = 0xD9
TEMP_REG = 0xC2

**ANDWF** **AND W with f**

Syntax: [ *label* ] ANDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) .AND. (f) → (dest)

Status Affected: Z

Encoding:

| 0001 | 01df | ffff |
|---|---|---|

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ANDWF  TEMP_REG, 1
```
Before Instruction
W = 0x17
TEMP_REG = 0xC2
After Instruction
W = 0x17
TEMP_REG = 0x02

**ANDLW** **AND literal with W**

Syntax: [ *label* ] ANDLW k

Operands: $0 \le k \le 255$

Operation: (W).AND. (k) → (W)

Status Affected: Z

Encoding:

| 1110 | kkkk | kkkk |
|---|---|---|

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ANDLW  H'5F'
```
Before Instruction
W = 0xA3
After Instruction
W = 0x03

**BCF** **Bit Clear f**

Syntax: [ *label* ] BCF f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: 0 → (f<b>)

Status Affected: None

Encoding:

| 0100 | bbbf | ffff |
|---|---|---|

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example:
```
BCF    FLAG_REG,  7
```
Before Instruction
FLAG_REG = 0xC7
After Instruction
FLAG_REG = 0x47

**COMF** **Complement f**

Syntax: [ *label* ] COMF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(\bar{f}) \rightarrow (dest)$

Status Affected: Z

Encoding:

| 0010 | 01df | ffff |
|---|---|---|

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
COMF   REG1,0
```
Before Instruction
REG1 = 0x13
After Instruction
REG1 = 0x13
W = 0xEC

**DECF** **Decrement f**

Syntax: [ *label* ] DECF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – 1 → (dest)

Status Affected: Z

Encoding:

| 0000 | 11df | ffff |
|---|---|---|

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
DECF    CNT, 1
```
Before Instruction
CNT = 0x01
Z = 0
After Instruction
CNT = 0x00
Z = 1

**DECFSZ** **Decrement f, Skip if 0**

Syntax: [ *label* ] DECFSZ f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – 1 → d; skip if result = 0

Status Affected: None

Encoding:

| 0010 | 11df | ffff |
|---|---|---|

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE      DECFSZ   CNT, 1
          GOTO     LOOP
CONTINUE  •
          •
          •
```
Before Instruction
PC = address (HERE)
After Instruction
CNT = CNT - 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT ≠ 0,
PC = address (HERE+1)

**RLF** **Rotate Left f through Carry**

Syntax: [ *label* ] RLF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

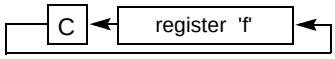
Operation: See description below

Status Affected: C

Encoding:

| 0011 | 01df | ffff |
|---|---|---|

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.




Words: 1

Cycles: 1

Example:
```
RLF    REG1,0
```
Before Instruction
```
REG1    =  1110 0110
C       =  0
```
After Instruction
```
REG1    =  1110 0110
W       =  1100 1100
C       =  1
```

**RRF** **Rotate Right f through Carry**

Syntax: [ *label* ] RRF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

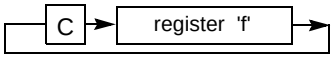
Operation: See description below

Status Affected: C

Encoding:

| 0011 | 00df | ffff |
|---|---|---|

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.




Words: 1

Cycles: 1

Example:
```
RRF    REG1,0
```
Before Instruction
```
REG1    =  1110 0110
C       =  0
```
After Instruction
```
REG1    =  1110 0110
W       =  0111 0011
C       =  0
```

**SLEEP** **Enter SLEEP Mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler; if assigned
1 → $\overline{TO}$;
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

| 0000 | 0000 | 0011 |
|---|---|---|

Description: Time-out status bit ($\overline{TO}$) is set. The power-down status bit ($\overline{PD}$) is cleared. The WDT and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example:
```
SLEEP
```

## 12.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

**Absolute Maximum Ratings(†)**

Ambient Temperature under bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on $V_{DD}$ with respect to $V_{SS}$ .....0V to +7.5V

Voltage on $\overline{MCLR}$ with respect to $V_{SS}$(1) .....0V to +14V

Voltage on all other pins with respect to $V_{SS}$ .....–0.6V to ($V_{DD}$ + 0.6V)

Total power dissipation(2) ..... 800 mW

Max. current out of $V_{SS}$ pin ..... 150 mA

Max. current into $V_{DD}$ pin ..... 100 mA

Max. current into an input pin (T0CKI only)..... ±500 μA

Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA

Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) ..... ±20 mA

Max. output current sunk by any I/O pin ..... 25 mA

Max. output current sourced by any I/O pin ..... 20 mA

Max. output current sourced by a single I/O port (PORTA, B or C) ..... 40 mA

Max. output current sunk by a single I/O port (PORTA, B or C)..... 50 mA

**Note 1:** Voltage spikes below $V_{SS}$ at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to $V_{SS}$.

**2:** Power Dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57**

| AC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 1 | TOSC | External CLKIN Period(1) | 250 | — | — | ns | XT OSC mode |
| | | | 100 | — | — | ns | 10 MHz mode |
| | | | 50 | — | — | ns | HS OSC mode (Comm/Ind) |
| | | | 62.5 | — | — | ns | HS OSC mode (Ext) |
| | | | 25 | — | — | µs | LP OSC mode |
| | | Oscillator Period(1) | 250 | — | — | ns | RC OSC mode |
| | | | 250 | — | 10,000 | ns | XT OSC mode |
| | | | 100 | — | 250 | ns | 10 MHz mode |
| | | | 50 | — | 250 | ns | HS OSC mode (Comm/Ind) |
| | | | 62.5 | — | 250 | ns | HS OSC mode (Ext) |
| | | | 25 | — | — | µs | LP OSC mode |
| 2 | Tcy | Instruction Cycle Time(2) | — | 4/FOSC | — | — | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 85* | — | — | ns | XT oscillator |
| | | | 20* | — | — | ns | HS oscillator |
| | | | 2.0* | — | — | µs | LP oscillator |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 25* | ns | XT oscillator |
| | | | — | — | 25* | ns | HS oscillator |
| | | | — | — | 50* | ns | LP oscillator |

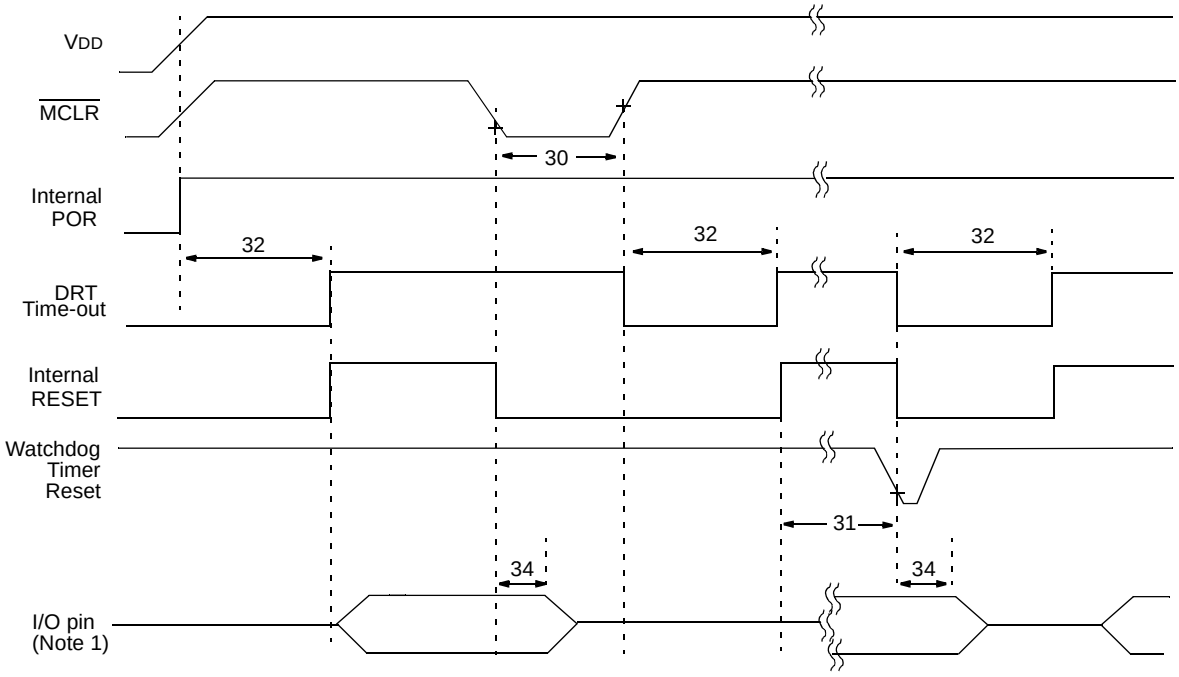
* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

**FIGURE 12-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54/55/56/57**




**Note 1:** Please refer to Figure 12-1 for load conditions.

**TABLE 12-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57**

| **AC Characteristics** | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 100* | — | — | ns | VDD = 5.0V |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 32 | TDRT | Device Reset Timer Period | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 34 | Tioz | I/O Hi-impedance from $\overline{\text{MCLR}}$ Low | — | — | 100* | ns | |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 14-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED**

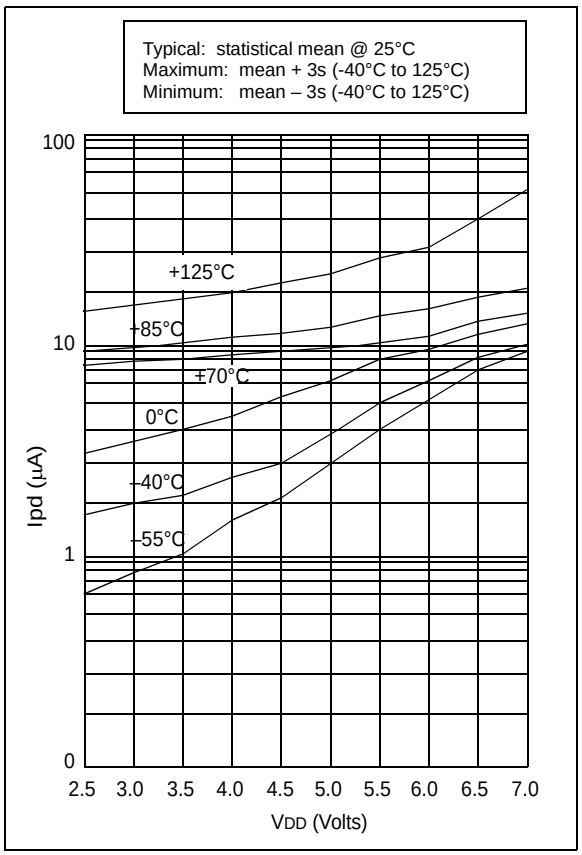



**FIGURE 14-7: TYPICAL IPD vs. VDD, WATCHDOG ENABLED**

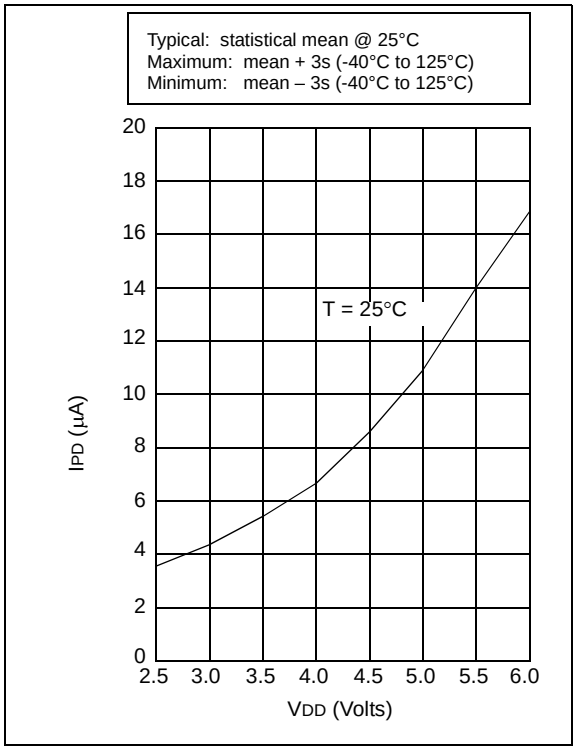
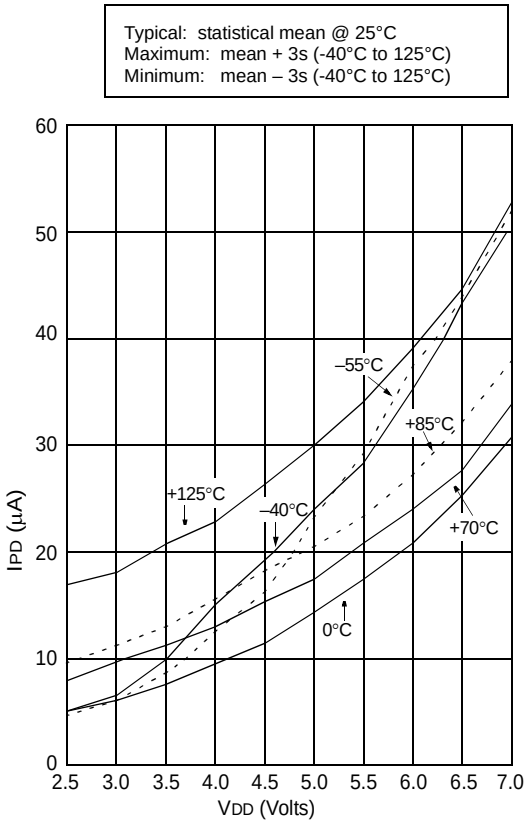



**FIGURE 14-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED**




IPD, with WDT enabled, has two components:
The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At –40°C, the latter dominates explaining the apparently anomalous behavior.

## 15.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended) PIC16LC54A-04E (Extended)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PIC16LC54A-04E** (Extended) | | | **Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
| **PIC16C54A-04E, 10E, 20E** (Extended) | | | **Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | IPD | **Power-down Current(2)** | | | | | |
| D020 | | PIC16LC54A | — | 2.5 | 15 | µA | VDD = 2.5V, WDT enabled, Extended |
| | | | — | 0.25 | 7.0 | µA | VDD = 2.5V, WDT disabled, Extended |
| D020A | | PIC16C54A | — | 5.0 | 22 | µA | VDD = 3.5V, WDT enabled |
| | | | — | 0.8 | 18* | µA | VDD = 3.5V, WDT disabled |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

**FIGURE 16-7: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS - VDD**

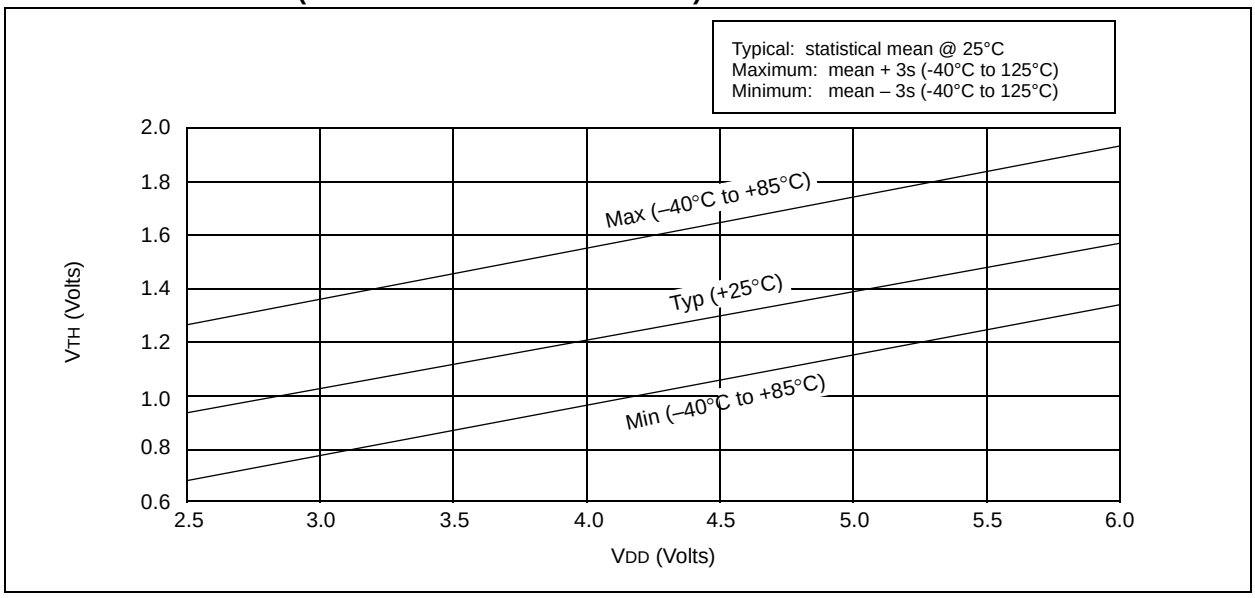



**FIGURE 16-8: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. VDD**

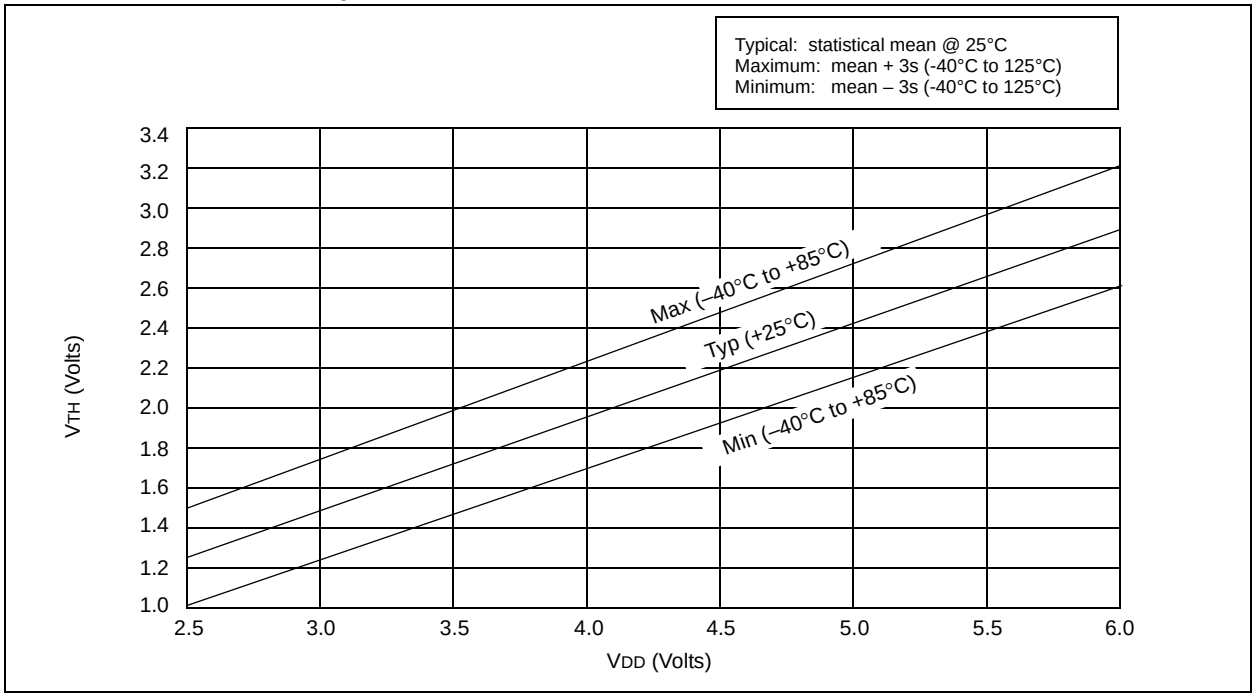


**FIGURE 16-18: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD**

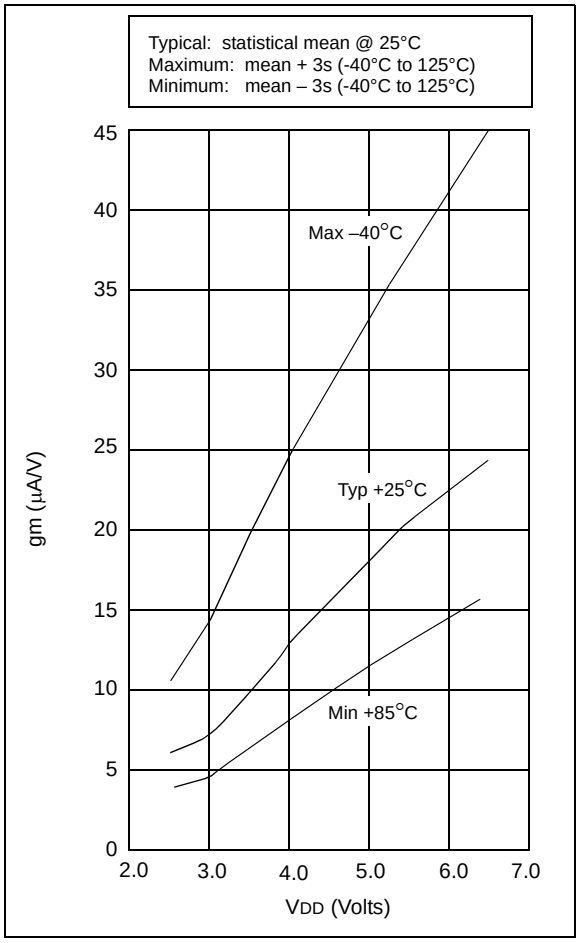



**FIGURE 16-19: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD**

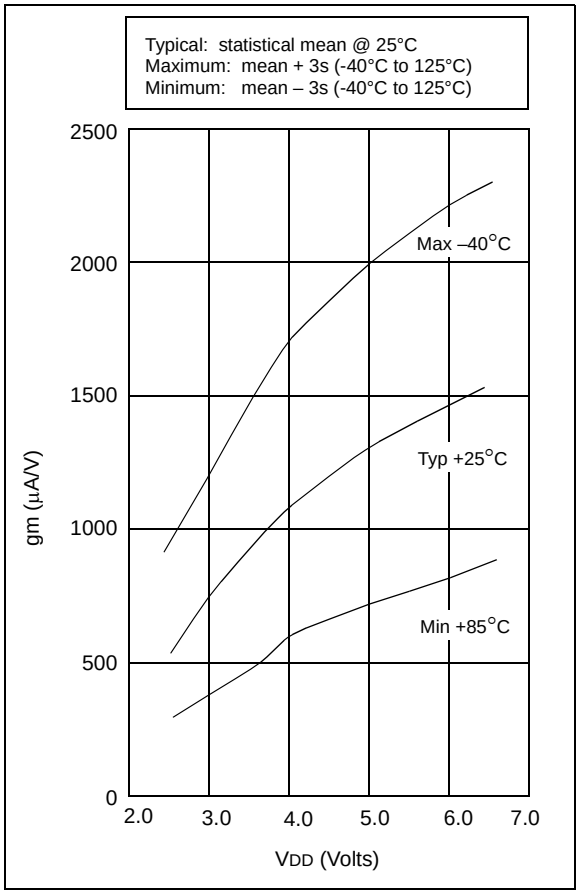


**FIGURE 16-20: PORTA, B AND C $I_{OH}$ vs. $V_{OH}$, $V_{DD}$ = 3V**

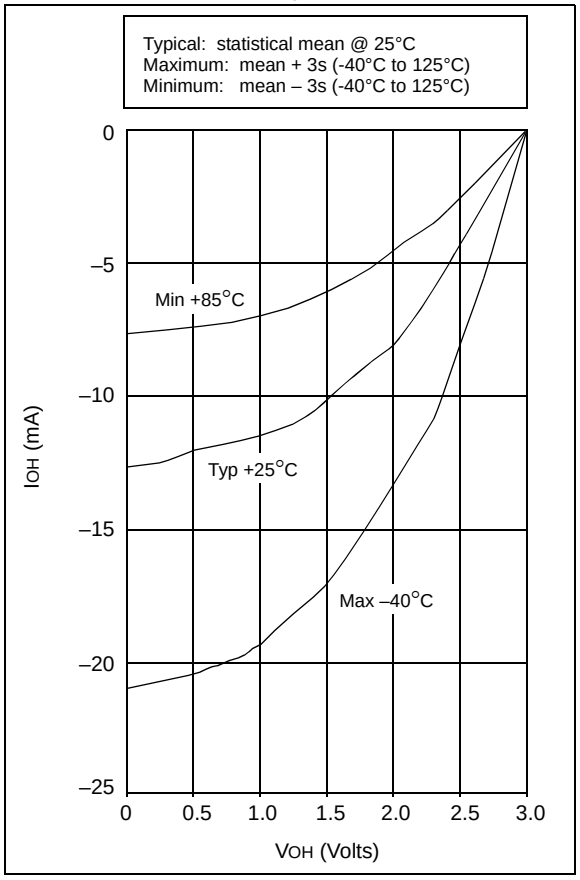
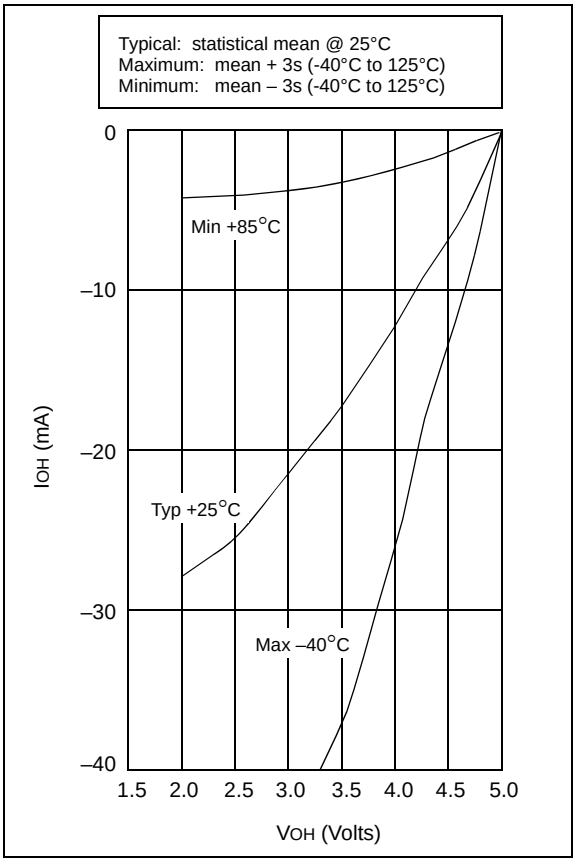



**FIGURE 16-21: PORTA, B AND C $I_{OH}$ vs. $V_{OH}$, $V_{DD}$ = 5V**



## 17.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial)
## PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial)
## PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial)
## PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PIC16LC5X**<br>**PIC16LCR5X**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **PIC16C5X**<br>**PIC16CR5X**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | IDD | **Supply Current(2,3)** | | | | | |
| D010 | | PIC16LC5X | — | 0.5 | 2.4 | mA | FOSC = 4.0 MHz, VDD = 5.5V, XT and RC modes |
| | | | — | 11 | 27 | µA | FOSC = 32 kHz, VDD = 2.5V, LP mode, Commercial |
| | | | — | 14 | 35 | µA | FOSC = 32 kHz, VDD = 2.5V, LP mode, Industrial |
| D010A | | PIC16C5X | — | 1.8 | 2.4 | mA | FOSC = 4 MHz, VDD = 5.5V, XT and RC modes |
| | | | — | 2.6 | 3.6* | mA | |
| | | | — | 4.5 | 16 | mA | FOSC = 10 MHz, VDD = 3.0V, HS mode |
| | | | — | 14 | 32 | µA | FOSC = 20 MHz, VDD = 5.5V, HS mode |
| | | | — | 17 | 40 | µA | FOSC = 32 kHz, VDD = 3.0V, LP mode, Commercial |
| | | | | | | | FOSC = 32 kHz, VDD = 3.0V, LP mode, Industrial |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

**FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF, 25°C**

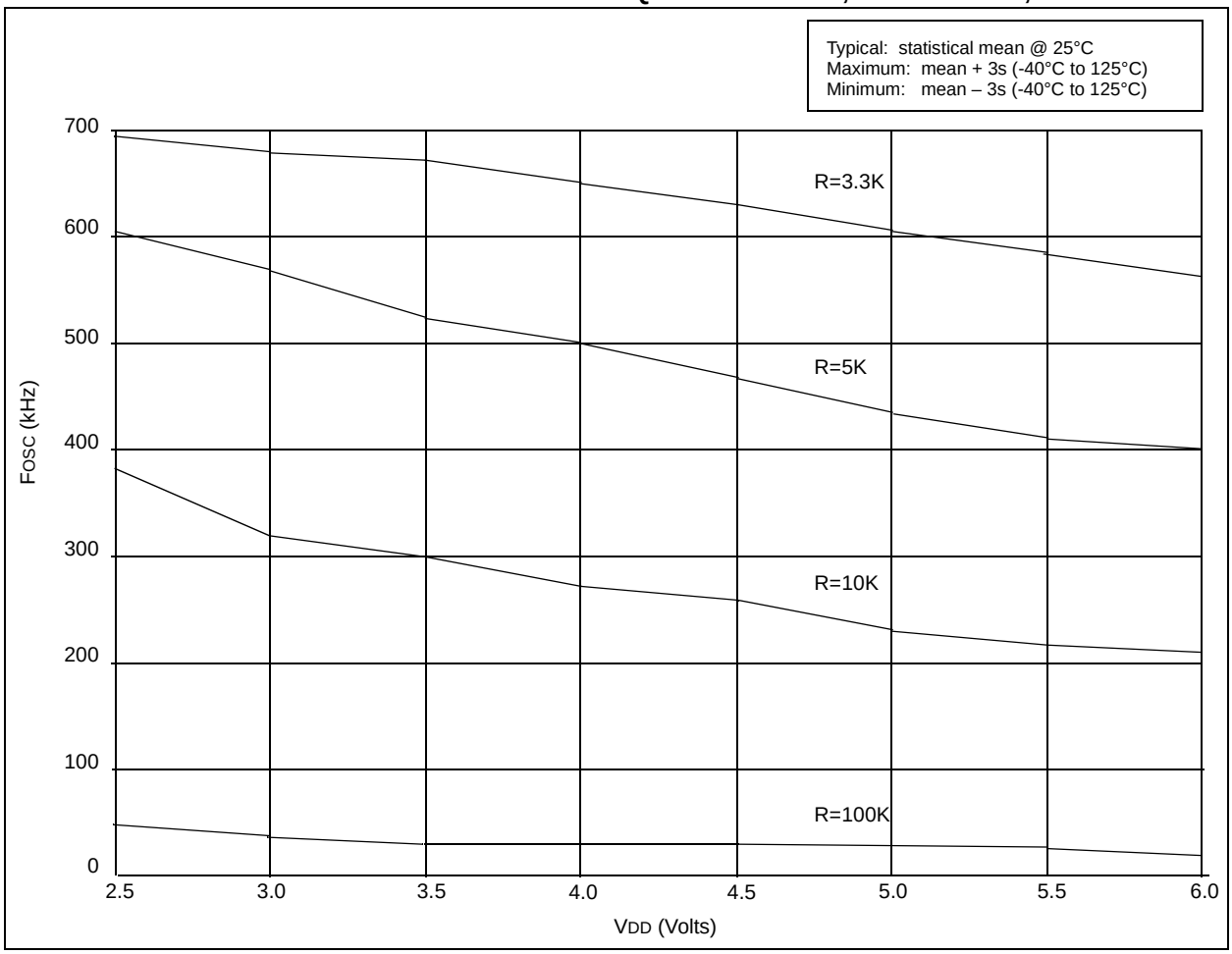
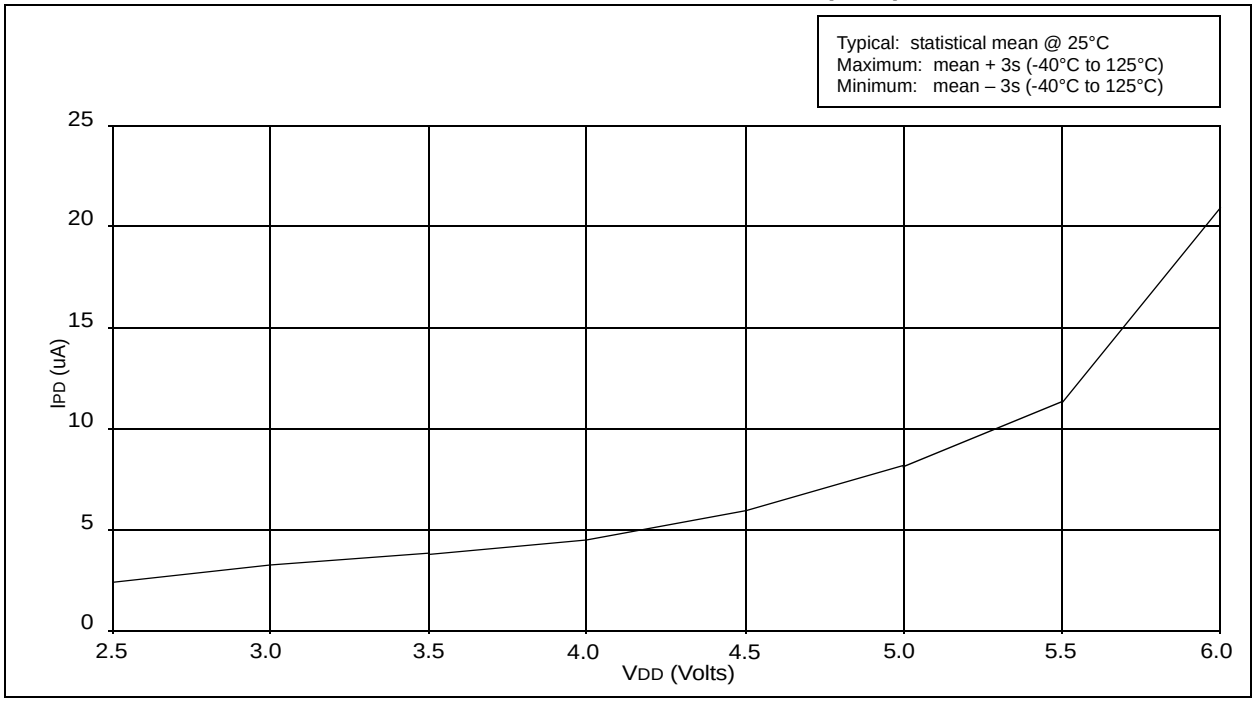



**FIGURE 18-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)**



## 19.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)(1)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D030 | VIL | **Input Low Voltage** | | | | | |
| | | I/O Ports | VSS | — | 0.8 | V | 4.5V <VDD ≤ 5.5V |
| | | MCLR (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | T0CKI (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | OSC1 | VSS | — | 0.2 VDD | V | HS, 20 MHz ≤ FOSC ≤ 40 MHz |
| D040 | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | 2.0 | — | VDD | V | 4.5V < VDD ≤ 5.5V |
| | | MCLR (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | T0CKI (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | OSC1 | 0.8 VDD | — | VDD | V | HS, 20 MHz ≤ FOSC ≤ 40 MHz |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current(2,3)** | | | | | **For VDD ≤ 5.5V:** |
| | | I/O ports | -1.0 | 0.5 | +1.0 | µA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| | | MCLR | -5.0 | — | +5.0 | µA | VPIN = VSS +0.25V |
| | | MCLR | — | 0.5 | +3.0 | µA | VPIN = VDD |
| | | T0CKI | -3.0 | 0.5 | +3.0 | µA | VSS ≤ VPIN ≤ VDD |
| | | OSC1 | -3.0 | 0.5 | — | µA | VSS ≤ VPIN ≤ VDD, HS |
| D080 | VOL | **Output Low Voltage** | | | | | |
| | | I/O ports | — | — | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| D090 | VOH | **Output High Voltage(3)** | | | | | |
| | | I/O ports | VDD - 0.7 | — | — | V | IOH = -5.4 mA, VDD = 4.5V |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected and HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 17.3.

**2:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**3:** Negative current is defined as coming out of the pin.

## 19.4 Timing Diagrams and Specifications

**FIGURE 19-3: EXTERNAL CLOCK TIMING - PIC16C5X-40**

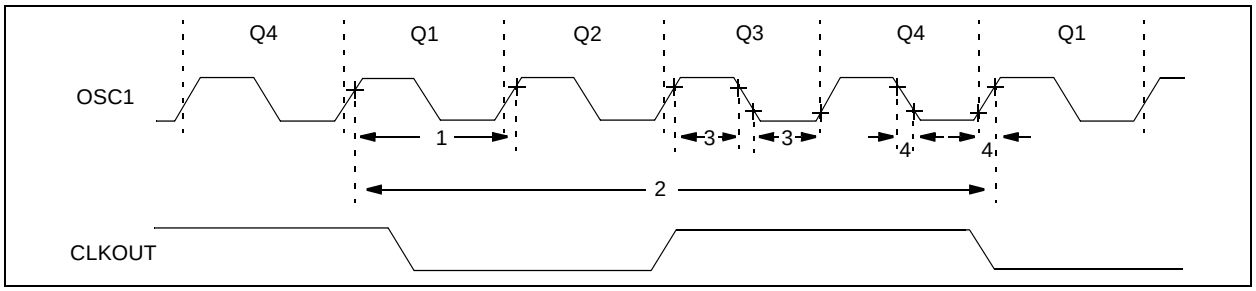



**TABLE 19-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X-40**

| AC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | FOSC | External CLKIN Frequency(1) | 20 | — | 40 | MHz | HS OSC mode |
| 1 | TOSC | External CLKIN Period(1) | 25 | — | — | ns | HS OSC mode |
| 2 | Tcy | Instruction Cycle Time(2) | — | 4/FOSC | — | — | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 6.0* | — | — | ns | HS oscillator |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 6.5* | ns | HS oscillator |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | - | XX | X | /XX | XXX |
|---|---|---|---|---|---|
| Device | | Frequency Range/OSC Type | Temperature Range | Package | Pattern |

| | | |
|---|---|---|
| Device | PIC16C54 | PIC16C54T(2) |
| | PIC16C54A | PIC16C54AT(2) |
| | PIC16CR54A | PIC16CR54AT(2) |
| | PIC16C54C | PIC16C54CT(2) |
| | PIC16CR54C | PIC16CR54CT(2) |
| | PIC16C55 | PIC16C55T(2) |
| | PIC16C55A | PIC16C55AT(2) |
| | PIC16C56 | PIC16C56T(2) |
| | PIC16C56A | PIC16C56AT(2) |
| | PIC16CR56A | PIC16CR56AT(2) |
| | PIC16C57 | PIC16C57T(2) |
| | PIC16C57C | PIC16C57CT(2) |
| | PIC16CR57C | PIC16CR57CT(2) |
| | PIC16C58B | PIC16C58BT(2) |
| | PIC16CR58B | PIC16CR58BT(2) |

| | | |
|---|---|---|
| Frequency Range/ Oscillator Type | RC | Resistor Capacitor |
| | LP | Low Power Crystal |
| | XT | Standard Crystal/Resonator |
| | HS | High Speed Crystal |
| | 02 | 200 KHz (LP) or 2 MHz (XT and RC) |
| | 04 | 200 KHz (LP) or 4 MHz (XT and RC) |
| | 10 | 10 MHz (HS only) |
| | 20 | 20 MHz (HS only) |
| | 40 | 40 MHz (HS only) |
| | b(4) | No oscillator type for JW packages(3) |

*RC/LP/XT/HS are for 16C54/55/56/57 devices only
-02 is available for 16LV54A only
-04/10/20 options are available for all other devices
-40 is available for 16C54C/55A/56A/57C/58B devices only

| | | | |
|---|---|---|---|
| Temperature Range | b(4) | = | 0°C to +70°C |
| | I | = | -40°C to +85°C |
| | E | = | -40°C to +125°C |

| | | | |
|---|---|---|---|
| Package | S | = | Die in Waffle Pack |
| | JW | = | 28-pin 600 mil/18-pin 300 mil windowed CERDIP(3) |
| | P | = | 28-pin 600 mil/18-pin 300 mil PDIP |
| | SO | = | 300 mil SOIC |
| | SS | = | 209 mil SSOP |
| | SP | = | 28-pin 300 mil Skinny PDIP |

*See Section 21 for additional package information.

| | |
|---|---|
| Pattern | QTP, SQTP, ROM code (factory specified) or Special Requirements. Blank for OTP and Windowed devices. |

**Examples:**

a) PIC16C55A - 04/P 301 = Commercial Temp., PDIP package, 4 MHz, standard VDD limits, QTP pattern #301

b) PIC16LC54C - 04I/SO Industrial Temp., SOIC package, 200 kHz, extended VDD limits

c) PIC16C57 - RC/SP = RC Oscillator, commercial temp, skinny PDIP package, 4 MHz, standard VDD limits

d) PIC16C58BT -40/SS 123 = commercial temp, SSOP package in tape and reel, 4 MHz, extended VDD limits, ROM pattern #123

**Note 1:** C = normal voltage range
LC = extended

**2:** T = in tape and reel - SOIC and SSOP packages only

**3:** JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirements of each oscillator type, including LC devices.

**4:** b = Blank

### Sales and Support

**Data Sheets**

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Worldwide Site (www.microchip.com)