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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57-lp-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

6.5.1 PAGING CONSIDERATIONS – PIC16C56/CR56, PIC16C57/CR57 AND PIC16C58/CR58

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS Register will not be updated. Therefore, the next GOTO, CALL or modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA<1:0>).

For example, a NOP at location 1FFh (page 0) increments the PC to 200h (page 1). A GOTO xxx at 200h will return the program to address xxh on page 0 (assuming that PA<1:0> are clear).

To prevent this, the page preselect bits must be updated under program control.

6.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the RESET vector).

The STATUS Register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a GOTO instruction at the RESET vector location will automatically cause the program to jump to page 0.

6.6 Stack

PIC16C5X devices have a 10-bit or 11-bit wide, two-level hardware push/pop stack.

A CALL instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W Register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the RETLW instruction, the PC is loaded with the Top of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC, therefore, paging is not an issue when returning from a subroutine.

6.7 Indirect Data Addressing; INDF and FSR Registers

The INDF Register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR Register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 6-1: INDIRECT ADDRESSING

- Register file 08 contains the value 10h
- Register file 09 contains the value 0Ah
- Load the value 08 into the FSR Register
- A read of the INDF Register will return the value of 10h
- Increment the value of the FSR Register by one (FSR = 09h)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF Register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 6-2.

EXAMPLE 6-2:

HOW TO CLEAR RAM USING INDIRECT ADDRESSING

	MOVLW	H'10'	;initialize pointer
	MOVWF	FSR	; to RAM
NEXT	CLRF	INDF	;clear INDF Register
	INCF	FSR,F	;inc pointer
	BTFSC	FSR,4	;all done?
	GOTO	NEXT	;NO, clear next
CONTINUE			
	:		;YES, continue

The FSR is either a 5-bit (PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56) or 7-bit (PIC16C57, PIC16CR57, PIC16CR58, PIC16CR58) wide register. It is used in conjunction with the INDF Register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56: These do not use banking. FSR<6:5> bits are unimplemented and read as '1's.

PIC16C57, **PIC16CR57**, **PIC16C58**, **PIC16CR58**: FSR<6:5> are the bank select bits and are used to select the bank to be addressed (00 = bank 0, 01 = bank 1, 10 = bank 2, 11 = bank 3).



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9.3 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

9.3.1 SLEEP

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the TO bit (STATUS<4>) is set, the PD bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the MCLR/VPP pin low.

For lowest current consumption while powered down, the T0CKI input should be at VDD or Vss and the $\overline{\text{MCLR}}/\text{VPP}$ pin must be at a logic high level ($\overline{\text{MCLR}}$ = VIH).

9.3.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

- 1. An external RESET input on MCLR/VPP pin.
- 2. A Watchdog Timer Time-out Reset (if WDT was enabled).

Both of these events cause a device RESET. The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits can be used to determine the cause of device RESET. The $\overline{\text{TO}}$ bit is cleared if a WDT timeout occurred (and caused wake-up). The $\overline{\text{PD}}$ bit, which is set on power-up, is cleared when SLEEP is invoked.

The WDT is cleared when the device wakes from SLEEP, regardless of the wake-up source.

9.4 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip does not recommend code pro-
	tecting windowed devices.

9.5 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

Note: Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

CALL	Subroutine Call			
Syntax:	[<i>label</i>] CALL k			
Operands:	$0 \leq k \leq 255$			
Operation:	(PC) + 1 \rightarrow TOS; k \rightarrow PC<7:0>; (STATUS<6:5>) \rightarrow PC<10:9>; 0 \rightarrow PC<8>			
Status Affected:	None			
Encoding:	1001 kkkk kkkk			
Description.	address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two- cycle instruction.			
Words:	1			
Cycles:	2			
Example:	HERE CALL THERE			
Before Instruction PC = address (HERE) After Instruction PC = address (THERE) TOS = address (HERE + 1)				

CLRE	Clear f
	Cical I

Syntax:	[label] CLRF f				
Operands:	$0 \le f \le 31$				
Operation:	$\begin{array}{l} 00h \rightarrow (f); \\ 1 \rightarrow Z \end{array}$				
Status Affected:	Z				
Encoding:	0000	011f	ffff		
Description:	The contents of register 'f' are cleared and the Z bit is set.				
Words:	1				
Cycles:	1				
Example:	CLRF	FLAG_RE	G		
Before Instruction FLAG_REG = 0x5A After Instruction					
$FLAG_REG = 0x00$					
Z = 1					

CLRW	Clear W
Syntax:	[label] CLRW
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow (W); \\ 1 \rightarrow Z \end{array}$
Status Affected:	Z
Encoding:	0000 0100 0000
Description:	The W register is cleared. Zero bit (Z) is set.
Words:	1
Cycles:	1
Example:	CLRW
VV = After Instruct W = Z =	= 0x5A tion = 0x00 = 1
CLRWDT	Clear Watchdog Timer
CLRWDT Syntax:	Clear Watchdog Timer
CLRWDT Syntax: Operands:	Clear Watchdog Timer [<i>label</i>] CLRWDT None
CLRWDT Syntax: Operands: Operation:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow \overline{TO};$ $1 \rightarrow \overline{PD}$
CLRWDT Syntax: Operands: Operation: Status Affected:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow \overline{TO};$ $1 \rightarrow \overline{PD}$ $\overline{TO}, \overline{PD}$
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding:	Clear Watchdog Timer[label]CLRWDTNone $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ \overline{TO}, PD 0000 0000
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description:	Clear Watchdog Timer[label] CLRWDTNone $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0100 The CLRWDT instruction resets theWDT. It also resets the prescaler, ifthe prescaler is assigned to theWDT and not Timer0. Status bitsTO and PD are set.
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description: Words:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0000 0100 The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set. 1
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	Clear Watchdog Timer [label] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0000 0100 The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set. 1 1
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0000 0100 The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set. 1 1 CLRWDT

After Instruction		
WDT counter	=	0x00
WDT prescaler	=	0
TO	=	1
PD	=	1

PIC16C5X

COMF	Complement f				
Syntax:	[<i>label</i>] COMF f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$				
Operation:	$(\overline{f}) \rightarrow (dest)$				
Status Affected:	Z				
Encoding:	0010 01df ffff				
Description:	The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example:	COMF REG1,0				
Before Instruction					
REG1	= 0x13				
After Instruct	ion				
REG1	= 0x13				
W	= 0xEC				

DECF	Decrement f				
Syntax:	[label] DECF f,	d		
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$				
Operation:	(f) – 1	\rightarrow (dest)			
Status Affected:	Z				
Encoding:	0000	11df	ffff		
Description:	Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example:	DECF	CNT,	1		
Before Instruc CNT Z After Instructi CNT Z	ction = = on = =	0x01 0 0x00 1			

DECFSZ	Decrement f, Skip if 0				
Syntax:	[label] DECFSZ f,d				
Operands:	$0 \le f \le 31$ $d \in [0,1]$				
Operation:	(f) $-1 \rightarrow d$; skip if result = 0				
Status Affected:	None				
Encoding:	0010 11df ffff				
Description:	The contents of register 'f' are dec- remented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, the next instruc- tion, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction				
Words:	1				
Cycles:	1(2)				
Example:	HERE DECFSZ CNT, 1 GOTO LOOP				
	CONTINUE • • •				
Before Instru	uction				
PC	= address (HERE)				
After Instruc	tion				
CNT	= CNT - 1;				
IT CN I	= 0,				
	= address (CONTINUE);				
	\neq U, - address (UFDF, 1)				
FU	= addless (HERE+1)				

12.5 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions
D030	Vil	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1 (Schmitt Trigger)	Vss Vss Vss Vss Vss Vss		0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD		Pin at hi-impedance PIC16C5X-RC only ⁽³⁾ PIC16C5X-XT, 10, HS, LP
D040	Vih	Input High Voltage I/O ports I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1 (Schmitt Trigger)	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD VDD	V V V V V V V	For all $V_{DD}^{(4)}$ 4.0V < $V_{DD} \le 5.5V^{(4)}$ $V_{DD} > 5.5 V$ PIC16C5X-RC only ⁽³⁾ PIC16C5X-XT, 10, HS, LP
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	—	—	V	
D060	Ιι∟	Input Leakage Current ^(1,2) I/O ports MCLR MCLR T0CKI OSC1	-1 -5 - -3 -3	0.5 — 0.5 0.5 0.5	+1 +5 +3 +3	μΑ μΑ μΑ μΑ μΑ	$\label{eq:statestar} \begin{array}{l} \mbox{For Vdd} \leq \mbox{5.5 V:} \\ \mbox{Vss} \leq \mbox{VplN} \leq \mbox{Vdd}, \\ \mbox{pin at hi-impedance} \\ \mbox{VplN} = \mbox{Vss} + \mbox{0.25V} \\ \mbox{VplN} = \mbox{Vdd} \\ \mbox{VplN} = \mbox{Vdd} \\ \mbox{Vss} \leq \mbox{VplN} \leq \mbox{Vdd} \\ \mbox{Vss} \leq \mbox{VplN} \leq \mbox{Vdd} \\ \mbox{Vss} \leq \mbox{VplN} \leq \mbox{Vdd} \\ \mbox{PlC16C5X-XT, 10, HS, LP} \end{array}$
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC
D090	Voн	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	VDD - 0.7 VDD - 0.7			V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, PIC16C5X-RC

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

AC Chara	cteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Symbol	Characteristic	Conditions					
1	Tosc	External CLKIN Period ⁽¹⁾	250			ns	XT OSC mode	
			100		—	ns	10 MHz mode	
			50		—	ns	HS OSC mode (Comm/Ind)	
			62.5		—	ns	HS OSC mode (Ext)	
			25		—	μS	LP OSC mode	
		Oscillator Period ⁽¹⁾	250	—	—	ns	RC OSC mode	
			250		10,000	ns	XT OSC mode	
			100		250	ns	10 MHz mode	
			50		250	ns	HS OSC mode (Comm/Ind)	
			62.5		250	ns	HS OSC mode (Ext)	
			25		—	μS	LP OSC mode	
2	Тсу	Instruction Cycle Time ⁽²⁾	—	4/Fosc	—	—		
3	TosL,	Clock in (OSC1) Low or High	85*	—	—	ns	XT oscillator	
	TosH	Time	20*	—	—	ns	HS oscillator	
			2.0*		—	μS	LP oscillator	
4	TosR,	Clock in (OSC1) Rise or Fall	—	_	25*	ns	XT oscillator	
	TosF	Time	—	—	25*	ns	HS oscillator	
			—	—	50*	ns	LP oscillator	

TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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13.3 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

DC CH	DC CHARACTERISTICS			$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$					
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions		
D030	VIL	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD	> > > > >	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes		
D040	Viн	Input High Voltage I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	2.0 0.6 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD		VDD VDD VDD VDD VDD VDD	V V V V V	VDD = 3.0V to 5.5V ⁽⁴⁾ Full VDD range ⁽⁴⁾ RC mode only ⁽³⁾ XT, HS and LP modes		
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	_	_	V			
D060	lı∟	Input Leakage Current ^(1,2) I/O ports	-1.0	_	+1.0	μA	For VDD \leq 5.5V: VSS \leq VPIN \leq VDD, pin at hi-impedance		
		MCLR MCLR TOCKI OSC1	-5.0 -3.0 -3.0	 0.5 0.5 0.5		μΑ μΑ μΑ μΑ	$VPIN = VSS + 0.25V$ $VPIN = VDD$ $VSS \le VPIN \le VDD$ $VSS \le VPIN \le VDD,$ $XT, HS and LP modes$		
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.5 0.5	V V	IOL = 10 mA, VDD = 6.0 V IOL = 1.9 mA, VDD = 6.0 V, RC mode only		
D090	Vон	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	Vdd – 0.5 Vdd – 0.5	_		V V	IOH = -4.0 mA, VDD = 6.0 V IOH = -0.8 mA, VDD = 6.0 V, RC mode only		

* These parameters are characterized but not tested.

- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- **Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
 - 2: Negative current is defined as coming out of the pin.
 - **3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
 - 4: The user may use the better of the two specifications.

13.4 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

DC CH	ARACTE	RISTICS	Standard O Operating Te	perating emperati	g Conditions ure -40°C	s (unless C ≤ TA ≤ +	ess otherwise specified) \leq +125°C for extended			
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions			
D030	VIL	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss		0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes			
D040	Vih	Input High Voltage I/O ports I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD VDD	V V V V V V V	For all VDD ⁽⁴⁾ 4.0V < VDD ≤ 5.5V ⁽⁴⁾ VDD > 5.5V RC mode only ⁽³⁾ XT, HS and LP modes			
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	—	—	V				
D060	lı∟	Input Leakage Current ^(1,2) I/O ports MCLR MCLR T0CKI OSC1	-1.0 -5.0 -3.0 -3.0	0.5 — 0.5 0.5 0.5	+1.0 	μΑ μΑ μΑ μΑ	For VDD \leq 5.5V: VSS \leq VPIN \leq VDD, pin at hi-impedance VPIN = VSS + 0.25V VPIN = VDD VSS \leq VPIN \leq VDD VSS \leq VPIN \leq VDD, XT, HS and LP modes			
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, RC mode only			
D090	Vон	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	VDD - 0.7 VDD - 0.7			V V	IOH = -5.4 mA, VDD = 4.5 V IOH = -1.0 mA, VDD = 4.5 V, RC mode only			

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.



TABLE 13-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR54A

AC Chara	acteristics	s otherwise sp ≤ +70°C for com ≤ +85°C for indu ≤ +125°C for ext	ecified) mercial strial ended			
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units
10	TosH2ckL	OSC1 [↑] to CLKOUT↓ ⁽¹⁾	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	_	40**	ns
15	TioV2ckH	Port in valid before CLKOUT ⁽¹⁾	0.25 TCY+30*	_	_	ns
16	TckH2iol	Port in hold after CLKOUT ⁽¹⁾	0*	_	-	ns
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽²⁾	—	_	100*	ns
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD		—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD		_	ns
20	TioR	Port output rise time ⁽²⁾		10	25**	ns
21	TioF	Port output fall time ⁽²⁾	_	10	25**	ns

* These parameters are characterized but not tested.

- ** These parameters are design targets and are not tested. No characterization data available at this time.
- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Please refer to Figure 13.1 for load conditions.

14.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.





TABLE 14-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Ave Fosc @	₃ge V, 25°C	
20 pF	3.3K	5 MHz	± 27%	
	5K	3.8 MHz	± 21%	
	10K	2.2 MHz	± 21%	
	100K	262 kHz	± 31%	
100 pF	3.3K	1.6 MHz	± 13%	
	5K	1.2 MHz	± 13%	
	10K	684 kHz	± 18%	
	100K	71 kHz	± 25%	
300 pF	3.3K	660 kHz	± 10%	
	5.0K	484 kHz	± 14%	
	10K	267 kHz	± 15%	
	100K	29 kHz	± 19%	

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviations from the average value for VDD = 5V.





15.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings ^(†)	
Ambient temperature under bias	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	–0.6V to (VDD + 0.6V)
Total power dissipation ⁽¹⁾	
Max. current out of Vss pin	150 mA
Max. current into VDD pin	100 mA
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, Iik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)	±20 mA
Max. output current sunk by any I/O pin	
Max. output current sourced by any I/O pin	
Max. output current sourced by a single I/O port (PORTA or B)	
Max. output current sunk by a single I/O port (PORTA or B)	50 mA
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH	$+ \sum \{(VDD-VOH) \times IOH\} + \sum (VOL \times IOL)$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



TABLE 15-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54A

		Standard Operating	g Conditions (ur	nless o	therw	ise spe	cified)				
	Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial										
	AC Characteristics $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial										
			–20°C ≤	$TA \leq +8$	85°C fc	or indus	trial - PIC16LV54A-02I				
			-40°C ≤	TA ≤ +1	25°C	for exte	nded				
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions				
40	Tt0H	T0CKI High Pulse Width									
		- No Prescaler	0.5 TCY + 20*	—	—	ns					
		- With Prescaler	10*			ns					
41	Tt0L	T0CKI Low Pulse Width									
		- No Prescaler	0.5 TCY + 20*	—	—	ns					
		- With Prescaler	10*			ns					
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> *	_	_	ns	Whichever is greater.				
			N				N = Prescale Value				
							(1, 2, 4,, 256)				

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Typical: statistical mean @ 25°C. Maximum: mean - 3 s (-40°C to 125°C) Minimum: mean

FIGURE 16-14: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 PF, 25°C)

FIGURE 16-15: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 PF, -40°C to +85°C)



17.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial)				e rating peratu	Condit re	ions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial			
PIC16C5X PIC16CR5X (Commercial, Industrial)				$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ} C \leq T A \leq +70^{\circ} C \mbox{ for commercial} \\ -40^{\circ} C \leq T A \leq +85^{\circ} C \mbox{ for industrial} \end{array}$					
Symbol	Characteristic/Device	Min Typ† Max Units				Conditions			
IDD	Supply Current ^(2,3)								
	PIC16LC5X		0.5	2.4	mA	Fosc = 4.0 MHz, VDD = 5.5V, XT and			
			11	27	μA	RC modes			
						FOSC = 32 kHz , VDD = 2.5V, LP mode,			
			14	35	μA	Commercial Ease $= 22 \text{ kHz}$ Vpp $= 2.5 \text{ // LP mode}$			
						Industrial			
	PIC16C5X		1.8	2.4	mA	Fosc = 4 MHz, VDD = 5.5V, XT and RC			
			2.6	3.6*	mA	modes			
		_	4.5	16	mA	FOSC = 10 MHz, VDD = 3.0V, HS mode			
		—	14	32	μA	FOSC = 20 MHz, VDD = 5.5V, HS mode			
			47	10	۸	FOSC = 32 KHZ, VDD = 3.0V, LP mode,			
			17	40	μA	Commercial Ease $= 32 \text{ kHz}$ Vpp $= 3.0 \text{ V}$ LP mode			
						Industrial			
	5X R5X hercial, Indi X SSX hercial, Indi Symbol	SX SX SSX Nercial, Industrial) Symbol Characteristic/Device IDD Supply Current ^(2,3) PIC16LC5X PIC16LC5X PIC16C5X PIC16C5X	Stand Opera R5X Stand iercial, Industrial) Stand Symbol Characteristic/Device Min IDD Supply Current ^(2,3) — PIC16LC5X — — — — — — — — — — — — — — — — — — — — — — — — — — — — — — — — — — — — — — — — —	Standard Operating Tem R5X Operating Tem iercial, Industrial) Standard Operating Tem Symbol Characteristic/Device Min Typ† IDD Supply Current ^(2,3) Min Typ† IDD Supply Current ^(2,3) 0.5 PIC16LC5X — 0.5 11 — 14 PIC16C5X — 1.8 2.6 — 14 14 — 14	Standard Operating Operating Temperature Operating Temperature Symbol Characteristic/Device Min Typ† Max IDD Supply Current ^(2,3) — 0.5 2.4 PIC16LC5X — 11 27 — 14 35 PIC16C5X — 1.8 2.4 — 14 35 — 14 35 — 14 32 — 14 32 — 14 32 — 14 32 — 14 32 — 14 32 — 14 32	Standard Operating Condit Operating TemperatureStandard Operating Condit Operating TemperatureStandard Operating Condit Operating TemperatureStandard Operating Condit Operating TemperatureSymbolCharacteristic/DeviceMinTyptMaxUnitsIDDSupply Current (2,3)IDDSupply Current PIC16LC5X0.52.4mAIDDPIC16LC5X—0.52.4mAIDDPIC16C5X—1.82.4mAIDDPIC16C5X—1.82.4mAIDDPIC16C5X—1.82.4mAIDDPIC16C5X—1.82.4mAIDDPIC16C5X—1.82.4mAIDDPIC16C5X—1.82.4mAIDDPIC16C5X—1.82.4mAIDDIDD1.82.4mAIDDIDDIDDIDD			

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .



FIGURE 17-8: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X, PIC16CR5X

TABLE 17-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X, PIC16CR5X

AC Charac	teristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions		
30	TmcL	MCLR Pulse Width (low)	1000*		—	ns	VDD = 5.0V		
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)		
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)		
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns			

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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18-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	р		.050			1.27	
Overall Height	Α	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	С	.009	.011	.012	0.23	0.27	0.30
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013 Drawing No. C04-051

28-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging







	Units	INCHES*		MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.050			1.27	
Overall Height	А	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	Е	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59
Overall Length	D	.695	.704	.712	17.65	17.87	18.08
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle Top	¢	0	4	8	0	4	8
Lead Thickness	С	.009	.011	.013	0.23	0.28	0.33
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013 Drawing No. C04-052

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	<u>xx x</u>	<u>/xx</u>	<u>xxx</u>	Exam	ples:
Device	Frequency Temper Range/OSC Rang Type	ature Package ge	Pattern	a) P P Q	IC16C55A - 04/P 301 = Commercial Temp., DIP package, 4 MHz, standard VDD limits, TP pattern #301
Device	PIC16C54 PIC1 PIC16C54A PIC1 PIC16C54A PIC1 PIC16C54C PIC1 PIC16C55C PIC1 PIC16C55A PIC1 PIC16C55A PIC1 PIC16C56A PIC1 PIC16C56A PIC1 PIC16C56A PIC1 PIC16C57C PIC1 PIC16C57C PIC1 PIC16C57C PIC1 PIC16C58B PIC1 PIC16C768B PIC1 PIC16C768B PIC1	6C54T ⁽²⁾ 6C54AT ⁽²⁾ 6CR54AT ⁽²⁾ 6CR54CT ⁽²⁾ 6C554CT ⁽²⁾ 6C55T ⁽²⁾ 6C55AT ⁽²⁾ 6C56AT ⁽²⁾ 6C56AT ⁽²⁾ 6C57CT ⁽²⁾ 6C57CT ⁽²⁾ 6C57CT ⁽²⁾ 6C757CT ⁽²⁾ 6C757CT ⁽²⁾ 6C757CT ⁽²⁾ 6C757CT ⁽²⁾ 6C757CT ⁽²⁾		c) P ci da d) P te M #	 1: C = normal voltage range LC = extended 123 1: C = normal voltage range LC = extended 2: T = in tape and reel - SOIC and SSOP packages only
Oscillator Type	 RC Resistor Capacitor LP Low Power Crystal XT Standard Crystal/Reso High Speed Crystal 200 KHz (LP) or 2 MHz 00 KHz (LP) or 4 MHz 10 MHz (HS only) 20 0MHz (HS only) 40 40 MHz (HS only) 40 40 MHz (HS only) b⁽⁴⁾ No oscillator type for J¹ *RC/LP/XT/HS are for 16C5 -02 is available for 16LV54A -04/10/20 options are availa -40 is available for 16C54C/ 	nator z (XT and RC) z (XT and RC) W packages ⁽³⁾ 4/55/56/57 devices of a only ble for all other device 55A/56A/57C/58B dev	nly es vices only		 3: JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirements of each oscillator type, including LC devices. 4: b = Blank
Temperature Range	$b^{(4)} = 0^{\circ}C \text{ to } +70^{\circ}C$ $I = -40^{\circ}C \text{ to } +85^{\circ}C$ $E = -40^{\circ}C \text{ to } +125^{\circ}C$	C C ℃			
Package	S = Die in Waffle Pac JW = 28-pin 600 mil/18 DIP(3) P = 28-pin 600 mil/18 SO = 300 mil SOIC SS SS = 209 mil SSOP SP SP = 28-pin 300 mil Sł *See Section 21 for addition *	:k 8-pin 300 mil windowe 8-pin 300 mil PDIP kinny PDIP al package informatic	d CER-		
Pattern	QTP, SQTP, ROM code (fac Requirements. Blank for OT	tory specified) or Spe P and Windowed dev	cial rices.		

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office

2. The Microchip Worldwide Site (www.microchip.com)