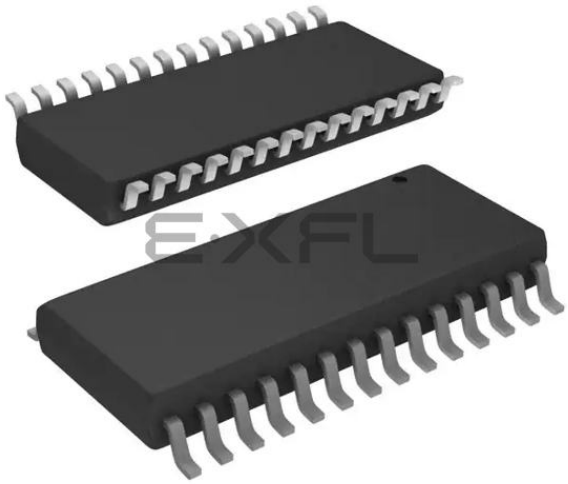

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57-lp-so

TABLE 3-1: PINOUT DESCRIPTION - PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58, PIC16CR58

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	DIP	SOIC	SSOP			
RA0	17	17	19	I/O	TTL	Bi-directional I/O port
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RB0	6	6	7	I/O	TTL	Bi-directional I/O port
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	
RB5	11	11	12	I/O	TTL	
RB6	12	12	13	I/O	TTL	
RB7	13	13	14	I/O	TTL	
T0CKI	3	3	3	I	ST	Clock input to Timer0. Must be tied to V_{SS} or V_{DD}, if not in use, to reduce current consumption.
$\overline{MCLR}/V_{PP}$	4	4	4	I	ST	Master clear (RESET) input/programming voltage input. This pin is an active low RESET to the device. Voltage on the $\overline{MCLR}/V_{PP}$ pin must not exceed V_{DD} to avoid unintended entering of Programming mode.
OSC1/CLKIN	16	16	18	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
V_{DD}	14	14	15,16	P	—	Positive supply for logic and I/O pins.
V_{SS}	5	5	5,6	P	—	Ground reference for logic and I/O pins.

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

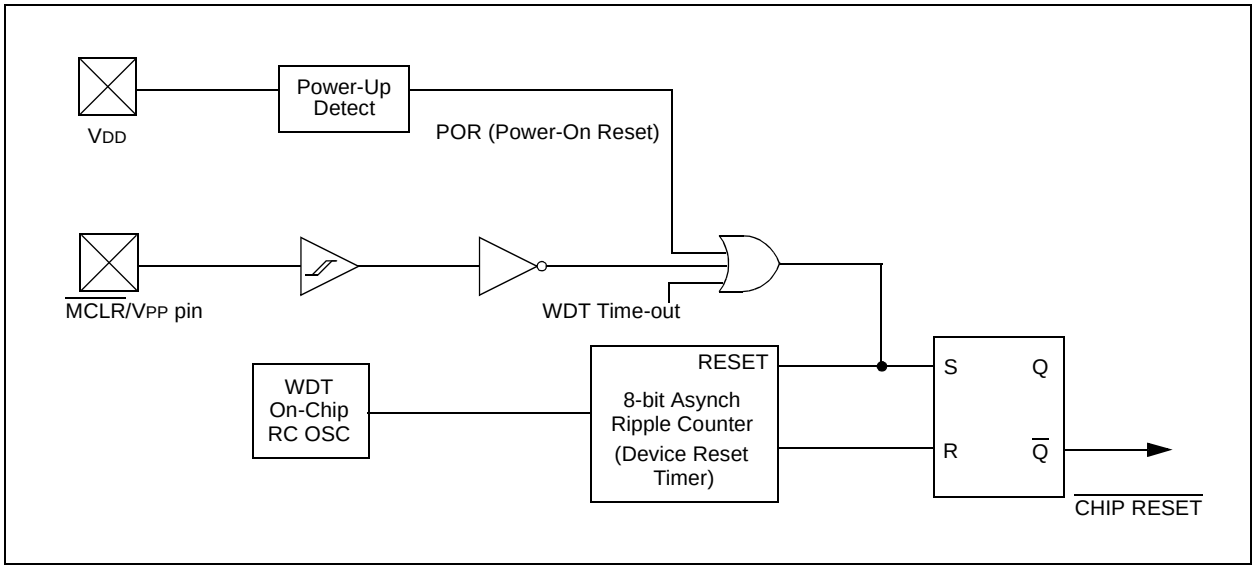
TABLE 5-3: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-On Reset	$\overline{MCLR}$ or WDT Reset
W	N/A	xxxx xxxx	uuuu uuuu
TRIS	N/A	1111 1111	1111 1111
OPTION	N/A	--11 1111	--11 1111
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000q quuu
FSR(1)	04h	1xxx xxxx	1uuu uuuu
PORTA	05h	---- xxxx	---- uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu
PORTC(2)	07h	xxxx xxxx	uuuu uuuu
General Purpose Register Files	07-7Fh	xxxx xxxx	uuuu uuuu

Legend: x = unknown u = unchanged - = unimplemented, read as '0'
q = see tables in Table 5-1 for possible values.

Note 1: These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for $\overline{MCLR}$ and WDT Reset, the value is 111u uuuu.
2: General purpose register file on PIC16C54/CR54/C56/CR56/C58/CR58.

FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



7.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., MOVF PORTB,W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

7.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used (RA<3:0>). Bits 7-4 are unimplemented and read as '0's.

7.2 PORTB

PORTB is an 8-bit I/O Register (PORTB<7:0>).

7.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58 and PIC16CR58.

7.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the TRIS f instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

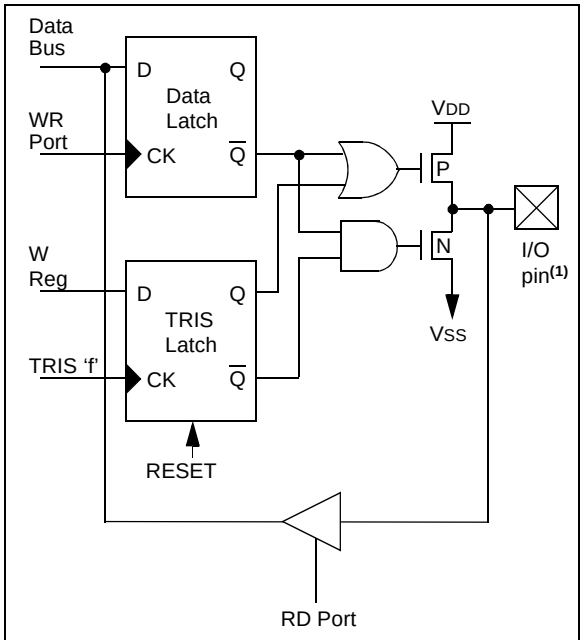
Note:	A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

7.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 7-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

FIGURE 7-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



Note 1: I/O pins have protection diodes to VDD and VSS.

TABLE 7-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	TRIS	I/O Control Registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'

7.6 I/O Programming Considerations

7.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 7-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

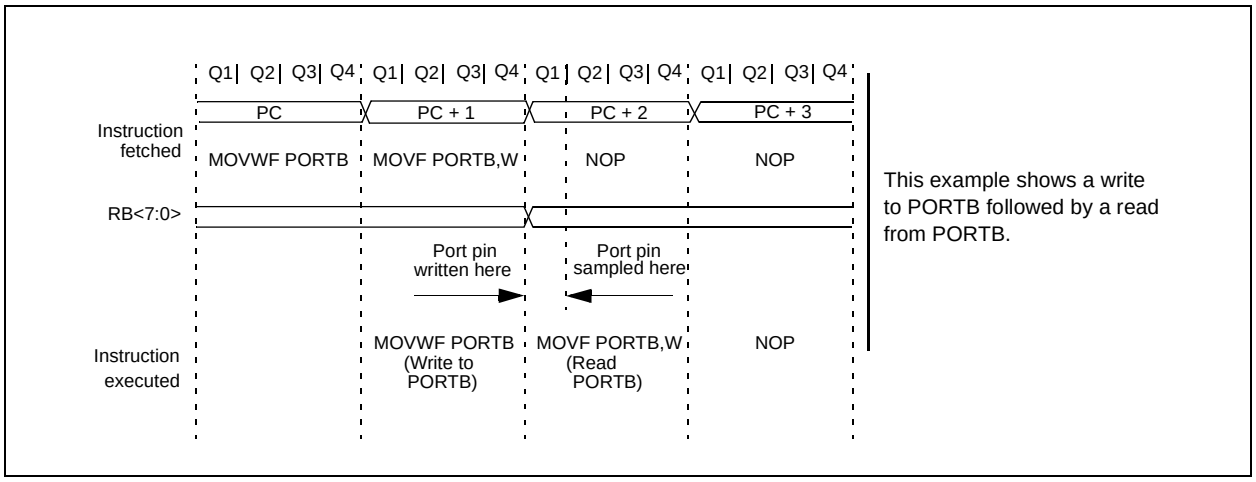
EXAMPLE 7-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                    PORT latch  PORT pins
;                    ----------  ----------
  BCF   PORTB, 7    ;01pp pppp   11pp pppp
  BCF   PORTB, 6    ;10pp pppp   11pp pppp
  MOVLW H'3F'        ;
  TRIS  PORTB       ;10pp pppp   10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

7.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 7-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 7-2: SUCCESSIVE I/O OPERATION



12.3 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)			Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic/Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**					
		PIC16C5X-RCE	3.25	—	6.0	V	
		PIC16C5X-XTE	3.25	—	6.0	V	
		PIC16C5X-10E	4.5	—	5.5	V	
		PIC16C5X-HSE	4.5	—	5.5	V	
		PIC16C5X-LPE	2.5	—	6.0	V	
D002	VDR	**RAM Data Retention Voltage(1)**	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	**Supply Current(2)**					
		PIC16C5X-RCE(3)	—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
		PIC16C5X-XTE	—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
		PIC16C5X-10E	—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
		PIC16C5X-HSE	—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
		PIC16C5X-HSE	—	9.0	20	mA	FOSC = 16 MHz, VDD = 5.5V
		PIC16C5X-LPE	—	19	55	μA	FOSC = 32 kHz, VDD = 3.25V, WDT disabled
D020	IPD	**Power-down Current(2)**	—	5.0	22	μA	VDD = 3.25V, WDT enabled
			—	0.8	18	μA	VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

12.5 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D030	VIL	**Input Low Voltage**					
		I/O ports	Vss	—	0.15 VDD	V	Pin at hi-impedance
		MCLR (Schmitt Trigger)	Vss	—	0.15 VDD	V	
		T0CKI (Schmitt Trigger)	Vss	—	0.15 VDD	V	
		OSC1 (Schmitt Trigger)	Vss	—	0.15 VDD	V	PIC16C5X-RC only(3)
		OSC1 (Schmitt Trigger)	Vss	—	0.3 VDD	V	PIC16C5X-XT, 10, HS, LP
D040	VIH	**Input High Voltage**					
		I/O ports	0.45 VDD	—	VDD	V	For all VDD(4)
		I/O ports	2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(4)
		I/O ports	0.36 VDD	—	VDD	V	VDD > 5.5 V
		MCLR (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		T0CKI (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		OSC1 (Schmitt Trigger)	0.85 VDD	—	VDD	V	PIC16C5X-RC only(3)
		OSC1 (Schmitt Trigger)	0.7 VDD	—	VDD	V	PIC16C5X-XT, 10, HS, LP
D050	VHYS	**Hysteresis of Schmitt Trigger inputs**	0.15 VDD*	—	—	V	
D060	IIL	**Input Leakage Current (1,2)**					**For VDD ≤ 5.5 V:**
		I/O ports	–1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
		MCLR	–5	—	—	µA	VPIN = VSS + 0.25V
		MCLR	—	0.5	+5	µA	VPIN = VDD
		T0CKI	–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
		OSC1	–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, 10, HS, LP
D080	VOL	**Output Low Voltage**					
		I/O ports	—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
		OSC2/CLKOUT	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC
D090	VOH	**Output High Voltage(2)**					
		I/O ports	VDD – 0.7	—	—	V	IOH = –5.4 mA, VDD = 4.5V
		OSC2/CLKOUT	VDD – 0.7	—	—	V	IOH = –1.0 mA, VDD = 4.5V, PIC16C5X-RC

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the $\overline{\text{MCLR}}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

TABLE 14-2: INPUT CAPACITANCE FOR PIC16C54/56

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{MCLR}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

TABLE 14-3: INPUT CAPACITANCE FOR PIC16C55/57

Pin	Typical Capacitance (pF)	
	28L PDIP (600 mil)	28L SOIC
RA port	5.2	4.8
RB port	5.6	4.7
RC port	5.0	4.1
$\overline{MCLR}$	17.0	17.0
OSC1	6.6	3.5
OSC2/CLKOUT	4.6	3.5
T0CKI	4.5	3.5

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

15.3 DC Characteristics: PIC16LV54A-02 (Commercial) PIC16LV54A-02I (Industrial)

PIC16LV54A-02 PIC16LV54A-02I (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –20°C ≤ TA ≤ +85°C for industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage** RC and XT modes	2.0	—	3.8	V	
D002	VDR	**RAM Data Retention Voltage(1)**	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	**Supply Current(2)** RC(3) and XT modes LP mode, Commercial LP mode, Industrial	 — — —	 0.5 11 14	 — 27 35	 mA µA µA	 FOSC = 2.0 MHz, VDD = 3.0V FOSC = 32 kHz, VDD = 2.5V WDT disabled FOSC = 32 kHz, VDD = 2.5V WDT disabled
D020	IPD	**Power-down Current(2,4)** Commercial Commercial Industrial Industrial	 — — — —	 2.5 0.25 3.5 0.3	 12 4.0 14 5.0	 µA µA µA µA	 VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

4: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection on wake-up from SLEEP mode or during initial power-up.

15.4 DC Characteristics: PIC16C54A-04, 10, 20, PIC16LC54A-04, PIC16LV54A-02 (Commercial) PIC16C54A-04I, 10I, 20I, PIC16LC54A-04I, PIC16LV54A-02I (Industrial) PIC16C54A-04E, 10E, 20E, PIC16LC54A-04E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial –20°C ≤ TA ≤ +85°C for industrial-PIC16LV54A-02I –40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D030	VIL	**Input Low Voltage**					
		I/O ports	VSS	—	0.2 VDD	V	Pin at hi-impedance
		MCLR (Schmitt Trigger)	VSS	—	0.15 VDD	V	
		T0CKI (Schmitt Trigger)	VSS	—	0.15 VDD	V	
		OSC1 (Schmitt Trigger)	VSS	—	0.15 VDD	V	RC mode only(3)
		OSC1	VSS	—	0.3 VDD		XT, HS and LP modes
D040	VIH	**Input High Voltage**					
		I/O ports	0.2 VDD + 1	—	VDD	V	For all VDD(4)
		I/O ports	2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(4)
		MCLR (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		T0CKI (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		OSC1 (Schmitt Trigger)	0.85 VDD	—	VDD	V	RC mode only(3)
		OSC1	0.7 VDD	—	VDD	V	XT, HS and LP modes
D050	VHYS	**Hysteresis of Schmitt Trigger inputs**	0.15 VDD*	—	—	V	
D060	IIL	**Input Leakage Current(1,2)**					**For VDD ≤ 5.5V:**
		I/O ports	-1.0	0.5	+1.0	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
		MCLR	-5.0	—	+5.0	µA	VPIN = VSS +0.25V
		MCLR	—	0.5	+3.0	µA	VPIN = VDD
		T0CKI	-3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
		OSC1	-3.0	0.5	—	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP modes
D080	VOL	**Output Low Voltage**					
		I/O ports	—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
		OSC2/CLKOUT	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC mode only
	VOH	**Output High Voltage(2)**					
		I/O ports	VDD - 0.7	—	—	V	IOH = -5.4 mA, VDD = 4.5V
		OSC2/CLKOUT	VDD - 0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, RC mode only

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

NOTES:

17.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial)
PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial)
PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial)
PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X **PIC16LCR5X** (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
PIC16C5X **PIC16CR5X** (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Symbol**	**Characteristic/Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**					
D001		PIC16LC5X	2.5 2.7 2.5	— — —	5.5 5.5 5.5	V V V	–40°C ≤ TA ≤ + 85°C, 16LCR5X –40°C ≤ TA ≤ 0°C, 16LC5X 0°C ≤ TA ≤ + 85°C 16LC5X
D001A		PIC16C5X	 3.0 4.5	 — —	 5.5 5.5	 V V	RC, XT, LP and HS mode from 0 - 10 MHz from 10 - 20 MHz
D002	VDR	**RAM Data Retention Voltage(1)**	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

17.4 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T	
F Frequency	T Time

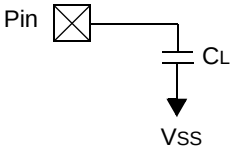
Lowercase letters (pp) and their meanings:

pp	
2 to	mc $\overline{\text{MCLR}}$
ck CLKOUT	osc oscillator
cy cycle time	os OSC1
drt device reset timer	t0 T0CKI
io I/O port	wdt watchdog timer

Uppercase letters and their meanings:

S	
F Fall	P Period
H High	R Rise
I Invalid (Hi-impedance)	V Valid
L Low	Z Hi-impedance

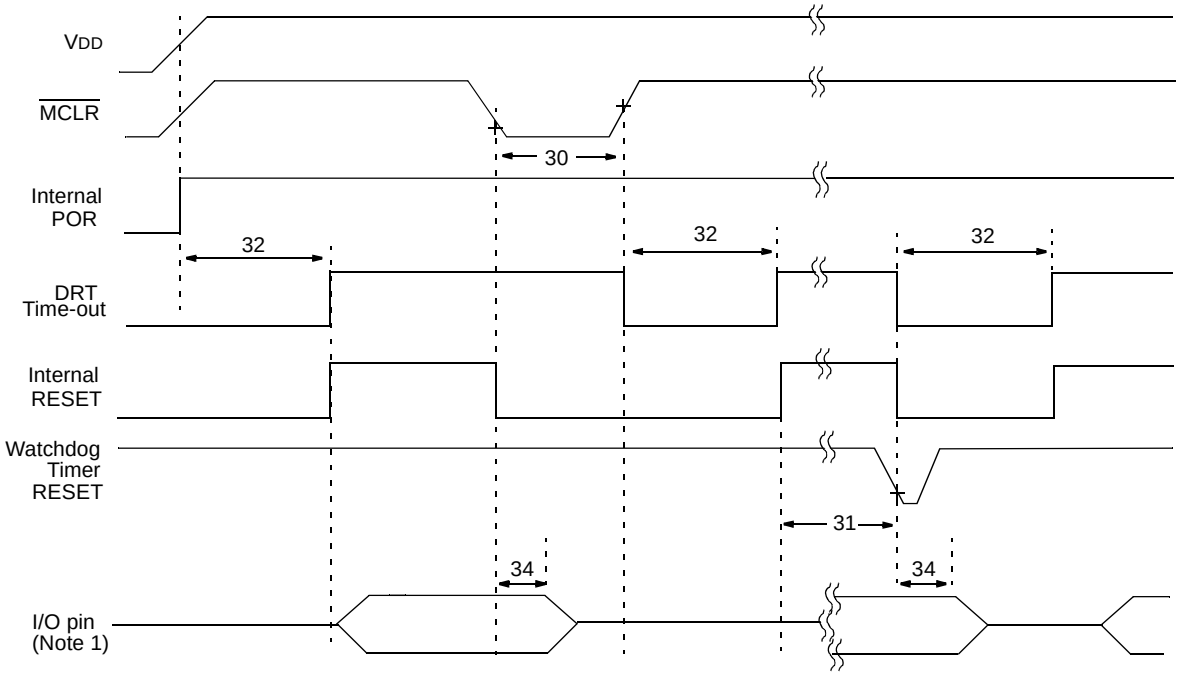
FIGURE 17-5: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B-04, 20



C_L = 50 pF for all pins and OSC2 for RC mode

0 -15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

FIGURE 17-8: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X, PIC16CR5X



Note 1: Please refer to Figure 17-5 for load conditions.

TABLE 17-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X, PIC16CR5X

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial –40°C ≤ TA ≤ +125°C for extended						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	1000*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	100*	300*	1000*	ns	

* These parameters are characterized but not tested.

† Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 18-12: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, 25°C)

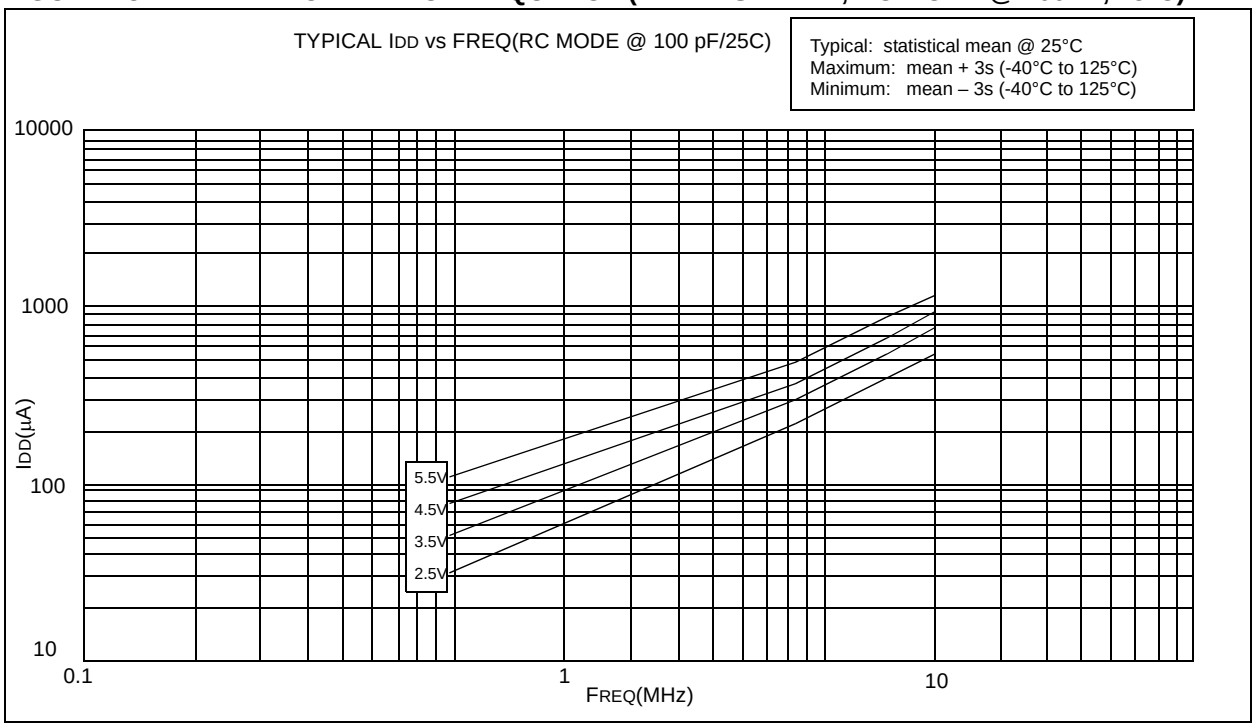
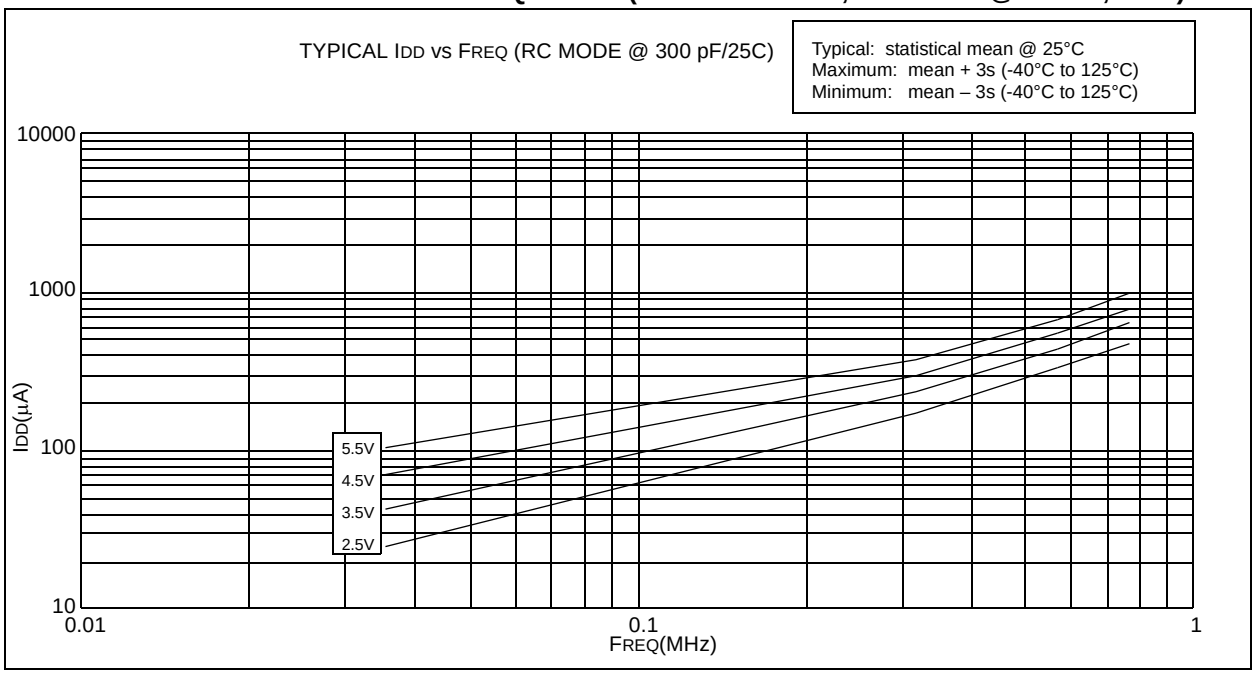


FIGURE 18-13: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, 25°C)



19.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)(1)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D030	VIL	**Input Low Voltage**					
		I/O Ports	VSS	—	0.8	V	4.5V <VDD ≤ 5.5V
		MCLR (Schmitt Trigger)	VSS	—	0.15 VDD	V	
		T0CKI (Schmitt Trigger)	VSS	—	0.15 VDD	V	
		OSC1	VSS	—	0.2 VDD	V	HS, 20 MHz ≤ FOSC ≤ 40 MHz
D040	VIH	**Input High Voltage**					
		I/O ports	2.0	—	VDD	V	4.5V < VDD ≤ 5.5V
		MCLR (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		T0CKI (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		OSC1	0.8 VDD	—	VDD	V	HS, 20 MHz ≤ FOSC ≤ 40 MHz
D050	VHYS	**Hysteresis of Schmitt Trigger inputs**	0.15 VDD*	—	—	V	
D060	IIL	**Input Leakage Current(2,3)**					**For VDD ≤ 5.5V:**
		I/O ports	-1.0	0.5	+1.0	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
		MCLR	-5.0	—	+5.0	µA	VPIN = VSS +0.25V
		MCLR	—	0.5	+3.0	µA	VPIN = VDD
		T0CKI	-3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
		OSC1	-3.0	0.5	—	µA	VSS ≤ VPIN ≤ VDD, HS
D080	VOL	**Output Low Voltage**					
		I/O ports	—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
D090	VOH	**Output High Voltage(3)**					
		I/O ports	VDD - 0.7	—	—	V	IOH = -5.4 mA, VDD = 4.5V

* These parameters are characterized but not tested.

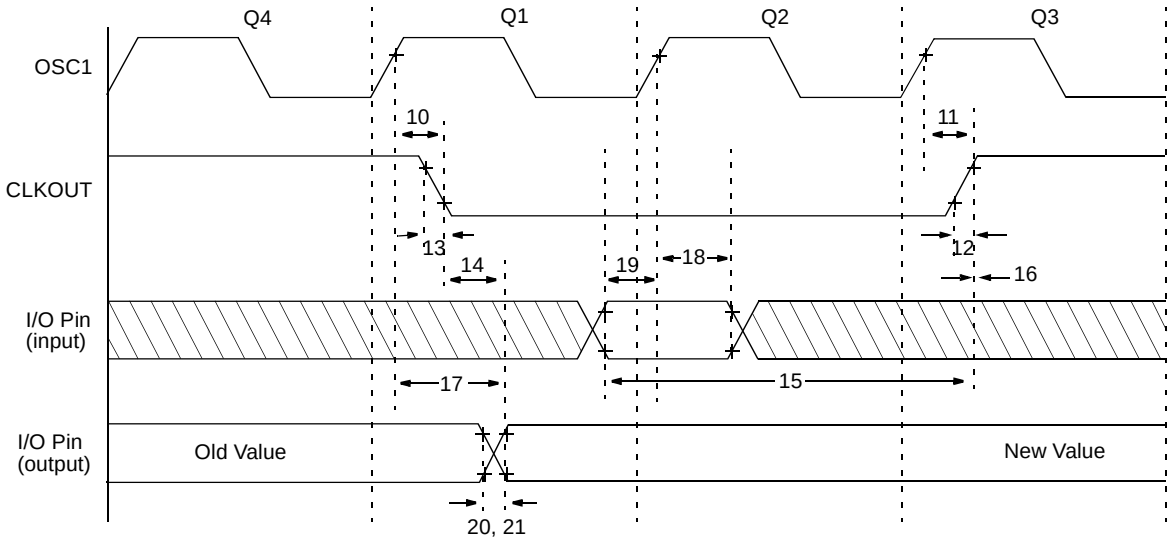
† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected and HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 17.3.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

FIGURE 19-4: CLKOUT AND I/O TIMING - PIC16C5X-40



Note: Refer to Figure 19-2 for load conditions.

TABLE 19-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X-40

AC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓ **(1,2)**	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ **(1,2)**	—	15	30**	ns
12	TckR	CLKOUT rise time **(1,2)**	—	5.0	15**	ns
13	TckF	CLKOUT fall time **(1,2)**	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid **(1,2)**	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ **(1,2)**	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ **(1,2)**	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid **(2)**	—	—	100	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time **(2)**	—	10	25**	ns
21	TioF	Port output fall time **(2)**	—	10	25**	ns

* These parameters are characterized but not tested.

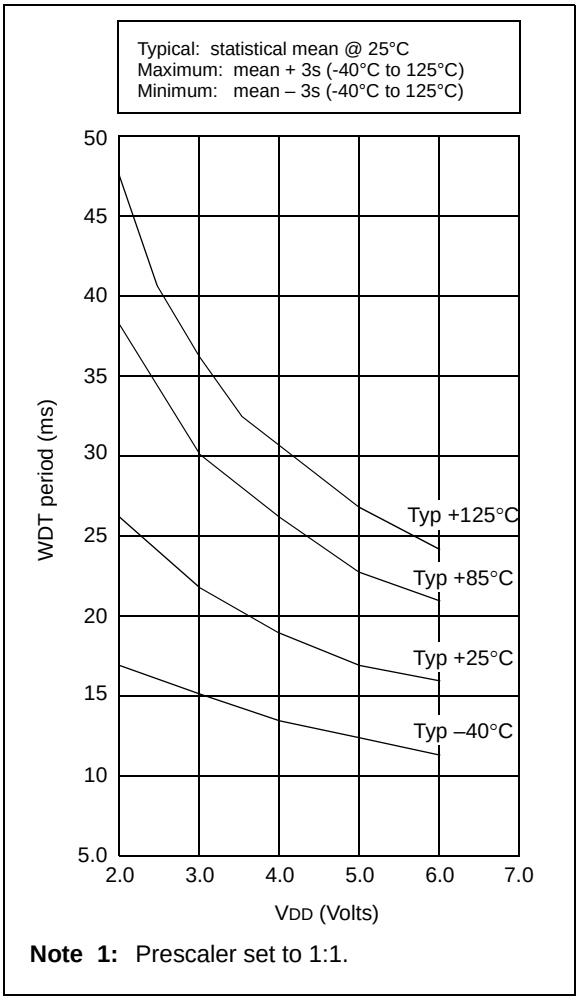
** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

2: Refer to Figure 19-2 for load conditions.

FIGURE 20-7: WDT TIMER TIME-OUT PERIOD vs. V_{DD}(1)



Note 1: Prescaler set to 1:1.

FIGURE 20-8: I_{OH} vs. V_{OH}, V_{DD} = 5 V

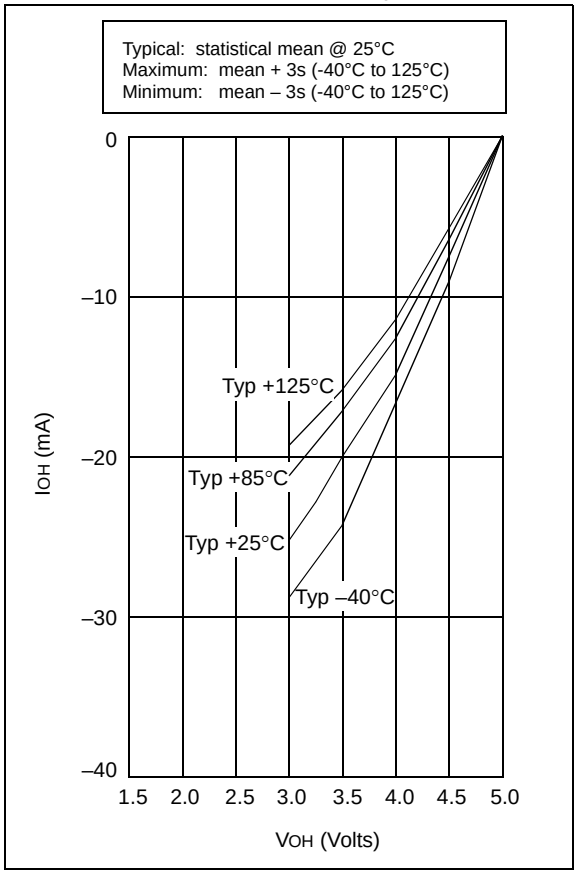


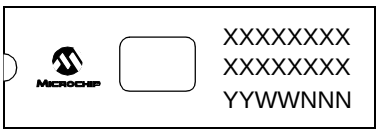
TABLE 20-1: INPUT CAPACITANCE

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{MCLR}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

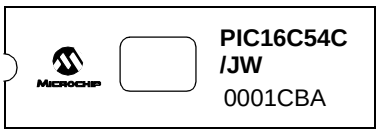
All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

Package Marking Information (Cont'd)

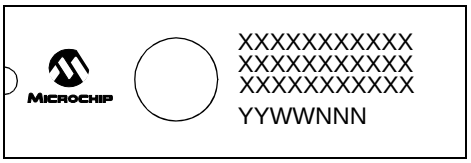
18-Lead CERDIP Windowed



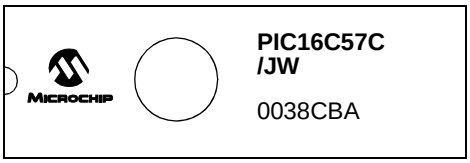
Example



28-Lead CERDIP Windowed



Example

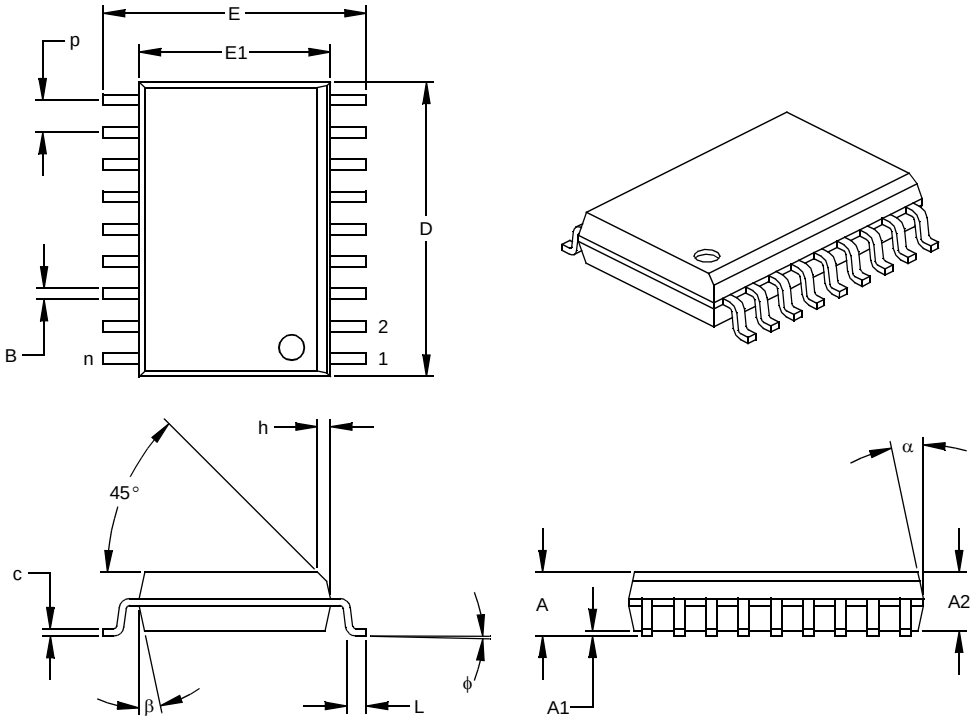


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-051

