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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57-lpi-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A twostage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle except for program branches.

The PIC16C54/CR54 and PIC16C55 address 512 x 12 of program memory, the PIC16C56/CR56 address 1K x 12 of program memory, and the PIC16C57/CR57 and PIC16C58/CR58 address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly. The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 (for PIC16C54/56/58) and Table 3-2 (for PIC16C55/57).

NOTES:

NOTES:

7.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., MOVF PORTB, W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

7.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used (RA<3:0>). Bits 7-4 are unimplemented and read as '0's.

7.2 PORTB

PORTB is an 8-bit I/O Register (PORTB<7:0>).

7.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16CR56, PIC16CR56, PIC16CS8 and PIC16CR58.

7.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the TRIS f instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

Note:	A read of the ports reads the pins, not the							
	output data latches. That is, if an output							
	driver on a pin is enabled and driven high,							
	but the external system is holding it low, a							
	read of the port will indicate that the pin is							
	low.							

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

TABLE 7-1:	SUMMARY O	F PORT	REGISTERS
			LOIOI LIVO

Value on Value on Bit 4 Bit 3 Bit 1 Bit 0 MCLR and Address Name Bit 7 Bit 6 Bit 5 Bit 2 Power-On Reset WDT Reset TRIS N/A I/O Control Registers (TRISA, TRISB, TRISC) 1111 1111 1111 1111 05h PORTA RA3 RA2 RA1 RA0 _ _ _ _ xxxx _ _ _ _ uuuu PORTB 06h RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0 XXXX XXXX uuuu uuuu 07h PORTC RC7 RC6 RC5 RC4 RC3 RC2 RC1 RC0 XXXX XXXX uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'

7.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 7-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

FIGURE 7-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



9.1 Configuration Bits

Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. Nine bits are code protection bits for the PIC16C54A, PIC16CR54A, PIC16C55A, PIC16C56A, PIC16CR56A, PIC16CR57C, PIC16CR57C, PIC16CR57C,

PIC16C58B, and PIC16CR58B devices (Register 9-1). One bit is for code protection for the PIC16C54, PIC16C55, PIC16C56 and PIC16C57 devices (Register 9-2).

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" diagrams in the back of this data sheet).

REGISTER 9-1: CONFIGURATION WORD FOR PIC16C54A/CR54A/C54C/CR54C/C55A/C56A/ CR56A/C57C/CR57C/C58B/CR58B

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0
bit 11											bit 0

bit 11-3: CP: Code Protection Bit

- 1 = Code protection off
 - 0 =Code protection on
- bit 2: WDTE: Watchdog timer enable bit
 - 1 = WDT enabled
 - 0 = WDT disabled

bit 1-0: FOSC1:FOSC0: Oscillator Selection Bit

- 00 = LP oscillator
- 01 = XT oscillator
- 10 = HS oscillator
- 11 = RC oscillator

Note 1: Refer to the PIC16C5X Programming Specification (Literature Number DS30190) to determine how to access the configuration word.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

SUBWF	Subtr	act V	V from	f				
Syntax:	[label]	S	UBWF	f,d				
Operands:	$0 \le f \le d \in [0]$	≦ 31 (,1]						
Operation:	(f) – (^v	$W) \rightarrow$	(dest)					
Status Affected:	C, DC	;, Z						
Encoding:	0000) 1	LOdf	ffff				
Description:	Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.							
Words:	1							
Cycles:	1							
Example 1:	SUBW	F	REG1,	1				
Before Instruct REG1 W C After Instructi REG1 W C Example 2: Before Instructi REG1 W C After Instructi	ction = = on = = ction = = on	3 2 ? 1 2 1 2 ?	; resu	ılt is posi	tive			
REG1	=	0						
W	=	2						
С	=	1	; resu	ult is zero				
Example 3: Before Inst REG1 W C After Instructi	ructior = = = on	ו 1 2 ?						
REG1	=	0xFl	F					
W	=	2						
С	=	0	; resu	ılt is nega	ative			

SWAPF	Swap Nibbles in f
Syntax:	[label] SWAPF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$
Operation:	$(f<3:0>) \rightarrow (dest<7:4>);$ $(f<7:4>) \rightarrow (dest<3:0>)$
Status Affected:	None
Encoding:	0011 10df ffff
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.
Words:	1
Cycles:	1
Example	SWAPF REG1, 0
REG1 After Instructi REG1 W	= 0xA5 ion = 0xA5 = 0x5A
TRIS	Load TRIS Register
Syntax:	[<i>label</i>] TRIS f
Operands:	f = 5, 6 or 7
Operation:	$(W) \rightarrow TRIS$ register f
Status Affected:	None
Encoding:	0000 0000 0fff
Description:	TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register.
Words:	1
Cycles:	1
Example	TRIS PORTB
Before Instruc W After Instructi TRISB	ction = 0xA5 on = 0xA5

12.3 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended				
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions
D001	Vdd	Supply Voltage PIC16C5X-RCE PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-LPE	3.25 3.25 4.5 4.5 2.5		6.0 6.0 5.5 5.5 6.0	V V V V V	
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	_	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current ⁽²⁾ PIC16C5X-RCE ⁽³⁾ PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-HSE PIC16C5X-LPE		1.8 1.8 4.8 9.0 19	3.3 3.3 10 10 20 55	mA mA mA mA μA	Fosc = 4 MHz, VDD = $5.5V$ Fosc = 4 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 16 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $3.25V$, WDT disabled
D020	IPD	Power-down Current ⁽²⁾	_	5.0 0.8	22 18	μΑ μΑ	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 PIC16LCR54A-04I (Commercial, Industrial)				ard Oper ting Tem	ating C	ondition 0° -40°	s (unless otherwise specified) $C \le TA \le +70^{\circ}C$ for commercial $C \le TA \le +85^{\circ}C$ for industrial
PIC16CR54A-04, 10, 20 PIC16CR54A-04I, 10I, 20I (Commercial, Industrial)			Standa Opera	ard Oper ting Temp	erating C	ondition 0° –40°	s (unless otherwise specified) $C \le TA \le +70^{\circ}C$ for commercial $C \le TA \le +85^{\circ}C$ for industrial
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions
	IPD	Power-down Current ⁽²⁾					
D006		PIC16LCR54A-Commercial		1.0 2.0 3.0 5.0	6.0 8.0* 15 25	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled
D006A		PIC16CR54A-Commercial		1.0 2.0 3.0 5.0	6.0 8.0* 15 25	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled
D007		PIC16LCR54A-Industrial	 	1.0 2.0 3.0 3.0 5.0	8.0 10* 20* 18 45	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 4.0V, WDT enabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled
D007A		PIC16CR54A-Industrial		1.0 2.0 3.0 3.0 5.0	8.0 10* 20* 18 45	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 4.0V, WDT enabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled

Legend: Rows with standard voltage device data only are shaded for improved readability.

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.
- **Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

13.4 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

DC CH	ARACTE	RISTICS	Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions	
D030	VIL	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss		0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes	
D040	Vih	Input High Voltage I/O ports I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD VDD	V V V V V V V	For all VDD ⁽⁴⁾ 4.0V < VDD ≤ 5.5V ⁽⁴⁾ VDD > 5.5V RC mode only ⁽³⁾ XT, HS and LP modes	
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	—	—	V		
D060	lı∟	Input Leakage Current ^(1,2) I/O ports MCLR MCLR T0CKI OSC1	-1.0 -5.0 -3.0 -3.0	0.5 — 0.5 0.5 0.5	+1.0 	μΑ μΑ μΑ μΑ	For VDD \leq 5.5V: VSS \leq VPIN \leq VDD, pin at hi-impedance VPIN = VSS + 0.25V VPIN = VDD VSS \leq VPIN \leq VDD VSS \leq VPIN \leq VDD, XT, HS and LP modes	
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, RC mode only	
D090	Vон	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	VDD - 0.7 VDD - 0.7			V V	IOH = -5.4 mA, VDD = 4.5 V IOH = -1.0 mA, VDD = 4.5 V, RC mode only	

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.



TABLE 13-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR54A

AC Chara	acteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units		
10	TosH2ckL	OSC1 [↑] to CLKOUT↓ ⁽¹⁾	—	15	30**	ns		
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	—	15	30**	ns		
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns		
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns		
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	_	40**	ns		
15	TioV2ckH	Port in valid before CLKOUT ⁽¹⁾	0.25 TCY+30*	_	_	ns		
16	TckH2iol	Port in hold after CLKOUT ⁽¹⁾	0*	_	_	ns		
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽²⁾	—	_	100*	ns		
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD		-	ns		
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD		_	ns		
20	TioR	Port output rise time ⁽²⁾		10	25**	ns		
21	TioF	Port output fall time ⁽²⁾	_	10	25**	ns		

* These parameters are characterized but not tested.

- ** These parameters are design targets and are not tested. No characterization data available at this time.
- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Please refer to Figure 13.1 for load conditions.

15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04 S PIC16LC54A-04I (Commercial, Industrial)				ard Ope ting Tem	perating	J Condi ure 	tions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $40^{\circ}C \le TA \le +85^{\circ}C$ for industrial
PIC16C54A-04, 10, 20 PIC16C54A-04I, 10I, 20I (Commercial, Industrial)				ard Ope ting Tem	perating	J Condi ure 	tions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $40^{\circ}C \le TA \le +85^{\circ}C$ for industrial
Param No.	Symbol	Characteristic/Device	Min	Тур†	Мах	Units	Conditions
	IPD	Power-down Current ⁽²⁾					
D006		PIC16LC5X	—	2.5	12	μΑ	VDD = 2.5V, WDT enabled, Commercial
			—	0.25	4.0	μΑ	VDD = 2.5V, WDT disabled, Commercial
			_	0.25	5.0	μΑ μΑ	VDD = 2.5V, WDT enabled, industrial $VDD = 2.5V$, WDT disabled, Industrial
D006A		PIC16C5X	_	4.0	12	μΑ	VDD = 3.0V, WDT enabled, Commercial
			—	0.25	4.0	μA	VDD = 3.0V, WDT disabled, Commercial
			—	5.0	14	μΑ	VDD = 3.0V, WDT enabled, Industrial
				0.3	5.0	μA	$v \Box U = 3.0v, v U T uisabled, industrial$

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

PIC16C5X

FIGURE 16-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)













17.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended) PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)				Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions		
D001	Vdd	Supply Voltage	3.0 4.5		5.5 5.5	V V	RC, XT, LP, and HS mode from 0 - 10 MHz from 10 - 20 MHz		
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode		
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset		
D010	IDD	Supply Current ⁽²⁾ XT and RC ⁽³⁾ modes HS mode	_	1.8 9.0	3.3 20	mA mA	Fosc = 4.0 MHz, Vdd = 5.5V Fosc = 20 MHz, Vdd = 5.5V		
D020	IPD	Power-down Current ⁽²⁾		0.3 10 12 4.8 18 26	17 50* 60* 31* 68* 90*	μΑ μΑ μΑ μΑ μΑ	VDD = 3.0V, WDT disabled VDD = 4.5V, WDT disabled VDD = 5.5V, WDT disabled VDD = 3.0V, WDT enabled VDD = 4.5V, WDT enabled VDD = 5.5V, WDT enabled		

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.









NOTES:

FIGURE 20-9: IOL vs. VOL, VDD = 5 V



20-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES*		N	IILLIMETERS	6
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	р		.026			0.65	
Overall Height	Α	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	Е	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25
Foot Angle	φ	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-150 Drawing No. C04-072

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