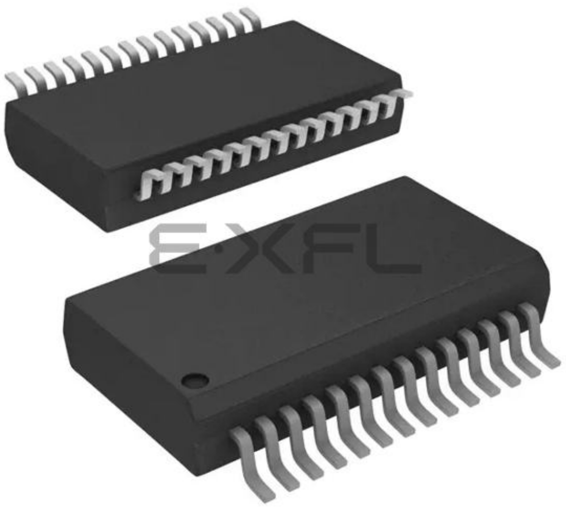

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57-rc-ss

NOTES:

8.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 9.2.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1, MOVWF 1, BSF 1,x,` etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

8.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 8-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 8-1: CHANGING PRESCALER (TIMER0→WDT)

```
CLRWDT                  ;Clear WDT
CLRF   TMR0             ;Clear TMR0 & Prescaler
MOVLW  B'00xx1111'      ;Last 3 instructions in
                         this example
OPTION                  ;are required only if
                        ;desired
CLRWDT                  ;PS<2:0> are 000 or
                        ;001
MOVLW  B'00xx1xxx'      ;Set Prescaler to
OPTION                  ;desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 8-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

EXAMPLE 8-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                      ;Clear WDT and
                            ;prescaler
MOVLW   B'xxxx0xxx'         ;Select TMR0, new
                            ;prescale value and
                            ;clock source
OPTION
```

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9.1 Configuration Bits

Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. Nine bits are code protection bits for the PIC16C54A, PIC16CR54A, PIC16C54C, PIC16CR54C, PIC16C55A, PIC16C56A, PIC16CR56A, PIC16C57C, PIC16CR57C, PIC16C58B, and PIC16CR58B devices (Register 9-1). One bit is for code protection for the PIC16C54, PIC16C55, PIC16C56 and PIC16C57 devices (Register 9-2).

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" diagrams in the back of this data sheet).

REGISTER 9-1: CONFIGURATION WORD FOR PIC16C54A/CR54A/C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0
bit 11											bit 0

bit 11-3: **CP**: Code Protection Bit
1 = Code protection off
0 = Code protection on

bit 2: **WDTE**: Watchdog timer enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection Bit
00 = LP oscillator
01 = XT oscillator
10 = HS oscillator
11 = RC oscillator

Note 1: Refer to the PIC16C5X Programming Specification (Literature Number DS30190) to determine how to access the configuration word.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

9.3 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

9.3.1 SLEEP

The Power-down mode is entered by executing a `SLEEP` instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the `SLEEP` instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{MCLR}$/V_{PP} pin low.

For lowest current consumption while powered down, the T0CKI input should be at V_{DD} or V_{SS} and the $\overline{MCLR}$/V_{PP} pin must be at a logic high level ($\overline{MCLR}$ = V_{IH}).

9.3.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. An external RESET input on $\overline{MCLR}$/V_{PP} pin.
2. A Watchdog Timer Time-out Reset (if WDT was enabled).

Both of these events cause a device RESET. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the cause of device RESET. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when `SLEEP` is invoked.

The WDT is cleared when the device wakes from SLEEP, regardless of the wake-up source.

9.4 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip does not recommend code protecting windowed devices.

9.5 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

Note:	Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

10.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 10-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers in that bank is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 10-1: OPCODE FIELD DESCRIPTIONS

Field	Description
`f`	Register file address (0x00 to 0x1F)
`W`	Working register (accumulator)
`b`	Bit address within an 8-bit file register
`k`	Literal field, constant data or label
`x`	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
`d`	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
`label`	Label name
`TOS`	Top of Stack
`PC`	Program Counter
`WDT`	Watchdog Timer Counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit
`dest`	Destination, either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time would be 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time would be 2 μs.

Figure 10-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations

11 6	5	4 0
OPCODE	d	f (FILE #)

d = 0 for destination W
d = 1 for destination f
f = 5-bit file register address

Bit-oriented file register operations

11 8	7 5	4 0
OPCODE	b (BIT #)	f (FILE #)

b = 3-bit bit address
f = 5-bit file register address

Literal and control operations (except GOTO)

11 8	7 0
OPCODE	k (literal)

k = 8-bit immediate value

Literal and control operations - GOTO instruction

11 9	8 0
OPCODE	k (literal)

k = 9-bit immediate value

RLF — Rotate Left f through Carry

Syntax: [*label*] RLF f,d

Operands: $0 \leq f \leq 31$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Encoding:

`0011`	`01df`	`ffff`

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: `RLF REG1,0`

```
Before Instruction
    REG1  =  1110 0110
    C     =  0
After Instruction
    REG1  =  1110 0110
    W     =  1100 1100
    C     =  1
```

RRF — Rotate Right f through Carry

Syntax: [*label*] RRF f,d

Operands: $0 \leq f \leq 31$
$d \in [0,1]$

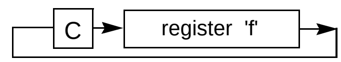
Operation: See description below

Status Affected: C

Encoding:

`0011`	`00df`	`ffff`

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Example: `RRF REG1,0`

```
Before Instruction
    REG1  =  1110 0110
    C     =  0
After Instruction
    REG1  =  1110 0110
    W     =  0111 0011
    C     =  0
```

SLEEP — Enter SLEEP Mode

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler; if assigned
1 → $\overline{TO}$;
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

`0000`	`0000`	`0011`

Description: Time-out status bit ($\overline{TO}$) is set. The power-down status bit ($\overline{PD}$) is cleared. The WDT and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example: `SLEEP`

SUBWF — Subtract W from f

Syntax:	[*label*] SUBWF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	(f) – (W) → (dest)
Status Affected:	C, DC, Z
Encoding:	`0000` `10df` `ffff`
Description:	Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1

Example 1: `SUBWF REG1, 1`

```
Before Instruction
  REG1  =  3
  W     =  2
  C     =  ?
After Instruction
  REG1  =  1
  W     =  2
  C     =  1      ; result is positive
```

Example 2:

```
Before Instruction
  REG1  =  2
  W     =  2
  C     =  ?
After Instruction
  REG1  =  0
  W     =  2
  C     =  1      ; result is zero
```

Example 3:

```
Before Instruction
  REG1  =  1
  W     =  2
  C     =  ?
After Instruction
  REG1  =  0xFF
  W     =  2
  C     =  0      ; result is negative
```

SWAPF — Swap Nibbles in f

Syntax:	[*label*] SWAPF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	(f<3:0>) → (dest<7:4>); (f<7:4>) → (dest<3:0>)
Status Affected:	None
Encoding:	`0011` `10df` `ffff`
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.
Words:	1
Cycles:	1

Example `SWAPF REG1, 0`

```
Before Instruction
  REG1  =  0xA5
After Instruction
  REG1  =  0xA5
  W     =  0x5A
```

TRIS — Load TRIS Register

Syntax:	[*label*] TRIS f
Operands:	f = 5, 6 or 7
Operation:	(W) → TRIS register f
Status Affected:	None
Encoding:	`0000` `0000` `0fff`
Description:	TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register.
Words:	1
Cycles:	1

Example `TRIS PORTB`

```
Before Instruction
  W      =  0xA5
After Instruction
  TRISB  =  0xA5
```

XORLW **Exclusive OR literal with W**

Syntax:	[*label*] XORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .XOR. k $\rightarrow$ (W)
Status Affected:	Z
Encoding:	`1111` `kkkk` `kkkk`
Description:	The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1
Example:	`XORLW` 0xAF

Before Instruction
W = 0xB5
After Instruction
W = 0x1A

XORWF **Exclusive OR W with f**

Syntax:	[*label*] XORWF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(W) .XOR. (f) $\rightarrow$ (dest)
Status Affected:	Z
Encoding:	`0001` `10df` `ffff`
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example	`XORWF REG,1`

Before Instruction
REG = 0xAF
W = 0xB5
After Instruction
REG = 0x1A
W = 0xB5

TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial –40°C ≤ TA ≤ +125°C for extended						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
1	TOSC	External CLKIN Period(1)	250	—	—	ns	XT OSC mode
			100	—	—	ns	10 MHz mode
			50	—	—	ns	HS OSC mode (Comm/Ind)
			62.5	—	—	ns	HS OSC mode (Ext)
			25	—	—	μs	LP OSC mode
		Oscillator Period(1)	250	—	—	ns	RC OSC mode
			250	—	10,000	ns	XT OSC mode
			100	—	250	ns	10 MHz mode
			50	—	250	ns	HS OSC mode (Comm/Ind)
			62.5	—	250	ns	HS OSC mode (Ext)
			25	—	—	μs	LP OSC mode
2	TCY	Instruction Cycle Time(2)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 PIC16LCR54A-04I (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
PIC16CR54A-04, 10, 20 **PIC16CR54A-04I, 10I, 20I** (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Symbol**	**Characteristic/Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**					
D001		PIC16LCR54A	2.0	—	6.25	V	
D001 D001A		PIC16CR54A	2.5 4.5	— —	6.25 5.5	V V	RC and XT modes HS mode
D002	VDR	**RAM Data Retention Voltage**(1)	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
	IDD	**Supply Current**(2)					
D005		PICLCR54A	— —	10 —	20 70	μA μA	Fosc = 32 kHz, VDD = 2.0V Fosc = 32 kHz, VDD = 6.0V
D005A		PIC16CR54A	 — — — — —	 2.0 0.8 90 4.8 9.0	 3.6 1.8 350 10 20	 mA mA μA mA mA	**RC(3) and XT modes:** FOSC = 4.0 MHz, VDD = 6.0V FOSC = 4.0 MHz, VDD = 3.0V FOSC = 200 kHz, VDD = 2.5V **HS mode:** FOSC = 10 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

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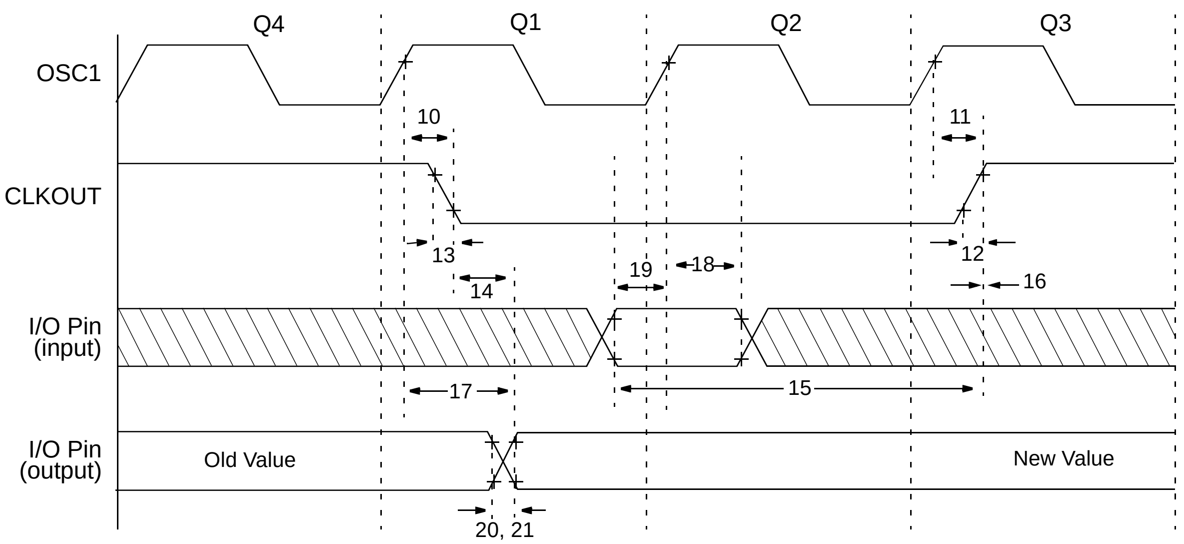
FIGURE 13-3: CLKOUT AND I/O TIMING - PIC16CR54A



Note: Please refer to Figure 13.1 for load conditions.

TABLE 13-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial –40°C ≤ TA ≤ +125°C for extended					
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓[(1)]	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑[(1)]	—	15	30**	ns
12	TckR	CLKOUT rise time[(1)]	—	5.0	15**	ns
13	TckF	CLKOUT fall time[(1)]	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid[(1)]	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑[(1)]	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑[(1)]	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid[(2)]	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time[(2)]	—	10	25**	ns
21	TioF	Port output fall time[(2)]	—	10	25**	ns

* These parameters are characterized but not tested.
** These parameters are design targets and are not tested. No characterization data available at this time.
† Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.
2: Please refer to Figure 13.1 for load conditions.

FIGURE 14-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD

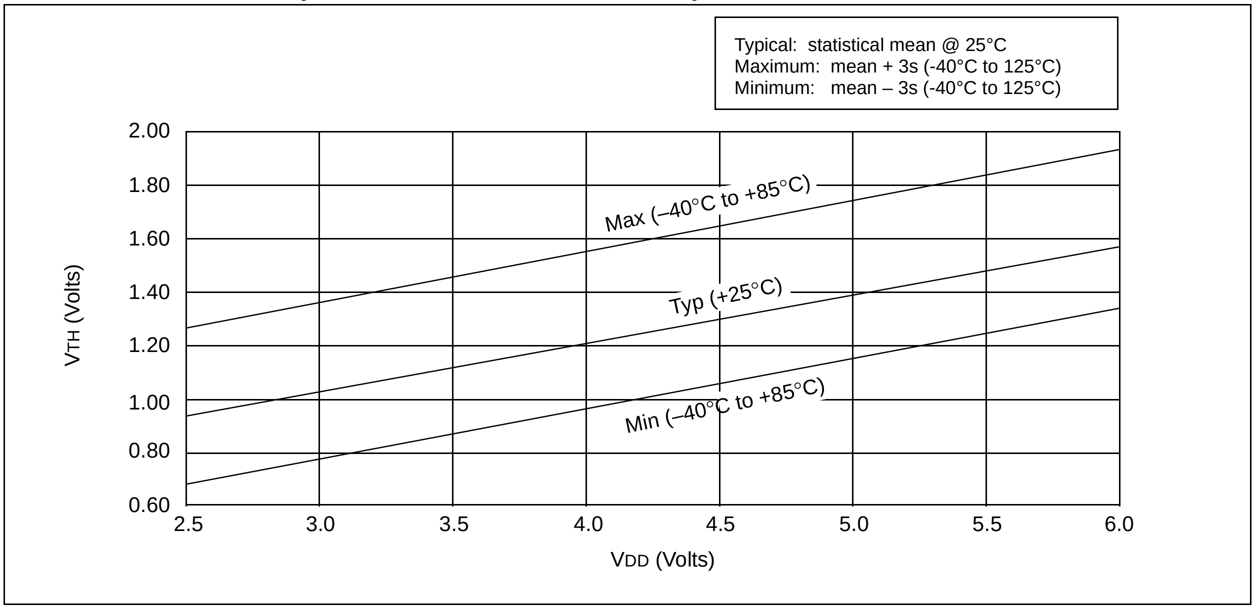
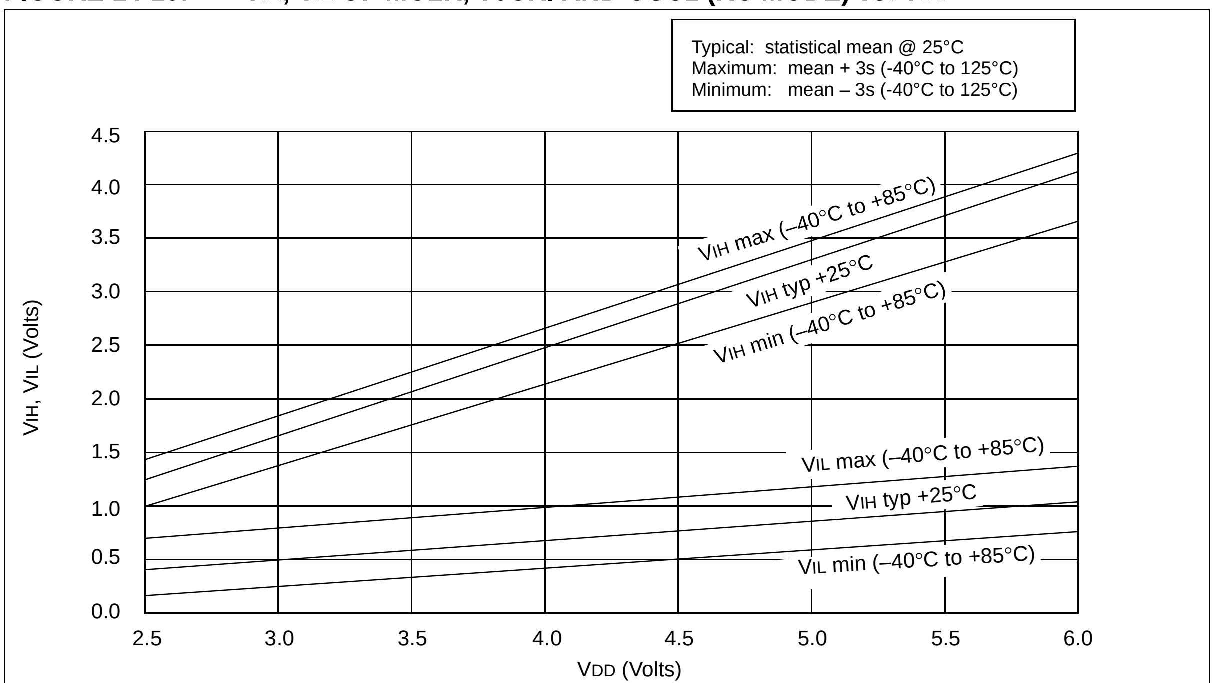


FIGURE 14-10: VIH, VIL OF $\overline{\text{MCLR}}$, T0CKI AND OSC1 (RC MODE) vs. VDD



Note: These input pins have Schmitt Trigger input buffers.

15.5 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T	
F Frequency	T Time

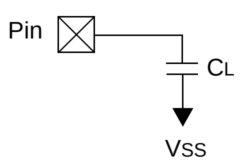
Lowercase letters (pp) and their meanings:

pp	
2 to	mc $\overline{\text{MCLR}}$
ck CLKOUT	osc oscillator
cy cycle time	os OSC1
drt device reset timer	t0 T0CKI
io I/O port	wdt watchdog timer

Uppercase letters and their meanings:

S	
F Fall	P Period
H High	R Rise
I Invalid (Hi-impedance)	V Valid
L Low	Z Hi-impedance

FIGURE 15-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54A



C_L = 50 pF for all pins and OSC2 for RC modes

0 -15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

FIGURE 16-22: PORTA, B AND C I_{OL} vs. V_{OL}, V_{DD} = 3V

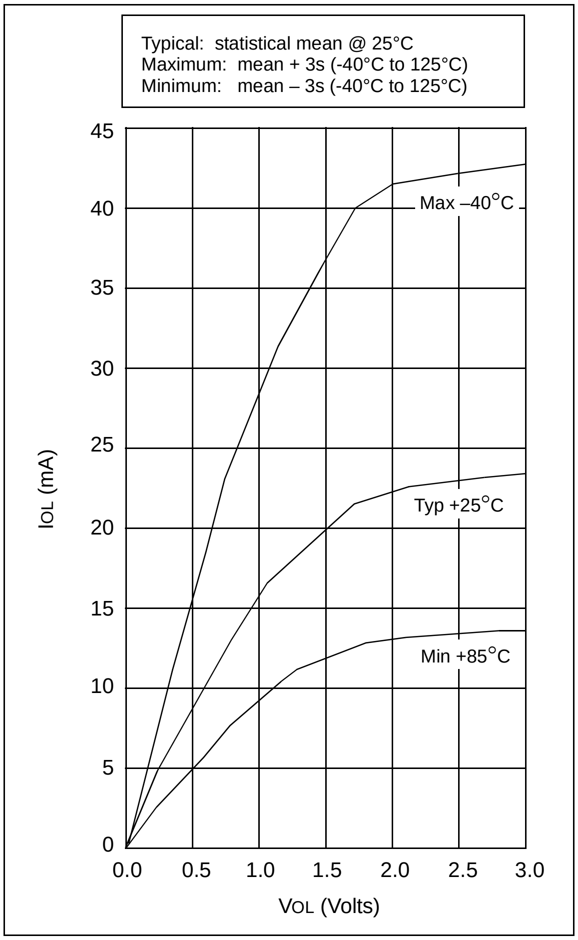


FIGURE 16-23: PORTA, B AND C I_{OL} vs. V_{OL}, V_{DD} = 5V

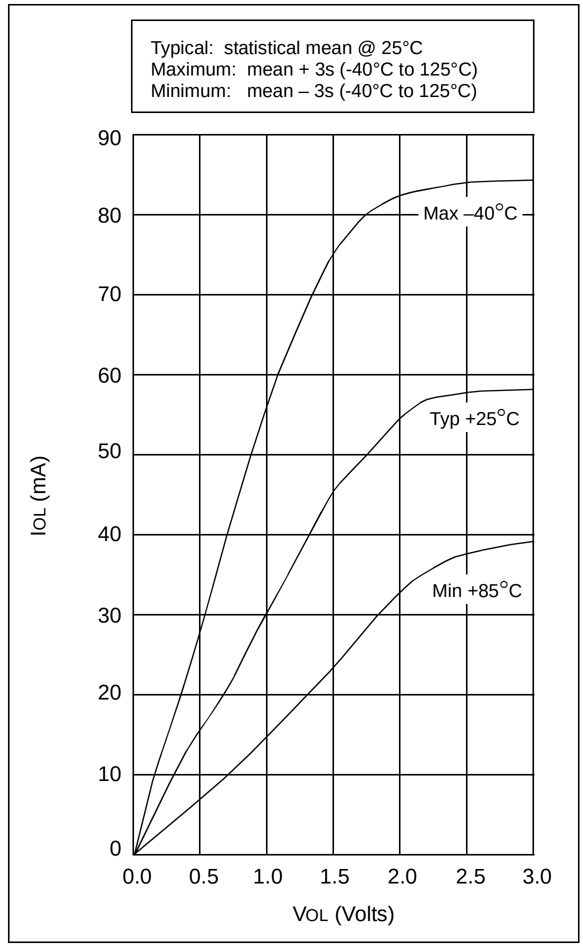
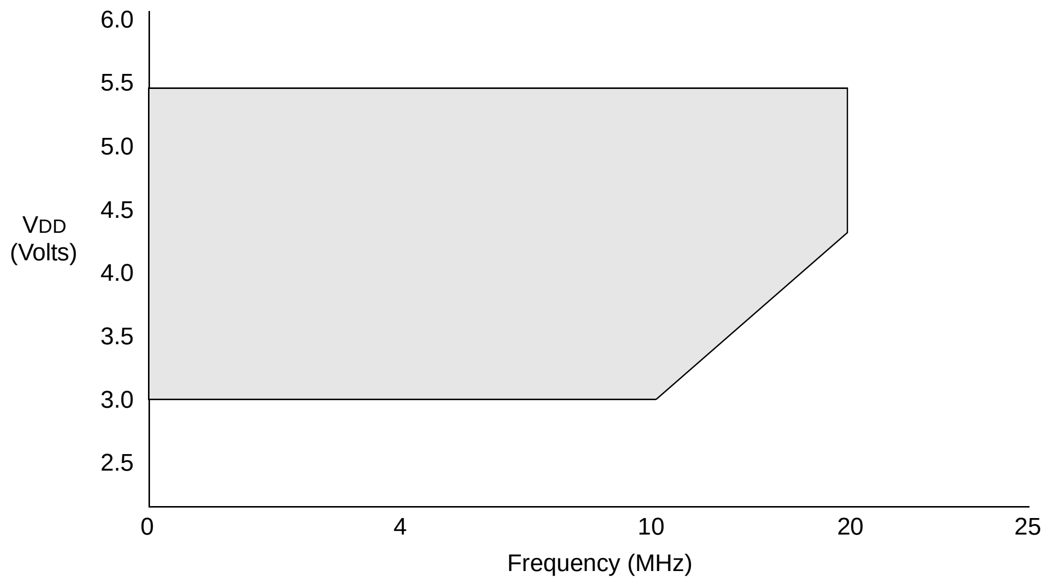


TABLE 16-2: INPUT CAPACITANCE FOR PIC16C54A/C58A

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{\text{MCLR}}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

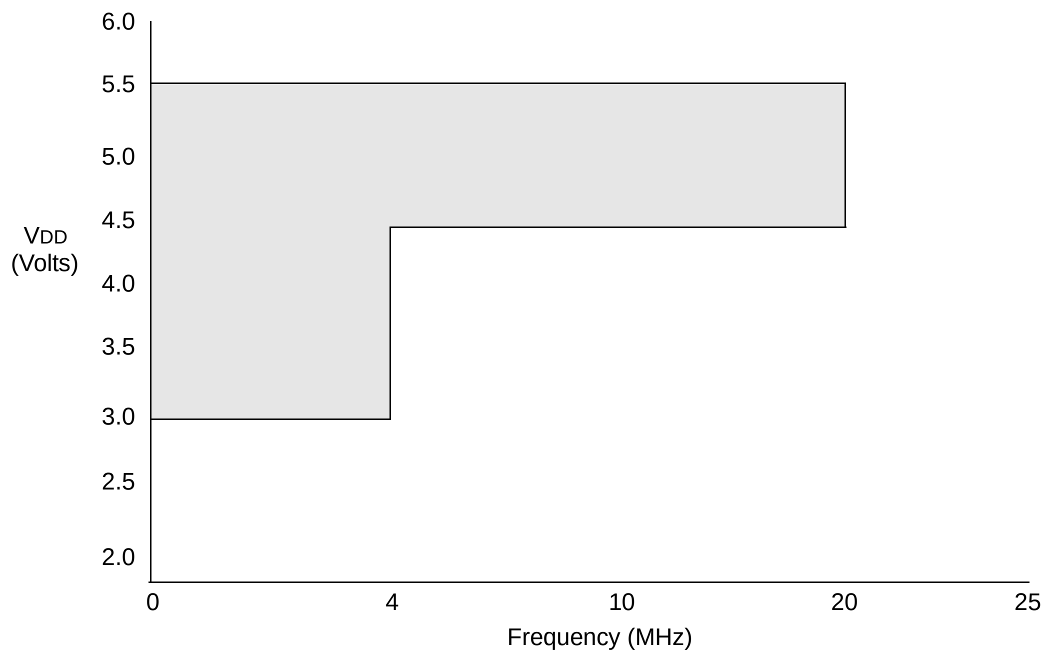
FIGURE 17-1: PIC16C54C/55A/56A/57C/58B-04, 20 VOLTAGE-FREQUENCY GRAPH, 0°C ≤ T_A ≤ +70°C (COMMERCIAL TEMPS)



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

FIGURE 17-2: PIC16C54C/55A/56A/57C/58B-04, 20 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ T_A < 0°C, +70°C < T_A ≤ +125°C (OUTSIDE OF COMMERCIAL TEMPS)



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

17.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial)	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial
PIC16C5X **PIC16CR5X** (Commercial, Industrial)	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial

Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
	VDD	**Supply Voltage**					
D001		PIC16LC5X	2.5 2.7 2.5	— — —	5.5 5.5 5.5	V V V	–40°C ≤ TA ≤ + 85°C, 16LCR5X –40°C ≤ TA ≤ 0°C, 16LC5X 0°C ≤ TA ≤ + 85°C 16LC5X
D001A		PIC16C5X	 3.0 4.5	 — —	 5.5 5.5	 V V	RC, XT, LP and HS mode from 0 - 10 MHz from 10 - 20 MHz
D002	VDR	**RAM Data Retention Voltage**(1)	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF, 25°C

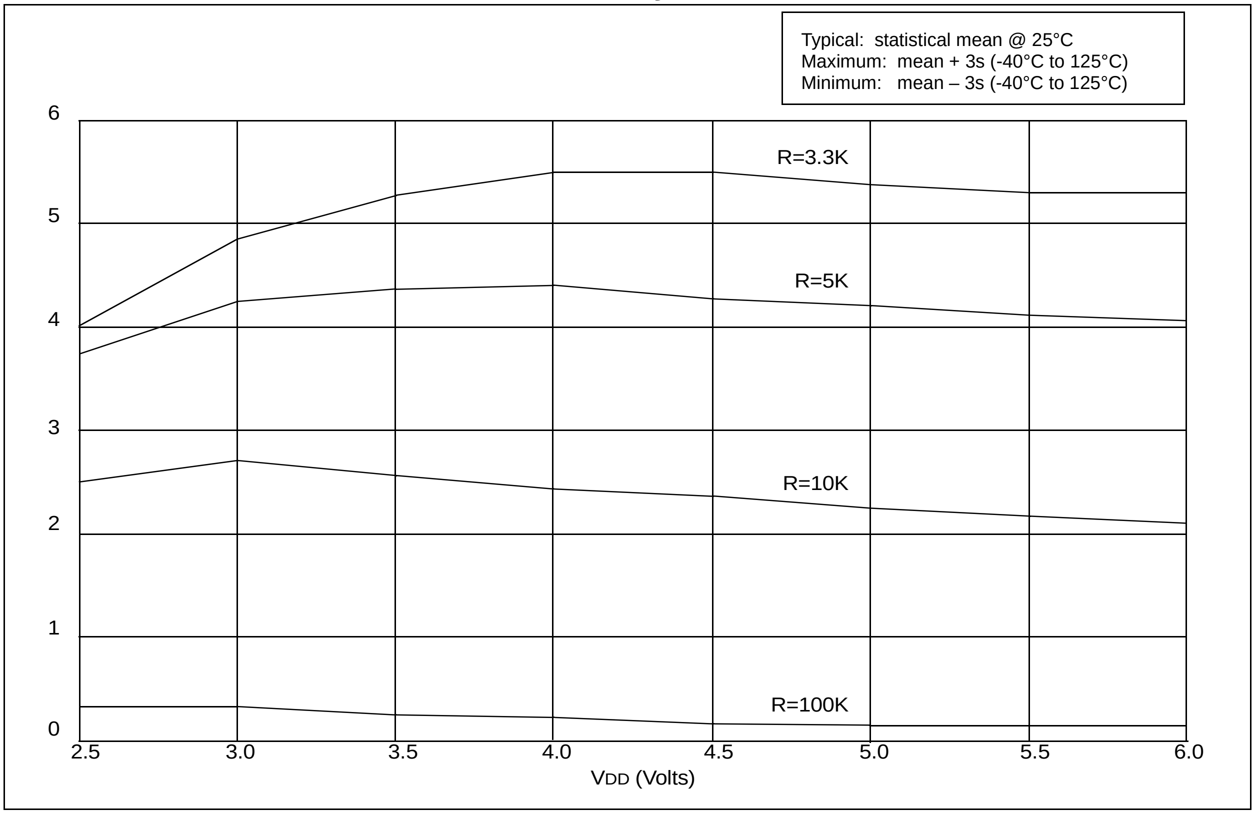
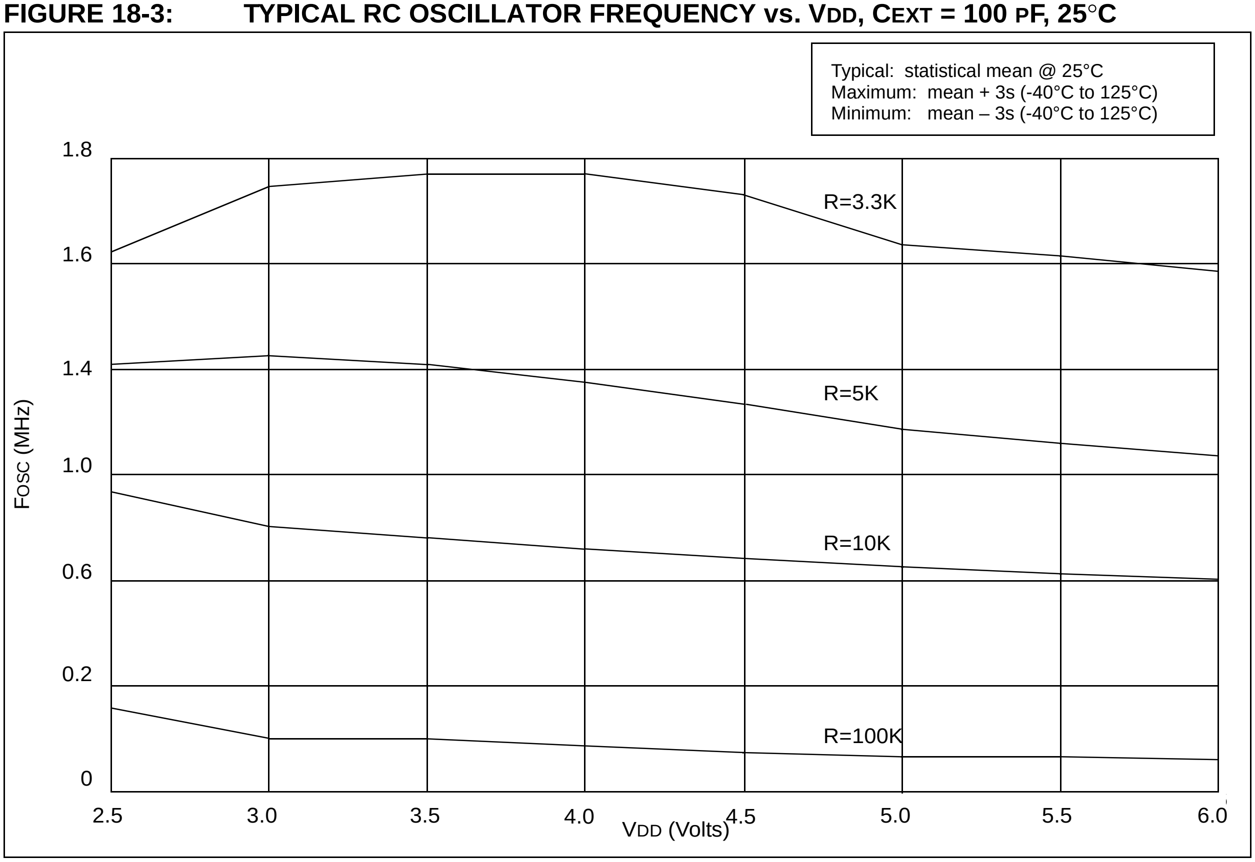


FIGURE 18-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF, 25°C



19.0 ELECTRICAL CHARACTERISTICS - PIC16LC54C 40MHz

Absolute Maximum Ratings[†]

Ambient temperature under bias........ –55°C to +125°C
Storage temperature .... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS}........ 0 to +14V
Voltage on all other pins with respect to V_{SS} .... –0.6V to (V_{DD} + 0.6V)
Total power dissipation[(1)] .... 800 mW
Max. current out of V_{SS} pin .... 150 mA
Max. current into V_{DD} pin .... 100 mA
Max. current into an input pin (T0CKI only) .... ±500 μA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})........ ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) .... ±20 mA
Max. output current sunk by any I/O pin .... 25 mA
Max. output current sourced by any I/O pin .... 20 mA
Max. output current sourced by a single I/O (Port A, B or C) .... 50 mA
Max. output current sunk by a single I/O (Port A, B or C)........ 50 mA

Note 1: Power dissipation is calculated as follows: Pdis = V_{DD} x {I_{DD} - $\sum$ I_{OH}} + $\sum$ {(V_{DD}-V_{OH}) x I_{OH}} + $\sum$(V_{OL} x I_{OL})

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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