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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3.25V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16c57-rce-p">https://www.e-xfl.com/product-detail/microchip-technology/pic16c57-rce-p</a>

# PIC16C5X

**TABLE 3-2: PINOUT DESCRIPTION - PIC16C55, PIC16C57, PIC16CR57**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	DIP	SOIC	SSOP			
RA0	6	6	5	I/O	TTL	Bi-directional I/O port
RA1	7	7	6	I/O	TTL	
RA2	8	8	7	I/O	TTL	
RA3	9	9	8	I/O	TTL	
RB0	10	10	9	I/O	TTL	Bi-directional I/O port
RB1	11	11	10	I/O	TTL	
RB2	12	12	11	I/O	TTL	
RB3	13	13	12	I/O	TTL	
RB4	14	14	13	I/O	TTL	
RB5	15	15	15	I/O	TTL	
RB6	16	16	16	I/O	TTL	
RB7	17	17	17	I/O	TTL	
RC0	18	18	18	I/O	TTL	Bi-directional I/O port
RC1	19	19	19	I/O	TTL	
RC2	20	20	20	I/O	TTL	
RC3	21	21	21	I/O	TTL	
RC4	22	22	22	I/O	TTL	
RC5	23	23	23	I/O	TTL	
RC6	24	24	24	I/O	TTL	
RC7	25	25	25	I/O	TTL	
T0CKI	1	1	2	I	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in use, to reduce current consumption.
$\overline{\text{MCLR}}$	28	28	28	I	ST	Master clear (RESET) input. This pin is an active low RESET to the device.
OSC1/CLKIN	27	27	27	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	26	26	26	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
VDD	2	2	3,4	P	—	Positive supply for logic and I/O pins.
Vss	4	4	1,14	P	—	Ground reference for logic and I/O pins.
N/C	3,5	3,5	—	—	—	Unused, do not connect.

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

# PIC16C5X

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NOTES:

# PIC16C5X

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NOTES:

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## 6.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 6-1).

The Special Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

**TABLE 6-1: SPECIAL FUNCTION REGISTER SUMMARY**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Details on Page
N/A	TRIS	I/O Control Registers (TRISA, TRISB, TRISC)								1111 1111	35
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								--11 1111	30
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32
01h	TMR0	Timer0 Module Register								xxxx xxxx	38
02h <sup>(1)</sup>	PCL	Low order 8 bits of PC								1111 1111	31
03h	STATUS	PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	29
04h	FSR	Indirect data memory address pointer								1xxx xxxx <sup>(3)</sup>	32
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	35
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	35
07h <sup>(2)</sup>	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	35

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused

- Note 1:** The upper byte of the Program Counter is not directly accessible. See Section 6.5 for an explanation of how to access these bits.
- Note 2:** File address 07h is a General Purpose Register on the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58 and PIC16CR58.
- Note 3:** These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for  $\overline{MCLR}$  and WDT Reset, the value is 111u uuuu.

# PIC16C5X

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NOTES:

# PIC16C5X

FIGURE 8-3:       TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALER

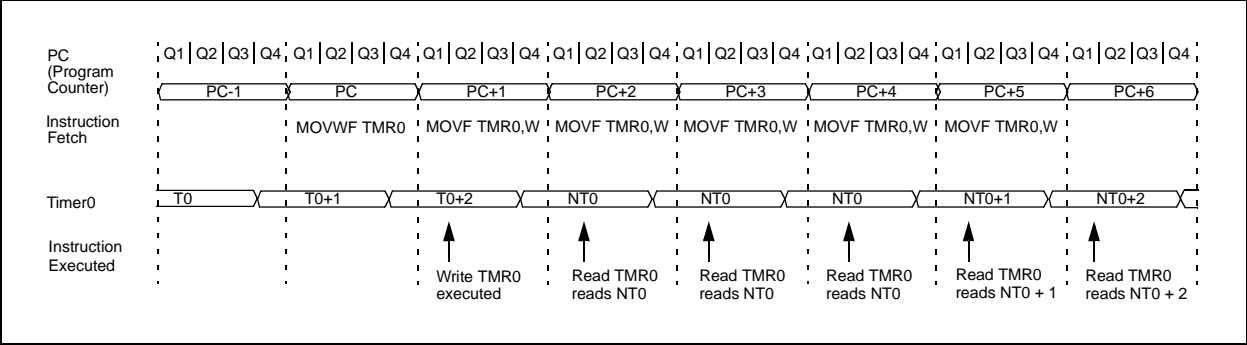


FIGURE 8-4:       TIMER0 TIMING: INTERNAL CLOCK/PRESCALER 1:2

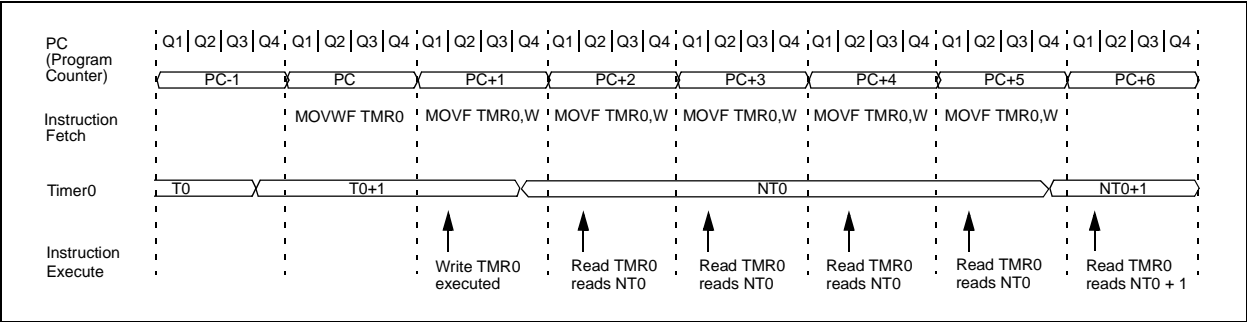


TABLE 8-1:       REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on MCLR and WDT Reset
01h	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells not used by Timer0.

# PIC16C5X

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NOTES:

## 9.3 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

### 9.3.1 SLEEP

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the  $\overline{TO}$  bit (STATUS<4>) is set, the  $\overline{PD}$  bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the  $\overline{MCLR}/VPP$  pin low.

For lowest current consumption while powered down, the  $T0CKI$  input should be at  $VDD$  or  $VSS$  and the  $\overline{MCLR}/VPP$  pin must be at a logic high level ( $\overline{MCLR} = V_{IH}$ ).

### 9.3.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. An external RESET input on  $\overline{MCLR}/VPP$  pin.
2. A Watchdog Timer Time-out Reset (if WDT was enabled).

Both of these events cause a device RESET. The  $\overline{TO}$  and  $\overline{PD}$  bits can be used to determine the cause of device RESET. The  $\overline{TO}$  bit is cleared if a WDT time-out occurred (and caused wake-up). The  $\overline{PD}$  bit, which is set on power-up, is cleared when SLEEP is invoked.

The WDT is cleared when the device wakes from SLEEP, regardless of the wake-up source.

## 9.4 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

**Note:** Microchip does not recommend code protecting windowed devices.

## 9.5 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

**Note:** Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

# PIC16C5X

**TABLE 10-2: INSTRUCTION SET SUMMARY**

Mnemonic, Operands		Description	Cycles	12-Bit Opcode			Status Affected	Notes
				MSb	LSb			
ADDWF	f, d	Add W and f	1	0001	11df	ffff	C, DC, Z	1, 2, 4
ANDWF	f, d	AND W with f	1	0001	01df	ffff	Z	2, 4
CLRF	f	Clear f	1	0000	011f	ffff	Z	4
CLRW	—	Clear W	1	0000	0100	0000	Z	
COMF	f, d	Complement f	1	0010	01df	ffff	Z	
DECF	f, d	Decrement f	1	0000	11df	ffff	Z	2, 4
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	0010	11df	ffff	None	2, 4
INCF	f, d	Increment f	1	0010	10df	ffff	Z	2, 4
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	0011	11df	ffff	None	2, 4
IORWF	f, d	Inclusive OR W with f	1	0001	00df	ffff	Z	2, 4
MOVF	f, d	Move f	1	0010	00df	ffff	Z	2, 4
MOVWF	f	Move W to f	1	0000	001f	ffff	None	1, 4
NOP	—	No Operation	1	0000	0000	0000	None	
RLF	f, d	Rotate left f through Carry	1	0011	01df	ffff	C	2, 4
RRF	f, d	Rotate right f through Carry	1	0011	00df	ffff	C	2, 4
SUBWF	f, d	Subtract W from f	1	0000	10df	ffff	C, DC, Z	1, 2, 4
SWAPF	f, d	Swap f	1	0011	10df	ffff	None	2, 4
XORWF	f, d	Exclusive OR W with f	1	0001	10df	ffff	Z	2, 4
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	0100	bbbf	ffff	None	2, 4
BSF	f, b	Bit Set f	1	0101	bbbf	ffff	None	2, 4
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	0110	bbbf	ffff	None	
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	0111	bbbf	ffff	None	
LITERAL AND CONTROL OPERATIONS								
ANDLW	k	AND literal with W	1	1110	kkkk	kkkk	Z	1
CALL	k	Call subroutine	2	1001	kkkk	kkkk	None	
CLRWDT	k	Clear Watchdog Timer	1	0000	0000	0100	TO, PD	
GOTO	k	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW	k	Inclusive OR Literal with W	1	1101	kkkk	kkkk	Z	
MOVLW	k	Move Literal to W	1	1100	kkkk	kkkk	None	
OPTION	k	Load OPTION register	1	0000	0000	0010	None	
RETLW	k	Return, place Literal in W	2	1000	kkkk	kkkk	None	
SLEEP	—	Go into standby mode	1	0000	0000	0011	TO, PD	
TRIS	f	Load TRIS register	1	0000	0000	0fff	None	3
XORLW	k	Exclusive OR Literal to W	1	1111	kkkk	kkkk	Z	

- Note 1:** The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO (see Section 6.5 for more on program counter).
- 2:** When an I/O register is modified as a function of itself (e.g. `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 3:** The instruction `TRIS f`, where  $f = 5, 6$  or  $7$  causes the contents of the W register to be written to the tristate latches of PORTA, B or C respectively. A '1' forces the pin to a hi-impedance state and disables the output buffers.
- 4:** If this instruction is executed on the TMR0 register (and, where applicable,  $d = 1$ ), the prescaler will be cleared (if assigned to TMR0).

# PIC16C5X

## COMF Complement f

Syntax: [ *label* ] COMF f,d

Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$

Operation:  $(f) \rightarrow (dest)$

Status Affected: Z

Encoding: 

0010	01df	ffff
------	------	------

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: COMF REG1, 0

Before Instruction

REG1 = 0x13

After Instruction

REG1 = 0x13

W = 0xEC

## DECF Decrement f

Syntax: [ *label* ] DECF f,d

Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$

Operation:  $(f) - 1 \rightarrow (dest)$

Status Affected: Z

Encoding: 

0000	11df	ffff
------	------	------

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: DECF CNT, 1

Before Instruction

CNT = 0x01

Z = 0

After Instruction

CNT = 0x00

Z = 1

## DECFSZ Decrement f, Skip if 0

Syntax: [ *label* ] DECFSZ f,d

Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$

Operation:  $(f) - 1 \rightarrow d$ ; skip if result = 0

Status Affected: None

Encoding: 

0010	11df	ffff
------	------	------

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.  
 If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example: 

HERE	DECFSZ	CNT, 1
	GOTO	LOOP
CONTINUE	•	
	•	
	•	

Before Instruction

PC = address (HERE)

After Instruction

CNT = CNT - 1;

if CNT = 0,

PC = address (CONTINUE);

if CNT  $\neq$  0,

PC = address (HERE+1)

FIGURE 14-15: WDT TIMER TIME-OUT PERIOD vs. VDD<sup>(1)</sup>

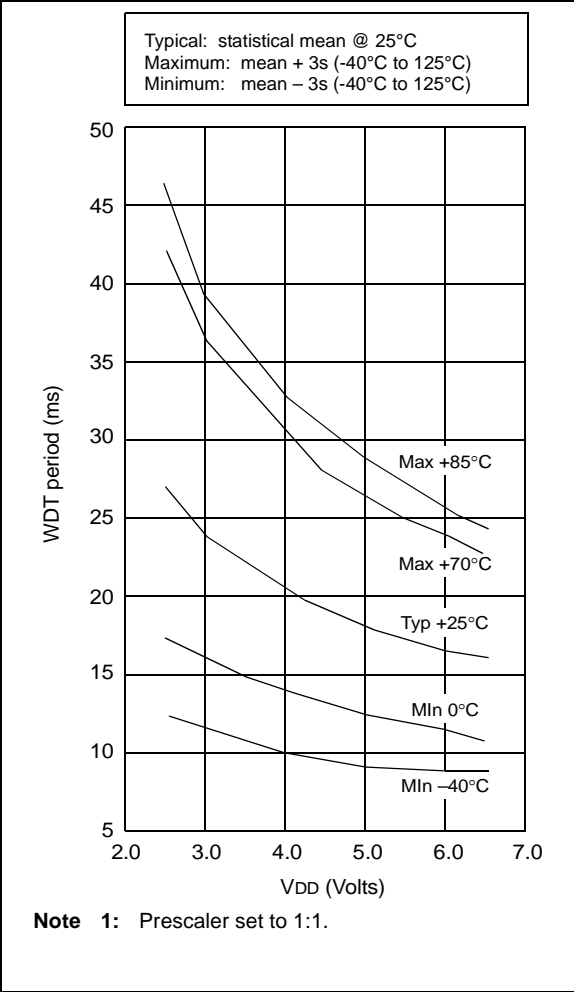


FIGURE 14-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD

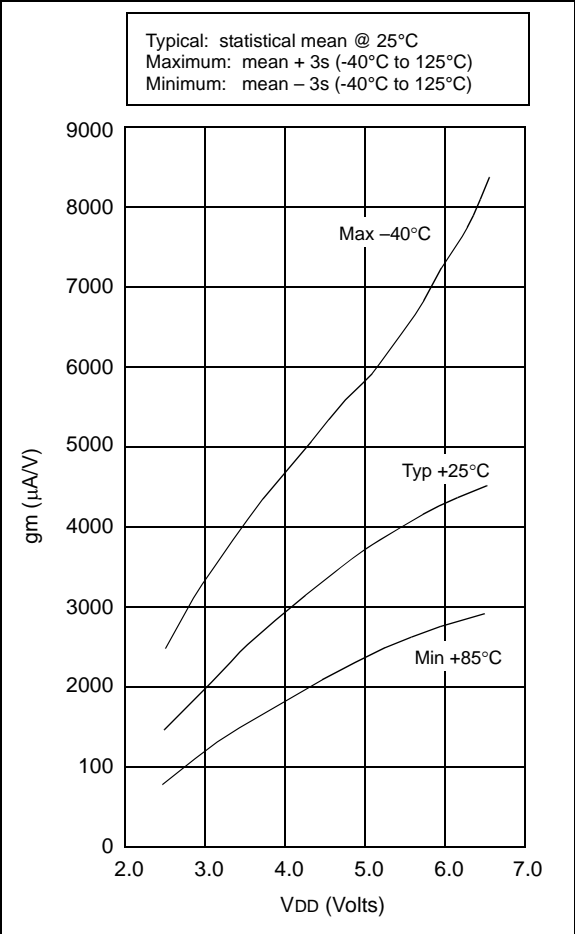


FIGURE 16-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF, 25°C

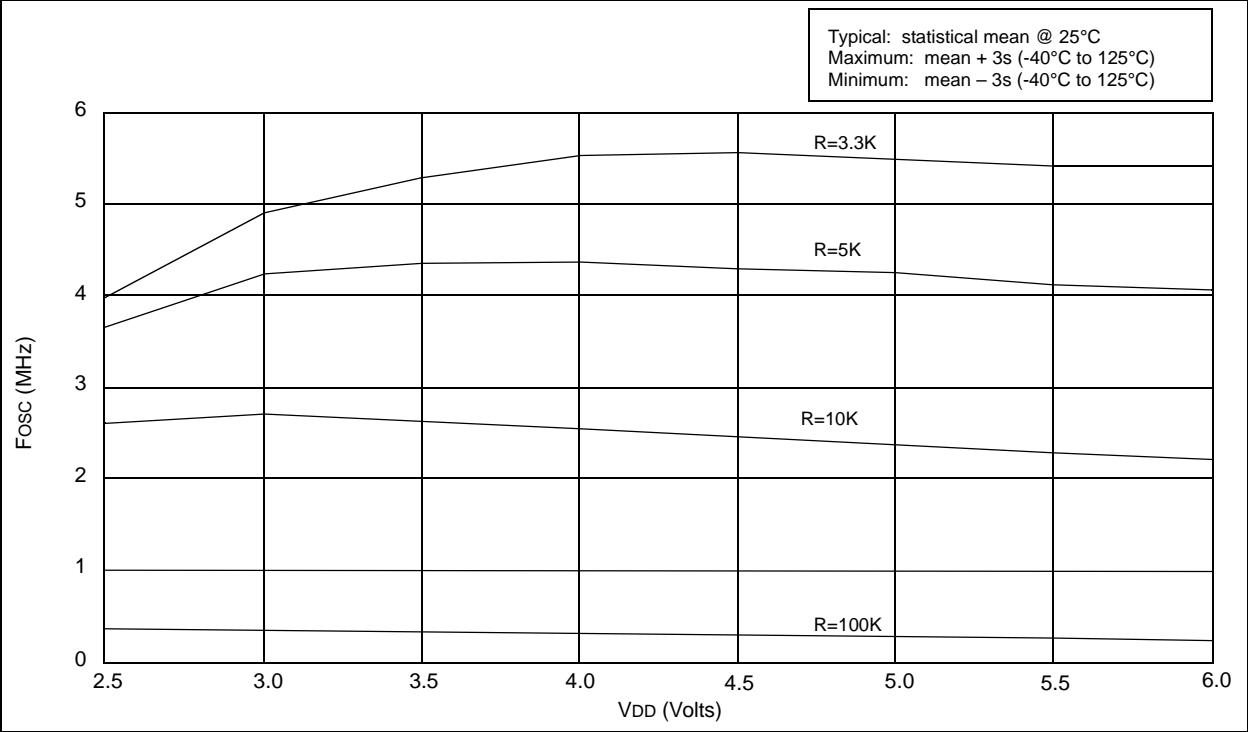
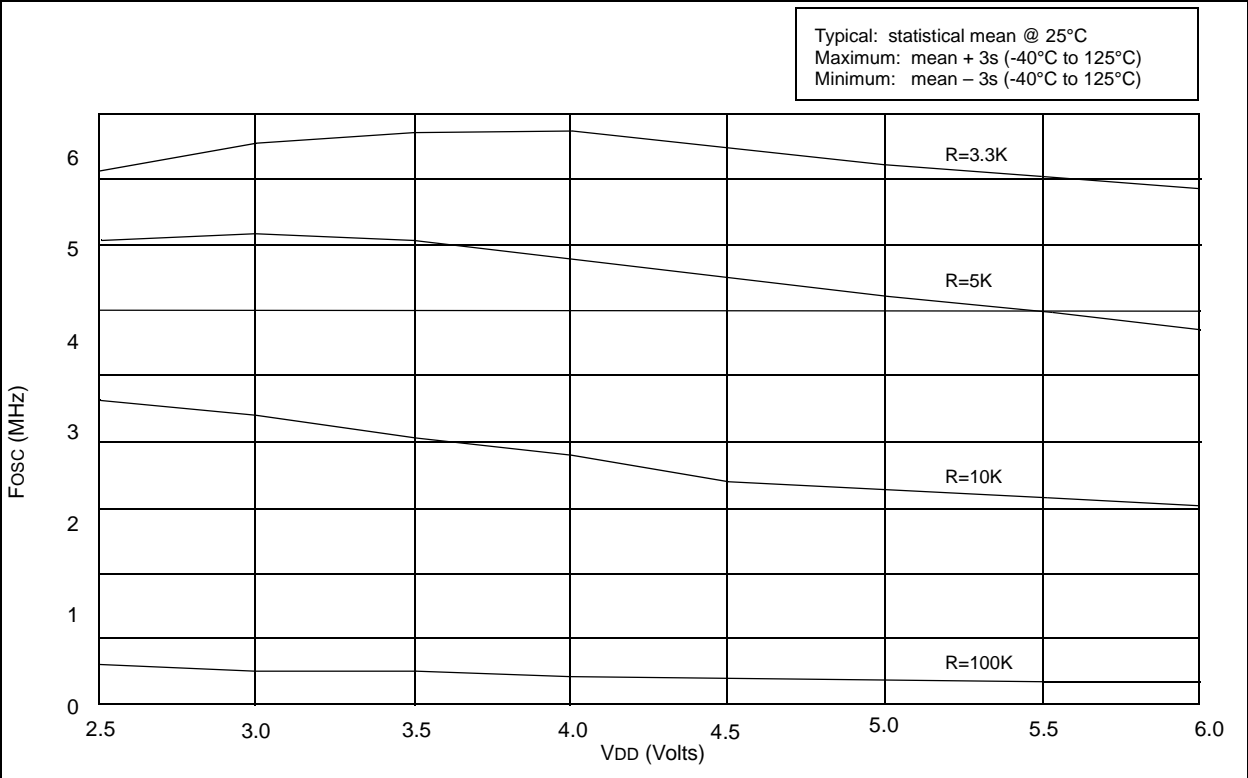


FIGURE 16-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF, 25°C



# PIC16C5X

FIGURE 16-5: TYPICAL I<sub>PD</sub> vs. V<sub>DD</sub>, WATCHDOG DISABLED (25°C)

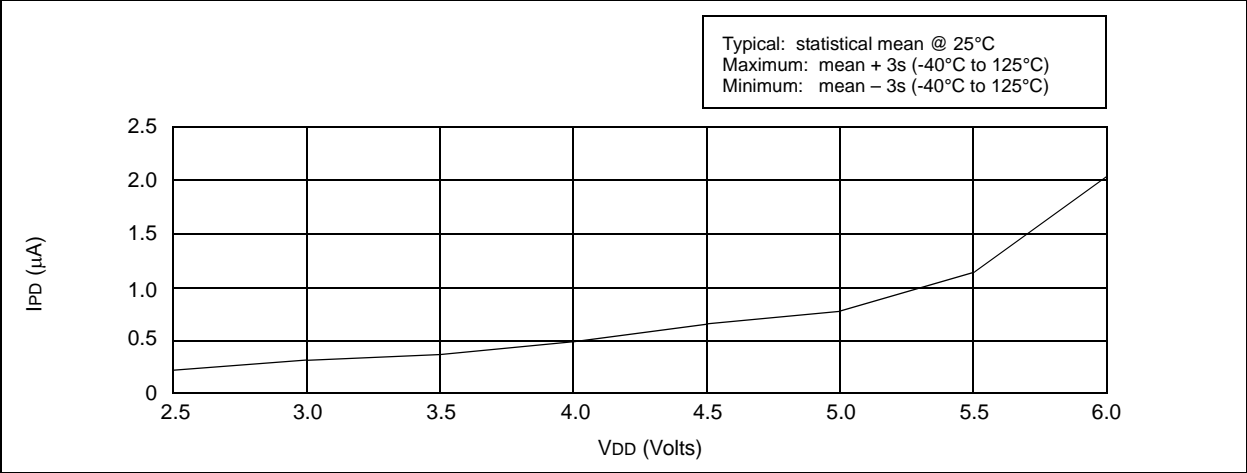
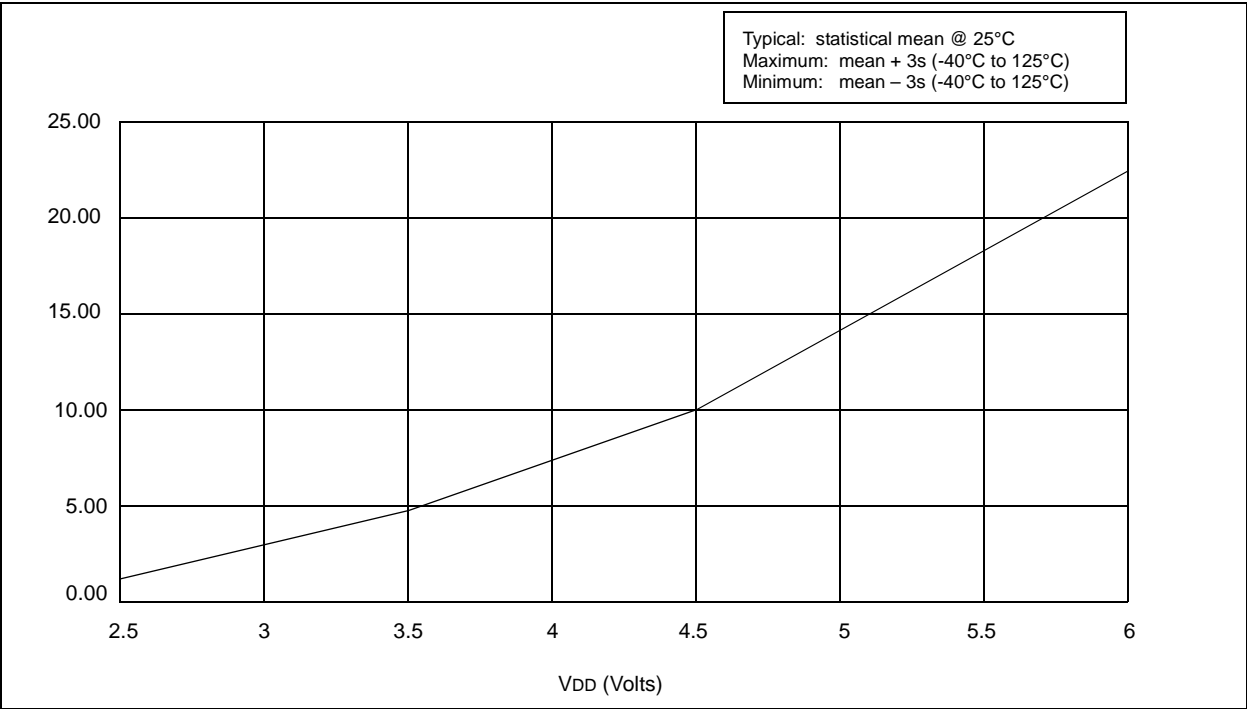


FIGURE 16-6: TYPICAL I<sub>PD</sub> vs. V<sub>DD</sub>, WATCHDOG ENABLED (25°C)



## 17.0 ELECTRICAL CHARACTERISTICS - PIC16LC54A

### Absolute Maximum Ratings<sup>(†)</sup>

Ambient temperature under bias .....	–55°C to +125°C
Storage temperature .....	–65°C to +150°C
Voltage on VDD with respect to VSS .....	0 to +7.5V
Voltage on MCLR with respect to VSS.....	0 to +14V
Voltage on all other pins with respect to VSS .....	–0.6V to (VDD + 0.6V)
Total power dissipation <sup>(1)</sup> .....	800 mW
Max. current out of Vss pin .....	150 mA
Max. current into VDD pin .....	100 mA
Max. current into an input pin (T0CKI only) .....	±500 µA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > VDD).....	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > VDD) .....	±20 mA
Max. output current sunk by any I/O pin .....	25 mA
Max. output current sourced by any I/O pin .....	20 mA
Max. output current sourced by a single I/O (Port A, B or C) .....	50 mA
Max. output current sunk by a single I/O (Port A, B or C).....	50 mA

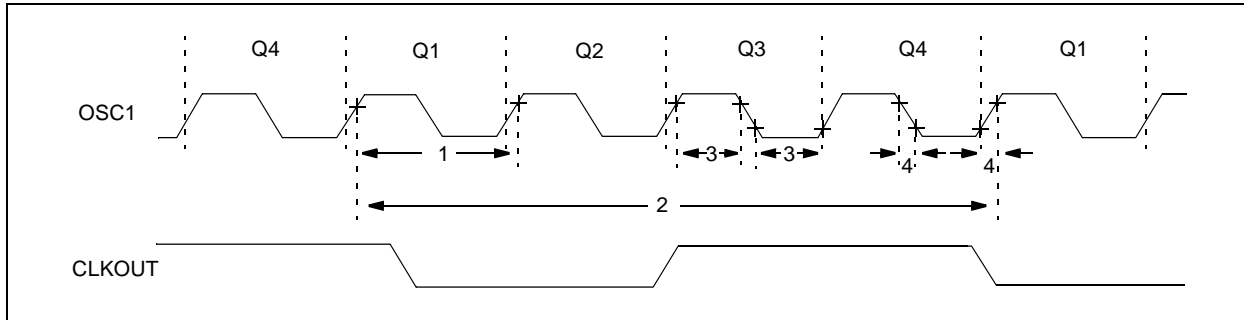
**Note 1:** Power dissipation is calculated as follows:  $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# PIC16C5X

## 17.5 Timing Diagrams and Specifications

**FIGURE 17-6: EXTERNAL CLOCK TIMING - PIC16C5X, PIC16CR5X**



**TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X**

<b>Standard Operating Conditions (unless otherwise specified)</b> Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended							
<b>AC Characteristics</b>							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency <sup>(1)</sup>	DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency <sup>(1)</sup>	DC	—	4.0	MHz	RC osc mode
			0.45	—	4.0	MHz	XT osc mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	20	MHz	HS osc mode (20)
			5.0	—	200	kHz	LP osc mode
1	TOSC	External CLKIN Period <sup>(1)</sup>	250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	μs	LP osc mode
		Oscillator Period <sup>(1)</sup>	250	—	—	ns	RC osc mode
			250	—	2,200	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	μs	LP osc mode

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF, 25°C

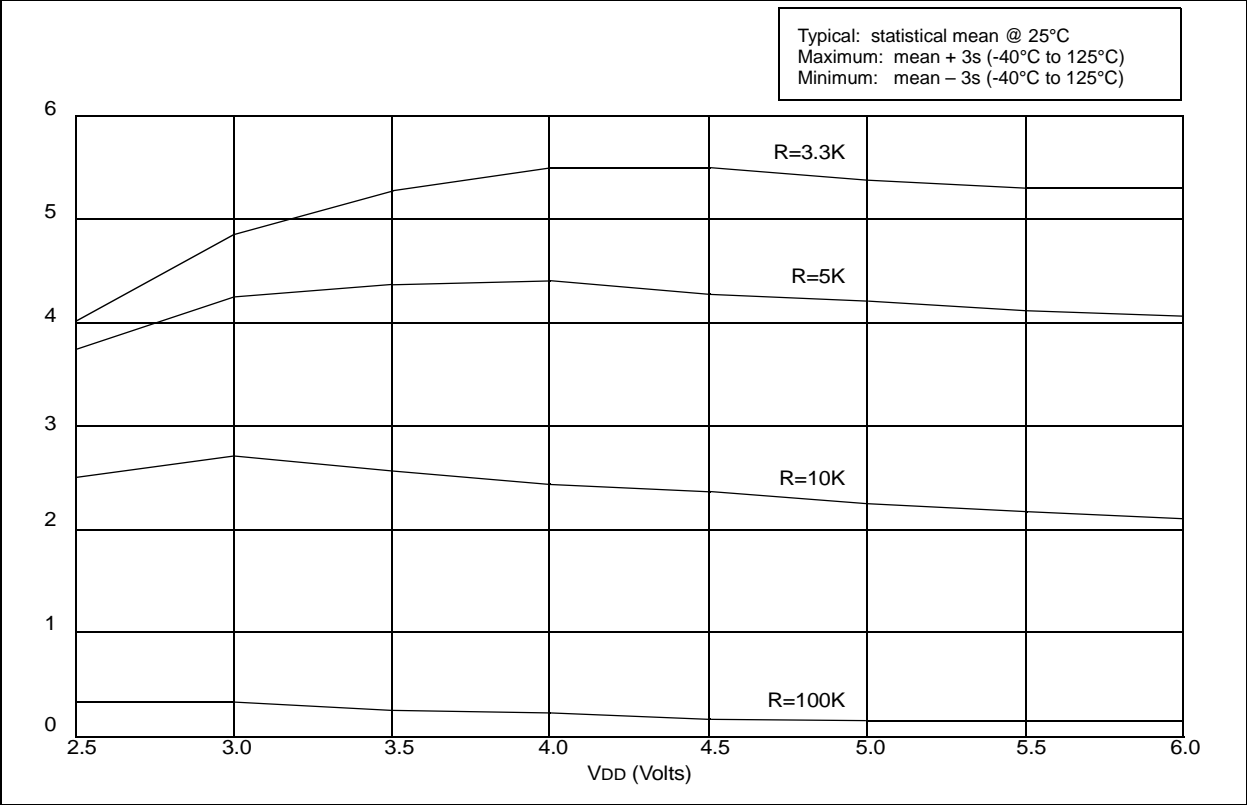


FIGURE 18-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF, 25°C

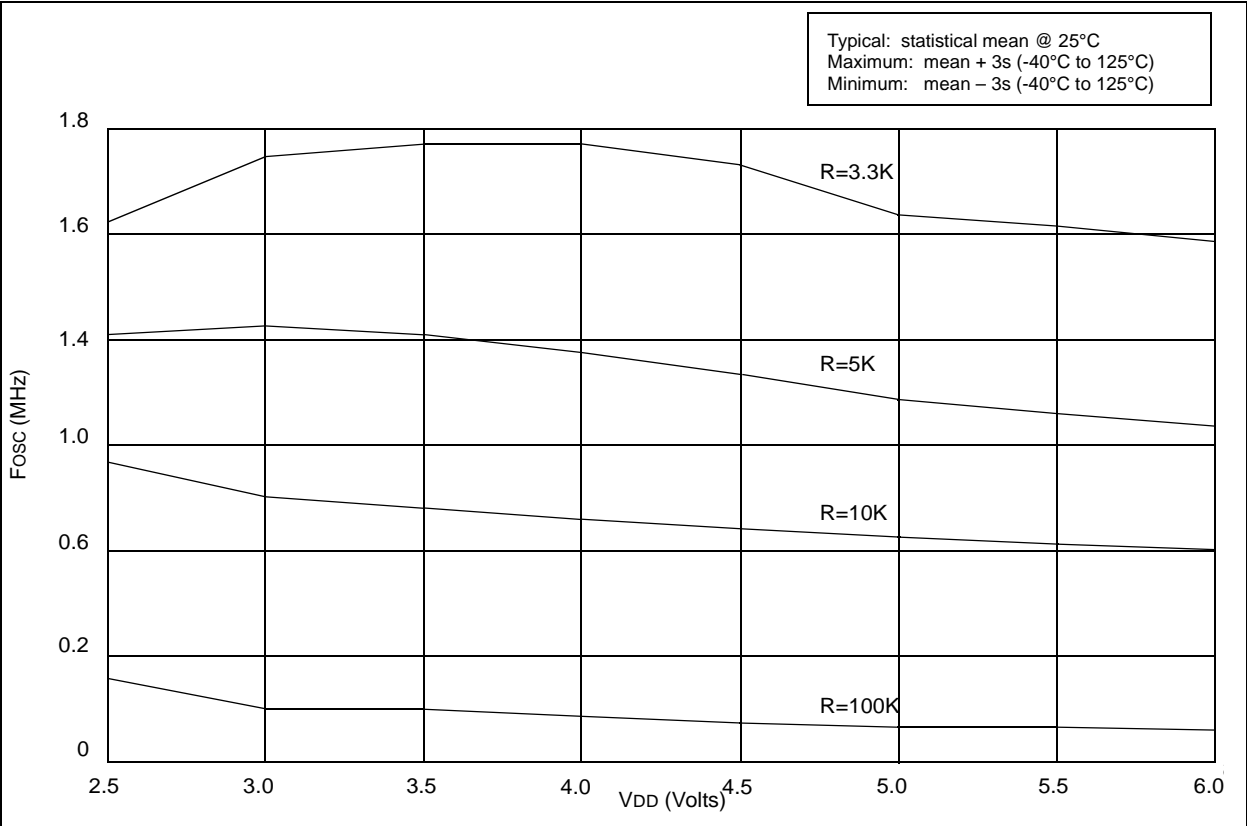


FIGURE 18-14: WDT TIMER TIME-OUT PERIOD vs. VDD<sup>(1)</sup>

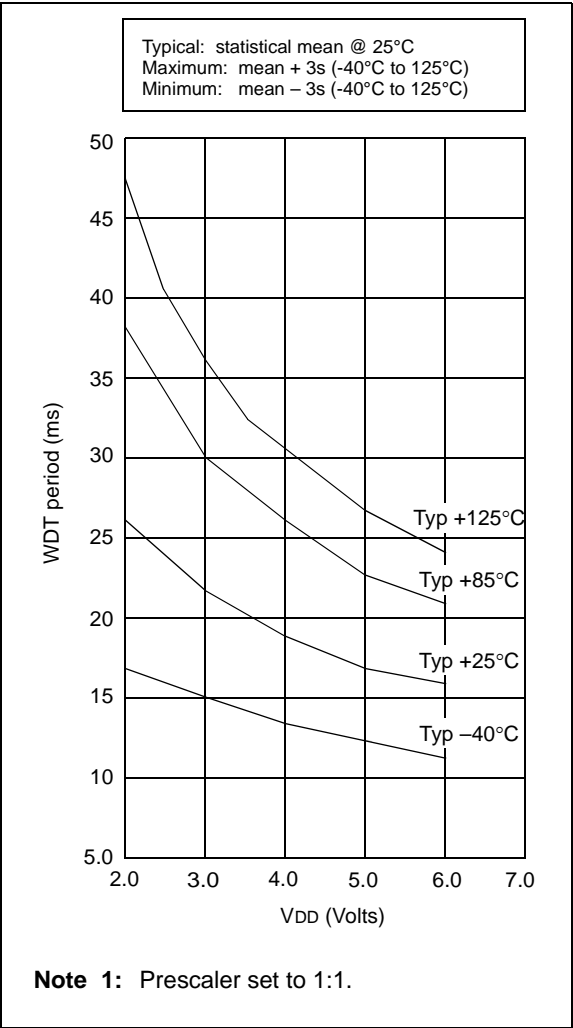


FIGURE 18-15: PORTA, B AND C I<sub>OH</sub> vs. V<sub>OH</sub>, VDD = 3 V

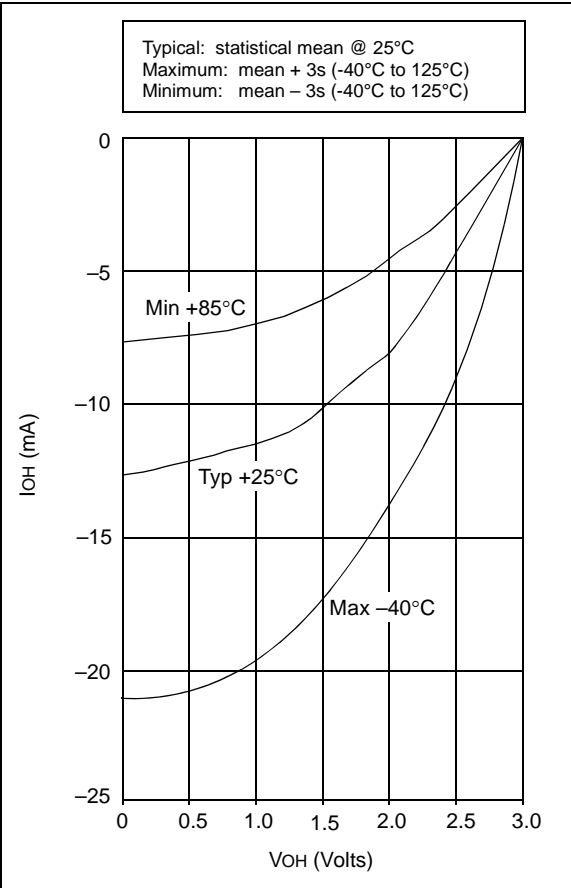


FIGURE 18-16: PORTA, B AND C  $I_{OH}$  vs.  $V_{OH}$ ,  $V_{DD} = 5\text{ V}$

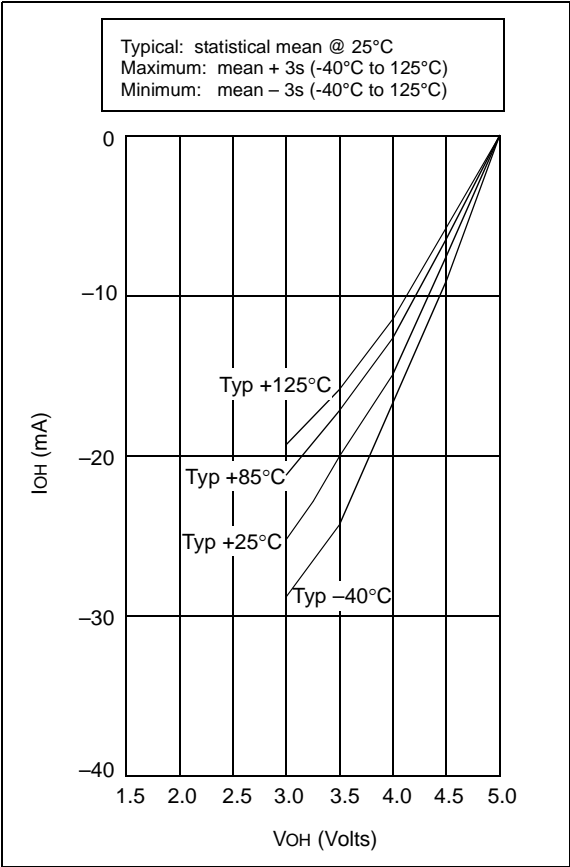
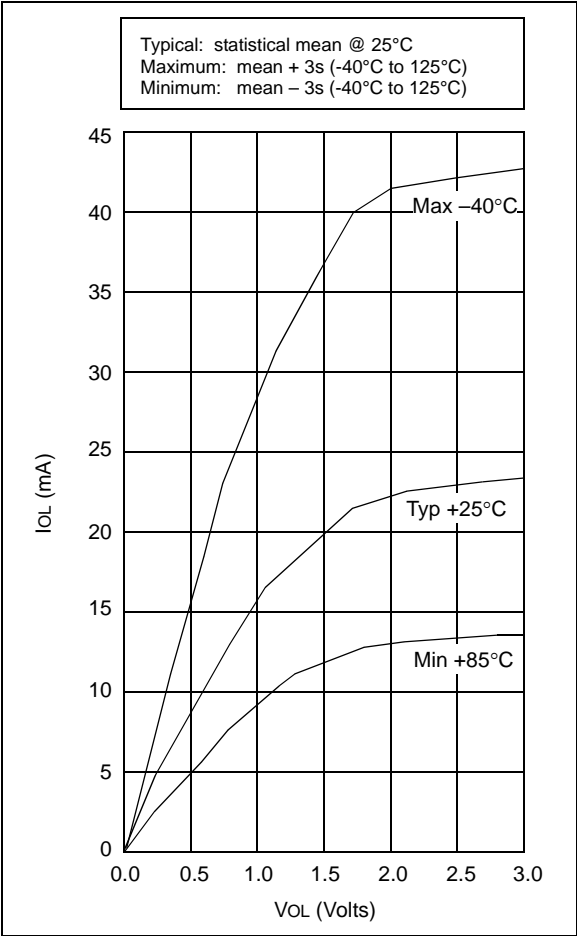


FIGURE 18-17: PORTA, B AND C  $I_{OL}$  vs.  $V_{OL}$ ,  $V_{DD} = 3\text{ V}$



## 19.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)<sup>(1)</sup>

PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature 0°C ≤ TA ≤ +70°C for commercial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	<b>Supply Voltage</b>	4.5	—	5.5	V	HS mode from 20 - 40 MHz
D002	VDR	<b>RAM Data Retention Voltage</b> <sup>(2)</sup>	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	<b>VDD Start Voltage</b> to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	<b>VDD Rise Rate</b> to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	<b>Supply Current</b> <sup>(3)</sup>	—	5.2 6.8	12.3 16	mA mA	FOSC = 40 MHz, VDD = 4.5V, HS mode FOSC = 40 MHz, VDD = 5.5V, HS mode
D020	IPD	<b>Power-down Current</b> <sup>(3)</sup>	—	1.8 9.8	7.0 27*	μA μA	VDD = 5.5V, WDT disabled, Commercial VDD = 5.5V, WDT enabled, Commercial

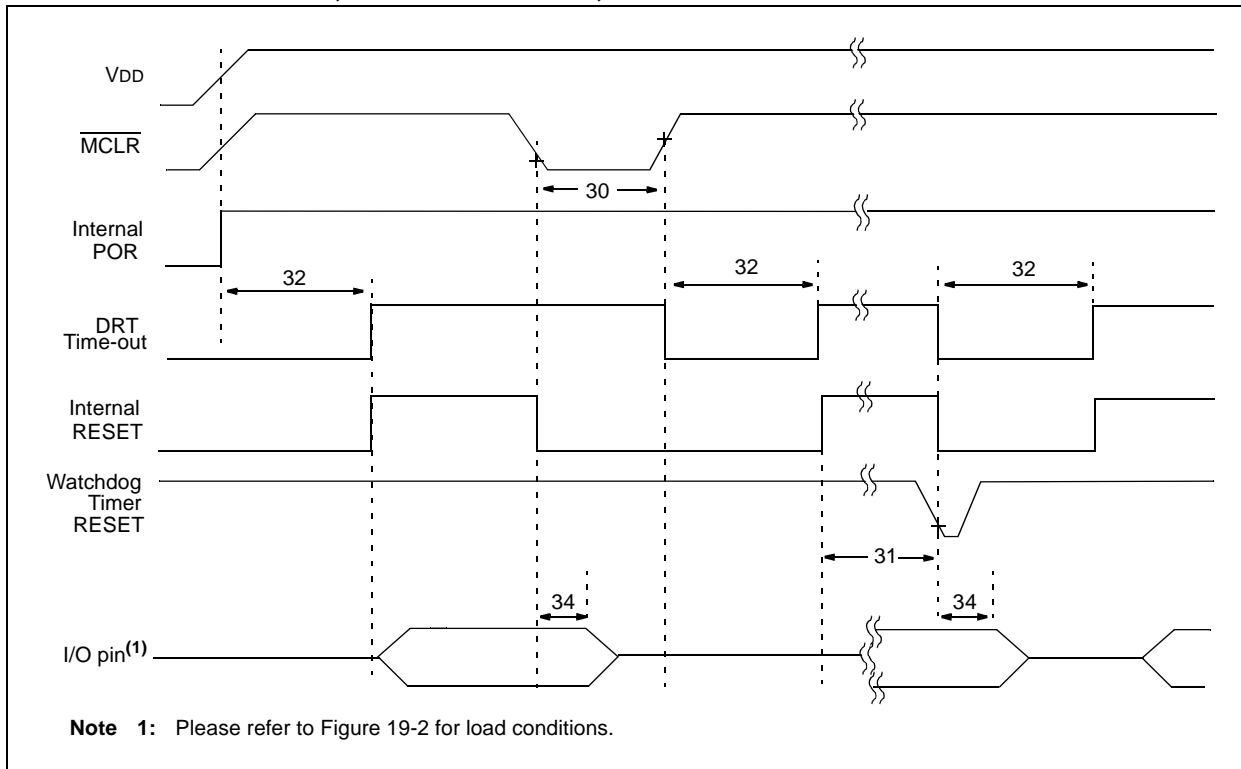
\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- Note 1:** Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected, HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 19.1.
- 2:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
- 3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
- The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
  - For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

# PIC16C5X

**FIGURE 19-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X-40**



**TABLE 19-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X-40**

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics							
Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial)							
Operating Voltage VDD range is described in Section 19.1.							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	1000*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns	

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.