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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57-xt-p

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NOTES:

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6.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 6-1).

The Special Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 6-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Details on Page
N/A	TRIS	I/O Control Registers (TRISA, TRISB, TRISC)								1111 1111	35
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								--11 1111	30
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32
01h	TMR0	Timer0 Module Register								xxxx xxxx	38
02h ⁽¹⁾	PCL	Low order 8 bits of PC								1111 1111	31
03h	STATUS	PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	29
04h	FSR	Indirect data memory address pointer								1xxx xxxx ⁽³⁾	32
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	35
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	35
07h ⁽²⁾	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	35

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 6.5 for an explanation of how to access these bits.

2: File address 07h is a General Purpose Register on the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58 and PIC16CR58.

3: These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for $\overline{MCLR}$ and WDT Reset, the value is 111u uuuu.

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6.5.1 PAGING CONSIDERATIONS – PIC16C56/CR56, PIC16C57/CR57 AND PIC16C58/CR58

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS Register will not be updated. Therefore, the next `GOTO`, `CALL` or modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA<1:0>).

For example, a `NOP` at location 1FFh (page 0) increments the PC to 200h (page 1). A `GOTO xxx` at 200h will return the program to address xxh on page 0 (assuming that PA<1:0> are clear).

To prevent this, the page preselect bits must be updated under program control.

6.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the RESET vector).

The STATUS Register page preselect bits are cleared upon a RESET, which means that page 0 is preselected.

Therefore, upon a RESET, a `GOTO` instruction at the RESET vector location will automatically cause the program to jump to page 0.

6.6 Stack

PIC16C5X devices have a 10-bit or 11-bit wide, two-level hardware push/pop stack.

A `CALL` instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential `CALL`'s are executed, only the most recent two return addresses are stored.

A `RETLW` instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential `RETLW`'s are executed, the stack will be filled with the address previously stored in level 2. Note that the W Register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the `RETLW` instruction, the PC is loaded with the Top of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC, therefore, paging is not an issue when returning from a subroutine.

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NOTES:

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13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 PIC16LCR54A-04I (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
PIC16CR54A-04, 10, 20 PIC16CR54A-04I, 10I, 20I (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
D001	V _{DD}	Supply Voltage					
		PIC16LCR54A	2.0	—	6.25	V	
		PIC16CR54A	2.5	—	6.25	V	RC and XT modes
D001A			4.5	—	5.5	V	HS mode
D002	V _{DR}	RAM Data Retention Voltage⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	V _{POR}	V_{DD} Start Voltage to ensure Power-on Reset	—	V _{SS}	—	V	See Section 5.1 for details on Power-on Reset
D004	S _{VDD}	V_{DD} Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D005	I _{DD}	Supply Current⁽²⁾					
		PICLCR54A	—	10	20	μA	F _{OSC} = 32 kHz, V _{DD} = 2.0V
			—	—	70	μA	F _{OSC} = 32 kHz, V _{DD} = 6.0V
D005A		PIC16CR54A	—	2.0	3.6	mA	RC⁽³⁾ and XT modes: F _{OSC} = 4.0 MHz, V _{DD} = 6.0V F _{OSC} = 4.0 MHz, V _{DD} = 3.0V F _{OSC} = 200 kHz, V _{DD} = 2.5V HS mode: F _{OSC} = 10 MHz, V _{DD} = 5.5V F _{OSC} = 20 MHz, V _{DD} = 5.5V
			—	0.8	1.8	mA	
			—	90	350	μA	
			—	4.8	10	mA	
			—	9.0	20	mA	

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all I_{DD} measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS}, T0CKI = V_{DD}, MCLR = V_{DD}; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through R_{EXT}. The current through the resistor can be estimated by the formula: I_R = V_{DD}/2R_{EXT} (mA) with R_{EXT} in kΩ.

PIC16C5X

FIGURE 13-3: CLKOUT AND I/O TIMING - PIC16CR54A

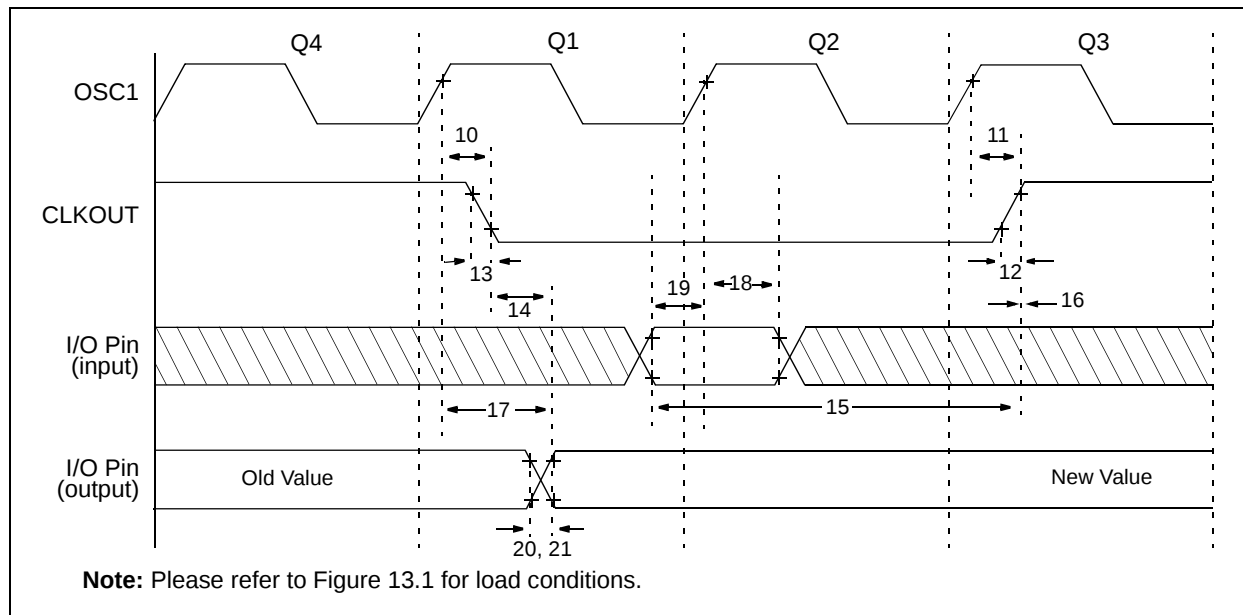


TABLE 13-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR54A

AC Characteristics		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature				
		0°C ≤ TA ≤ +70°C for commercial				
		-40°C ≤ TA ≤ +85°C for industrial				
		-40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽¹⁾	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ ⁽¹⁾	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽²⁾	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽²⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

Note 2: Please refer to Figure 13.1 for load conditions.

FIGURE 16-20: PORTA, B AND C I_{OH} vs. V_{OH} , $V_{DD} = 3V$

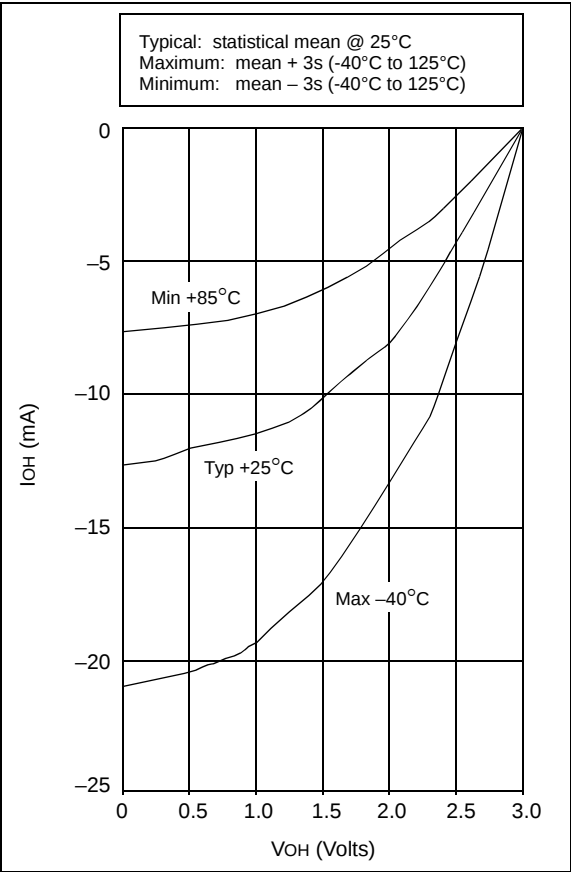
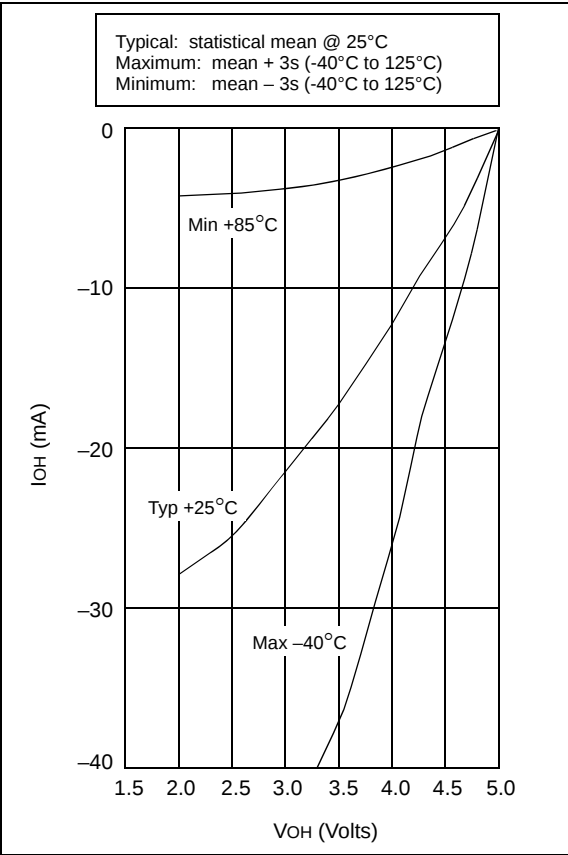


FIGURE 16-21: PORTA, B AND C I_{OH} vs. V_{OH} , $V_{DD} = 5V$



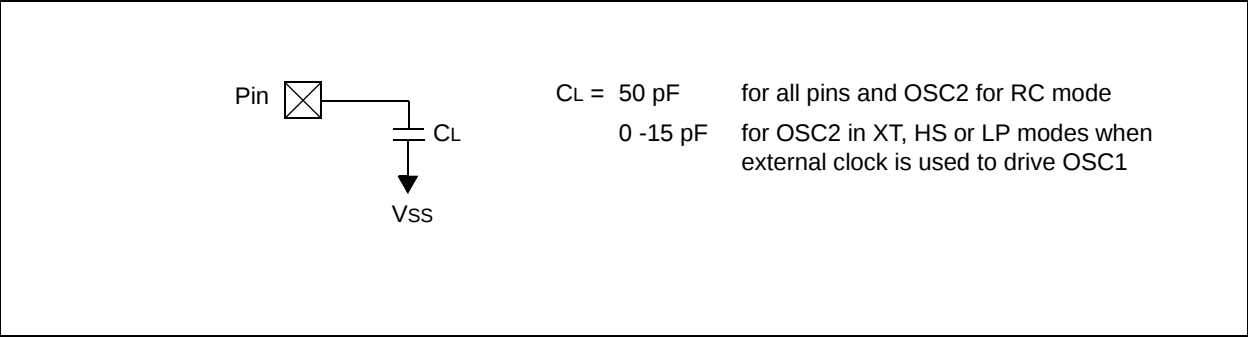
17.4 Timing Parameter Symbolology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T			
F	Frequency	T	Time
Lowercase letters (pp) and their meanings:			
pp		mc	MCLR
2	to	osc	oscillator
ck	CLKOUT	os	OSC1
cy	cycle time	t0	T0CKI
drt	device reset timer	wdt	watchdog timer
io	I/O port		
Uppercase letters and their meanings:			
S		P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	Hi-impedance
L	Low		

FIGURE 17-5: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B-04, 20



PIC16C5X

17.5 Timing Diagrams and Specifications

FIGURE 17-6: EXTERNAL CLOCK TIMING - PIC16C5X, PIC16CR5X

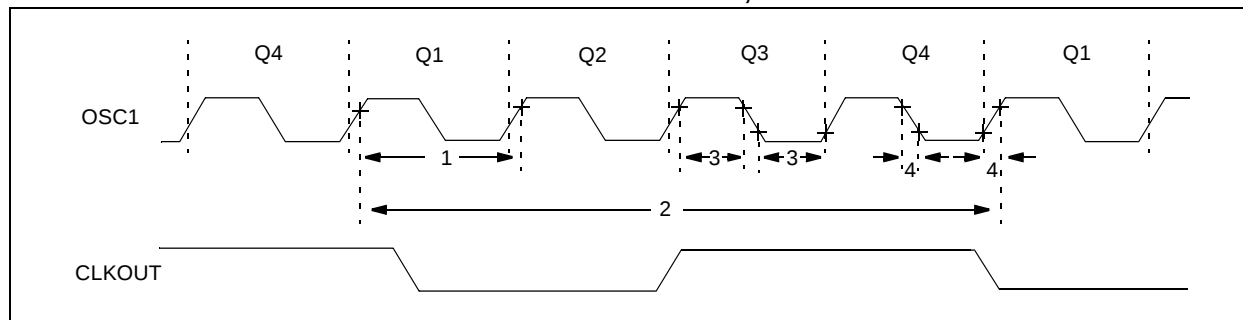


TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended							
AC Characteristics							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	External CLKIN Frequency ⁽¹⁾	DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency ⁽¹⁾	DC	—	4.0	MHz	RC osc mode
			0.45	—	4.0	MHz	XT osc mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	20	MHz	HS osc mode (20)
			5.0	—	200	kHz	LP osc mode
1	Tosc	External CLKIN Period ⁽¹⁾	250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	μs	LP osc mode
		Oscillator Period ⁽¹⁾	250	—	—	ns	RC osc mode
			250	—	2,200	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	μs	LP osc mode

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

PIC16C5X

FIGURE 17-7: CLKOUT AND I/O TIMING - PIC16C5X, PIC16CR5X

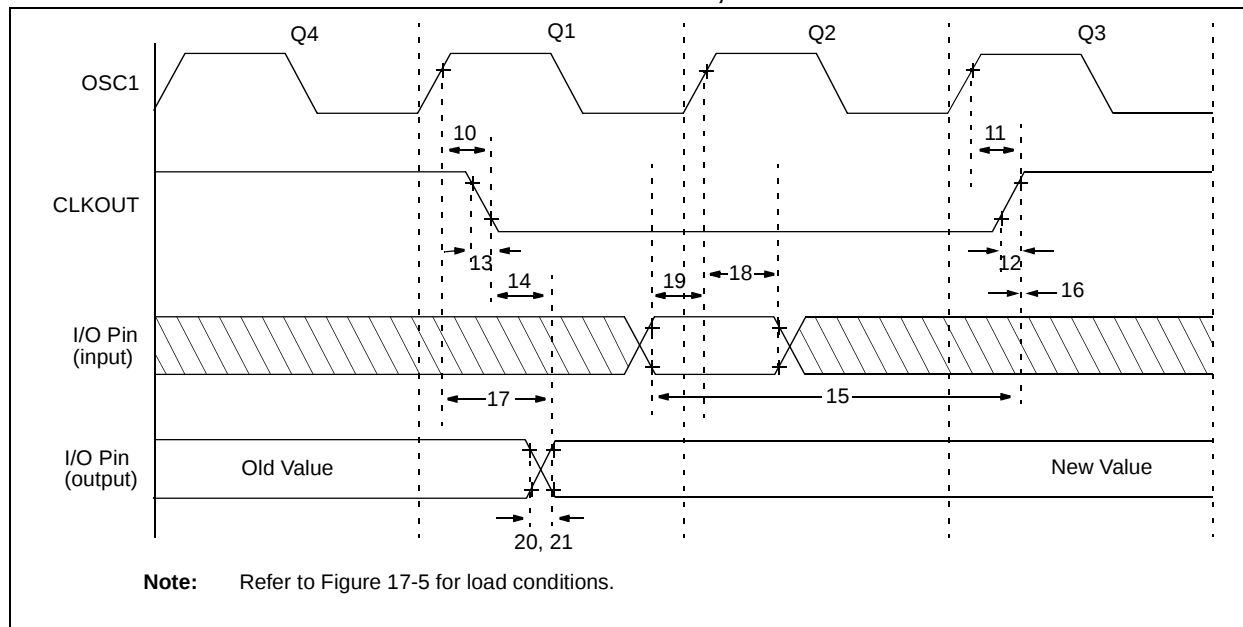


TABLE 17-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽¹⁾	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ ⁽¹⁾	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽²⁾	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽²⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

2: Refer to Figure 17-5 for load conditions.

FIGURE 17-8: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X, PIC16CR5X

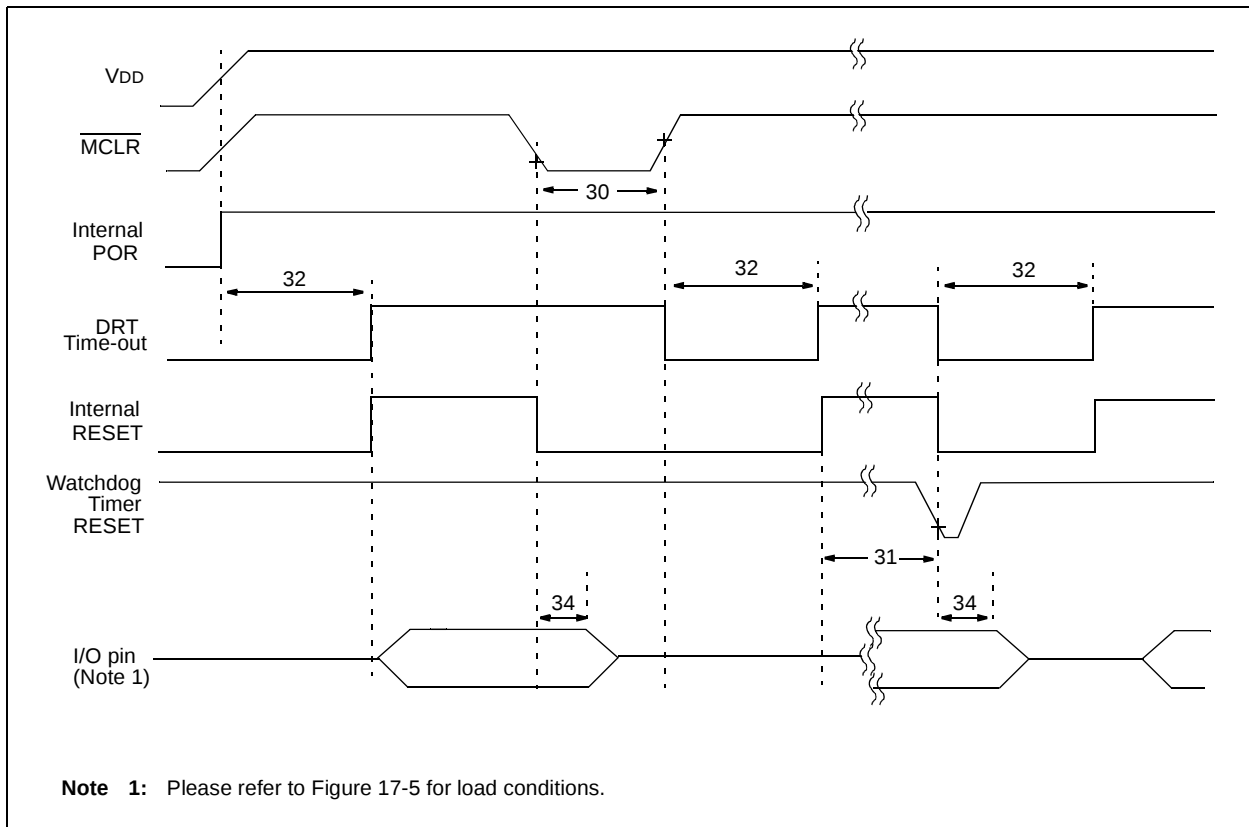


TABLE 17-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X, PIC16CR5X

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics		Operating Temperature					
		0°C ≤ TA ≤ +70°C for commercial					
		-40°C ≤ TA ≤ +85°C for industrial					
		-40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	1000*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. V_{DD} , $C_{EXT} = 300$ pF, 25°C

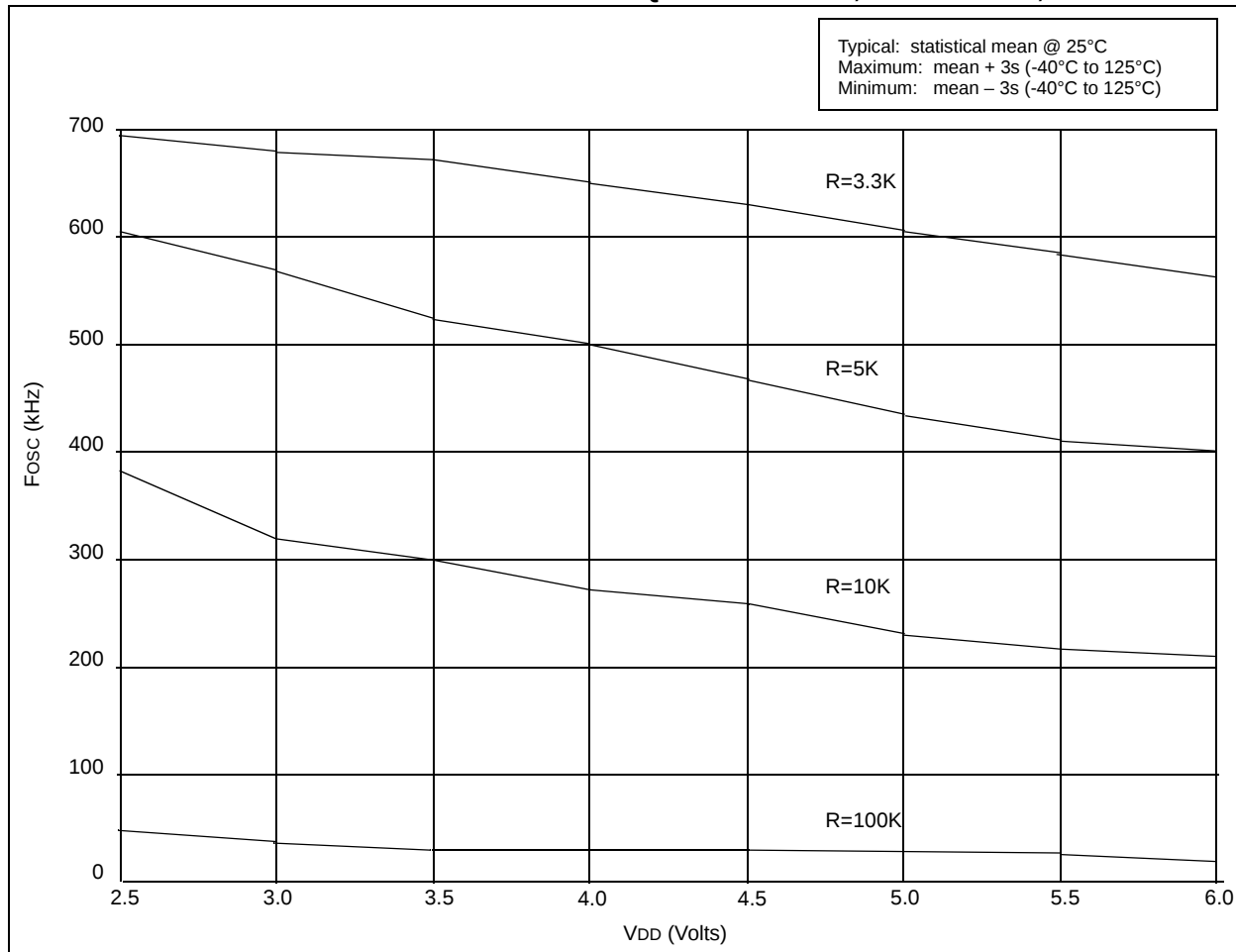
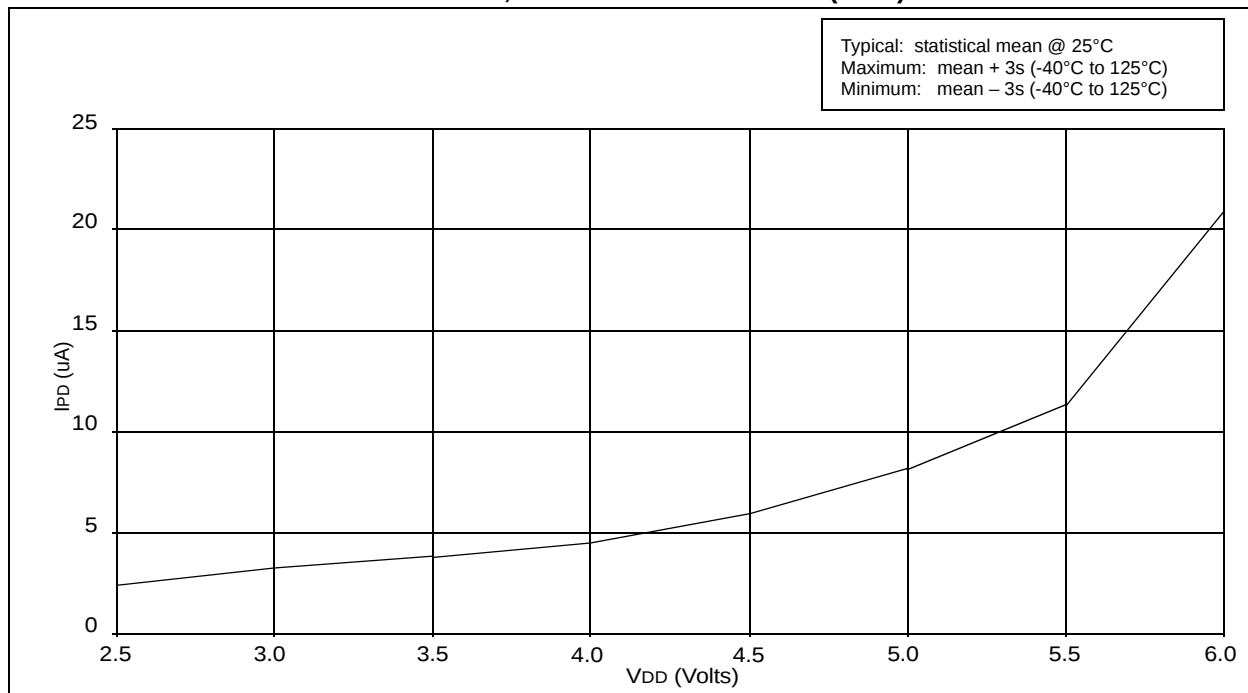
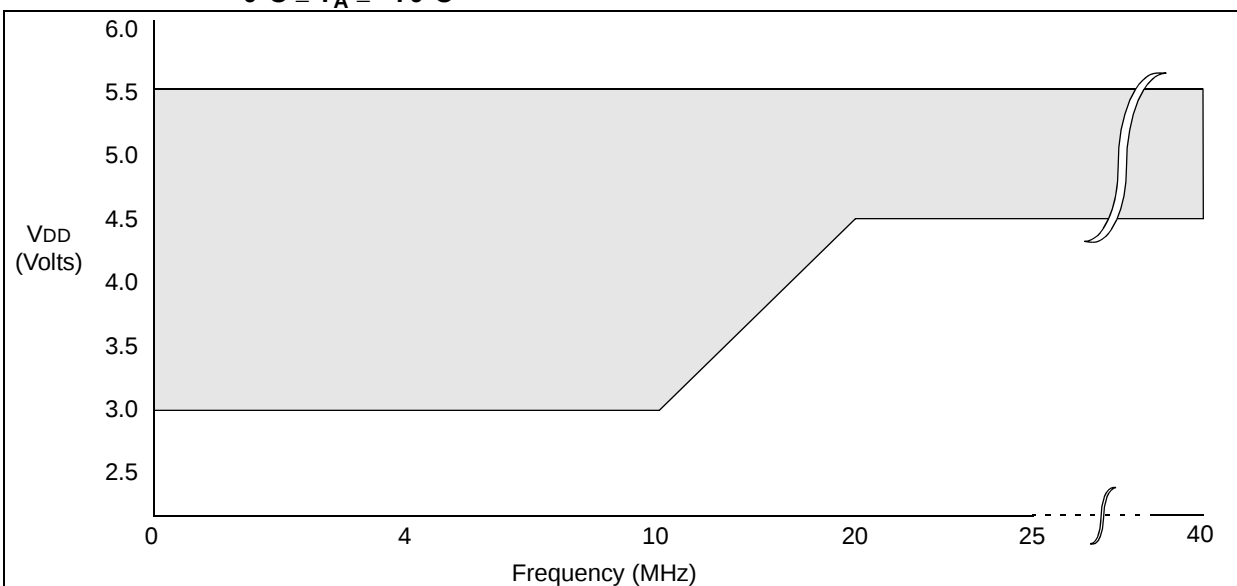


FIGURE 18-5: TYPICAL I_{PD} vs. V_{DD} , WATCHDOG DISABLED (25°C)



PIC16C5X

FIGURE 19-1: PIC16C54C/C55A/C56A/C57C/C58B-40 VOLTAGE-FREQUENCY GRAPH, $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$

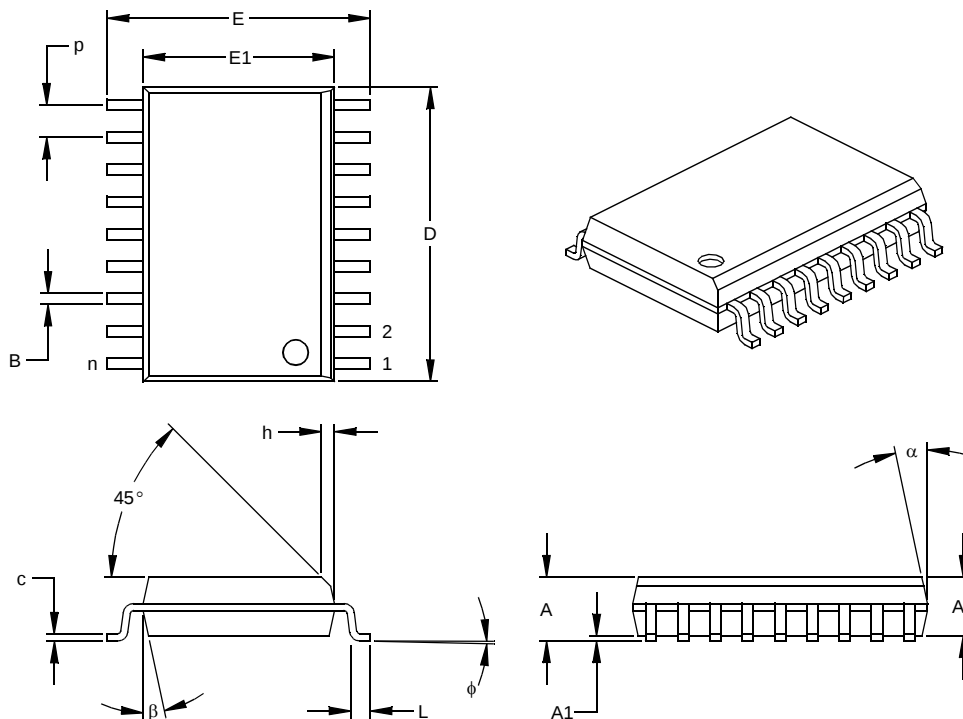


- Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.
- 2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
- 3:** Operation between 20 to 40 MHz requires the following:
- VDD between 4.5V. and 5.5V
 - OSC1 externally driven
 - OSC2 not connected
 - HS mode
 - Commercial temperatures
- Devices qualified for 40 MHz operation have -40 designation (ex: PIC16C54C-40/P).
- 4:** For operation between DC and 20 MHz, see Section 17.1.

PIC16C5X

18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-013

Drawing No. C04-051

APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

1. Check any `CALL`, `GOTO` or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
4. Verify all writes to `STATUS`, `OPTION`, and `FSR` registers since these have changed.
5. Change `RESET` vector to proper value for processor used.
6. Remove any use of the `ADDLW`, `RETURN` and `SUBLW` instructions.
7. Rewrite any code segments that use interrupts.

APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.

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PIC16C5X

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-	XX	X	/XX	XXX
Device		Frequency Range/OSC Type	Temperature Range	Package	Pattern
Device		PIC16C54 PIC16C54A PIC16CR54A PIC16C54C PIC16CR54C PIC16C55 PIC16C55A PIC16C56 PIC16C56A PIC16CR56A PIC16C57 PIC16C57C PIC16CR57C PIC16C58B PIC16CR58B	PIC16C54T ⁽²⁾ PIC16C54AT ⁽²⁾ PIC16CR54AT ⁽²⁾ PIC16C54CT ⁽²⁾ PIC16CR54CT ⁽²⁾ PIC16C55T ⁽²⁾ PIC16C55AT ⁽²⁾ PIC16C56T ⁽²⁾ PIC16C56AT ⁽²⁾ PIC16CR56AT ⁽²⁾ PIC16C57T ⁽²⁾ PIC16C57CT ⁽²⁾ PIC16CR57CT ⁽²⁾ PIC16C58BT ⁽²⁾ PIC16CR58BT ⁽²⁾		
Frequency Range/ Oscillator Type		RC Resistor Capacitor LP Low Power Crystal XT Standard Crystal/Resonator HS High Speed Crystal 02 200 KHz (LP) or 2 MHz (XT and RC) 04 200 KHz (LP) or 4 MHz (XT and RC) 10 10 MHz (HS only) 20 20 MHz (HS only) 40 40 MHz (HS only) b ⁽⁴⁾ No oscillator type for JW packages ⁽³⁾			
		*RC/LP/XT/HS are for 16C54/55/56/57 devices only -02 is available for 16LV54A only -04/10/20 options are available for all other devices -40 is available for 16C54C/55A/56A/57C/58B devices only			
Temperature Range		b ⁽⁴⁾ = 0°C to +70°C I = -40°C to +85°C E = -40°C to +125°C			
Package		S = Die in Waffle Pack JW = 28-pin 600 mil/18-pin 300 mil windowed CER-DIP ⁽³⁾ P = 28-pin 600 mil/18-pin 300 mil PDIP SO = 300 mil SOIC SS = 209 mil SSOP SP = 28-pin 300 mil Skinny PDIP			
		*See Section 21 for additional package information.			
Pattern		QTP, SQTP, ROM code (factory specified) or Special Requirements. Blank for OTP and Windowed devices.			

Examples:

- PIC16C55A - 04/P 301 = Commercial Temp., PDIP package, 4 MHz, standard V_{DD} limits, QTP pattern #301
- PIC16LC54C - 04I/SO Industrial Temp., SOIC package, 200 kHz, extended V_{DD} limits
- PIC16C57 - RC/SP = RC Oscillator, commercial temp, skinny PDIP package, 4 MHz, standard V_{DD} limits
- PIC16C58BT -40/SS 123 = commercial temp, SSOP package in tape and reel, 4 MHz, extended V_{DD} limits, ROM pattern #123

- Note 1:** C = normal voltage range
LC = extended
- Note 2:** T = in tape and reel - SOIC and SSOP packages only
- Note 3:** JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirements of each oscillator type, including LC devices.
- Note 4:** b = Blank

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

- Your local Microchip sales office
- The Microchip Worldwide Site (www.microchip.com)

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