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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3.25V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57-xte-p



PIC16C5X

8-Bit EPROM/ROM-Based CMOS Microcontrollers

1.0 GENERAL DESCRIPTION

The PIC16C5X from Microchip Technology is a family of low cost, high performance, 8-bit fully static, EPROM/ROM-based CMOS microcontrollers. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle except for program branches which take two cycles. The PIC16C5X delivers performance in an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C5X products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external RESET circuitry. There are four oscillator configurations to choose from, including the power saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and Code Protection features improve system cost, power and reliability.

The UV erasable Cerdip packaged versions are ideal for code development, while the cost effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers, while benefiting from the OTP's flexibility.

The PIC16C5X products are supported by a full featured macro assembler, a software simulator, an in-circuit emulator, a low cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC16C5X series fits perfectly in applications ranging from high speed automotive and appliance motor control to low power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customizing application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low cost, low power, high performance ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, co-processor applications).

6.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the \overline{TO} and \overline{PD} bits are not

writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS Register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 10.0, Instruction Set Summary.

REGISTER 6-1: STATUS REGISTER (ADDRESS: 03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
PA2	PA1	PA0	\overline{TO}	\overline{PD}	Z	DC	C
bit 7			bit 0				

bit 7: **PA2:** This bit unused at this time.

Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

bit 6-5: **PA<1:0>:** Program page preselect bits (PIC16C56/CR56)(PIC16C57/CR57)(PIC16C58/CR58)

00 = Page 0 (000h - 1FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58

01 = Page 1 (200h - 3FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58

10 = Page 2 (400h - 5FFh) - PIC16C57/CR57, PIC16C58/CR58

11 = Page 3 (600h - 7FFh) - PIC16C57/CR57, PIC16C58/CR58

Each page is 512 words.

Using the PA<1:0> bits as general purpose read/write bits in devices which do not use them for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: **\overline{TO} :** Time-out bit

1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction

0 = A WDT time-out occurred

bit 3: **\overline{PD} :** Power-down bit

1 = After power-up or by the `CLRWDT` instruction

0 = By execution of the `SLEEP` instruction

bit 2: **Z:** Zero bit

1 = The result of an arithmetic or logic operation is zero

0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC:** Digit carry/borrow bit (for `ADDWF` and `SUBWF` instructions)

ADDWF

1 = A carry from the 4th low order bit of the result occurred

0 = A carry from the 4th low order bit of the result did not occur

SUBWF

1 = A borrow from the 4th low order bit of the result did not occur

0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C:** Carry/borrow bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

ADDWF

1 = A carry occurred

0 = A carry did not occur

SUBWF

1 = A borrow did not occur

0 = A borrow occurred

RRF or RLF

Loaded with LSb or MSb, respectively

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

1 = bit is set

0 = bit is cleared

x = bit is unknown

8.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 9.2.1). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1,x, etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

8.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 8-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 8-1: CHANGING PRESCALER (TIMER0→WDT)

```
CLRWDT          ;Clear WDT
CLRF    TMR0     ;Clear TMR0 & Prescaler
MOVLW  B'00xx1111' ;Last 3 instructions in
                    this example
OPTION          ;are required only if
                ;desired
CLRWDT          ;PS<2:0> are 000 or
                ;001
MOVLW  B'00xx1xxx' ;Set Prescaler to
OPTION          ;desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 8-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

EXAMPLE 8-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT          ;Clear WDT and
                ;prescaler
MOVLW  B'xxxx0xxx' ;Select TMR0, new
                    ;prescale value and
                    ;clock source
OPTION
```

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TABLE 10-2: INSTRUCTION SET SUMMARY

Mnemonic, Operands		Description	Cycles	12-Bit Opcode			Status Affected	Notes
				MSb	LSb			
ADDWF	f, d	Add W and f	1	0001	11df	ffff	C, DC, Z	1, 2, 4
ANDWF	f, d	AND W with f	1	0001	01df	ffff	Z	2, 4
CLRF	f	Clear f	1	0000	011f	ffff	Z	4
CLRW	—	Clear W	1	0000	0100	0000	Z	
COMF	f, d	Complement f	1	0010	01df	ffff	Z	
DECF	f, d	Decrement f	1	0000	11df	ffff	Z	2, 4
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	0010	11df	ffff	None	2, 4
INCF	f, d	Increment f	1	0010	10df	ffff	Z	2, 4
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	0011	11df	ffff	None	2, 4
IORWF	f, d	Inclusive OR W with f	1	0001	00df	ffff	Z	2, 4
MOVF	f, d	Move f	1	0010	00df	ffff	Z	2, 4
MOVWF	f	Move W to f	1	0000	001f	ffff	None	1, 4
NOP	—	No Operation	1	0000	0000	0000	None	
RLF	f, d	Rotate left f through Carry	1	0011	01df	ffff	C	2, 4
RRF	f, d	Rotate right f through Carry	1	0011	00df	ffff	C	2, 4
SUBWF	f, d	Subtract W from f	1	0000	10df	ffff	C, DC, Z	1, 2, 4
SWAPF	f, d	Swap f	1	0011	10df	ffff	None	2, 4
XORWF	f, d	Exclusive OR W with f	1	0001	10df	ffff	Z	2, 4
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	0100	bbbf	ffff	None	2, 4
BSF	f, b	Bit Set f	1	0101	bbbf	ffff	None	2, 4
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	0110	bbbf	ffff	None	
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	0111	bbbf	ffff	None	
LITERAL AND CONTROL OPERATIONS								
ANDLW	k	AND literal with W	1	1110	kkkk	kkkk	Z	1
CALL	k	Call subroutine	2	1001	kkkk	kkkk	None	
CLRWDT	k	Clear Watchdog Timer	1	0000	0000	0100	TO, PD	
GOTO	k	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW	k	Inclusive OR Literal with W	1	1101	kkkk	kkkk	Z	
MOVLW	k	Move Literal to W	1	1100	kkkk	kkkk	None	
OPTION	k	Load OPTION register	1	0000	0000	0010	None	
RETLW	k	Return, place Literal in W	2	1000	kkkk	kkkk	None	
SLEEP	—	Go into standby mode	1	0000	0000	0011	TO, PD	
TRIS	f	Load TRIS register	1	0000	0000	0fff	None	3
XORLW	k	Exclusive OR Literal to W	1	1111	kkkk	kkkk	Z	

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO (see Section 6.5 for more on program counter).

- When an I/O register is modified as a function of itself (e.g. `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- The instruction `TRIS f`, where $f = 5, 6$ or 7 causes the contents of the W register to be written to the tristate latches of PORTA, B or C respectively. A '1' forces the pin to a hi-impedance state and disables the output buffers.
- If this instruction is executed on the TMR0 register (and, where applicable, $d = 1$), the prescaler will be cleared (if assigned to TMR0).

ADDWF Add W and f

Syntax: [*label*] ADDWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) + (f) \rightarrow (\text{dest})$

Status Affected: C, DC, Z

Encoding:

0001	11df	ffff
------	------	------

Description: Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: ADDWF TEMP_REG, 0

Before Instruction

W = 0x17
TEMP_REG = 0xC2

After Instruction

W = 0xD9
TEMP_REG = 0xC2

ANDWF AND W with f

Syntax: [*label*] ANDWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) .\text{AND}. (f) \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

0001	01df	ffff
------	------	------

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: ANDWF TEMP_REG, 1

Before Instruction

W = 0x17
TEMP_REG = 0xC2

After Instruction

W = 0x17
TEMP_REG = 0x02

ANDLW AND literal with W

Syntax: [*label*] ANDLW k

Operands: $0 \leq k \leq 255$

Operation: $(W) .\text{AND}. (k) \rightarrow (W)$

Status Affected: Z

Encoding:

1110	kkkk	kkkk
------	------	------

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: ANDLW H'5F'

Before Instruction

W = 0xA3

After Instruction

W = 0x03

BCF Bit Clear f

Syntax: [*label*] BCF f,b

Operands: $0 \leq f \leq 31$
 $0 \leq b \leq 7$

Operation: $0 \rightarrow (f)$

Status Affected: None

Encoding:

0100	bbbf	ffff
------	------	------

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example: BCF FLAG_REG, 7

Before Instruction

FLAG_REG = 0xC7

After Instruction

FLAG_REG = 0x47

11.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PIC MCUs and can be used to develop for this and other PIC microcontrollers. The MPLAB ICD utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

11.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in Stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable VDD and VPP supplies, which allow it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In Stand-alone mode, the PRO MATE II device programmer can read, verify, or program PIC devices. It can also set code protection in this mode.

11.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PIC devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

11.11 PICDEM 1 Low Cost PIC MCU Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE in-circuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

11.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I²C™ bus and separate headers for connection to an LCD module and a keypad.

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NOTES:

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13.2 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

PIC16CR54A-04E, 10E, 20E (Extended)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage RC, XT and LP modes HS mode	3.25 4.5	— —	6.0 5.5	V V	
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current ⁽²⁾ RC ⁽³⁾ and XT modes HS mode HS mode	— — —	1.8 4.8 9.0	3.3 10 20	mA mA mA	FOSC = 4.0 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 16 MHz, VDD = 5.5V
D020	IPD	Power-down Current ⁽²⁾	— —	5.0 0.8	22 18	μA μA	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{EXT}$ (mA) with REXT in kΩ.

FIGURE 13-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR54A

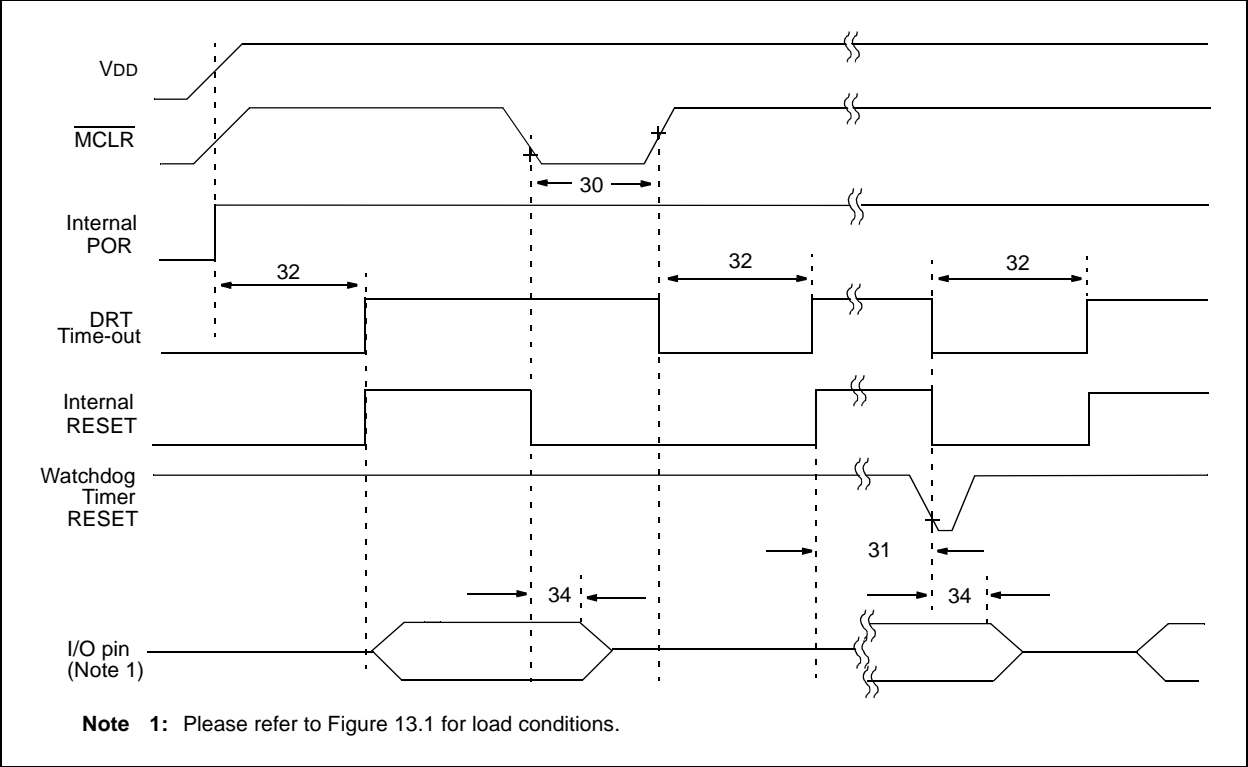


TABLE 13-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR54A

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics		Operating Temperature					
		0°C ≤ TA ≤ +70°C for commercial					
		-40°C ≤ TA ≤ +85°C for industrial					
		-40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	1.0*	—	—	μs	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7.0*	18*	40*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	7.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	TioZ	I/O Hi-impedance from MCLR Low	—	—	1.0*	μs	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 14-4: TYPICAL RC OSC
FREQUENCY vs. VDD,
CEXT = 300 PF

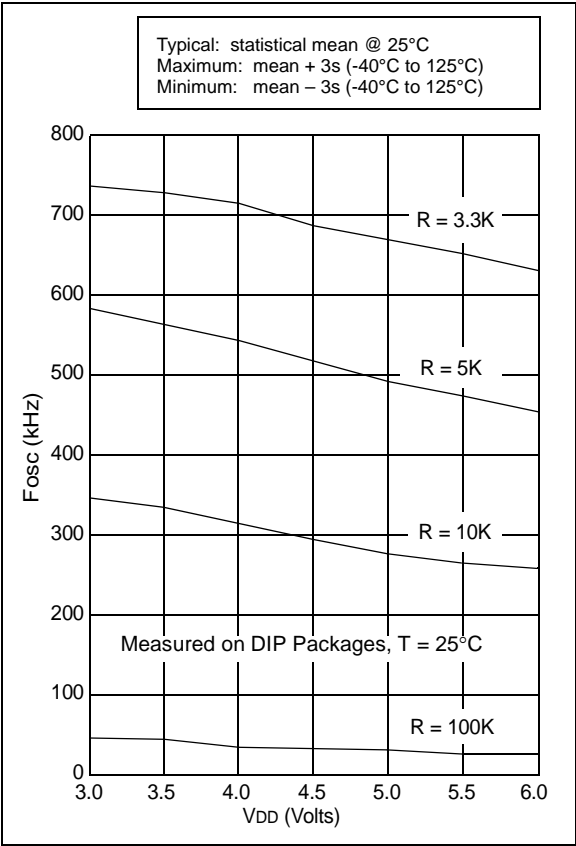


FIGURE 14-5: TYPICAL IPD vs. VDD,
WATCHDOG DISABLED

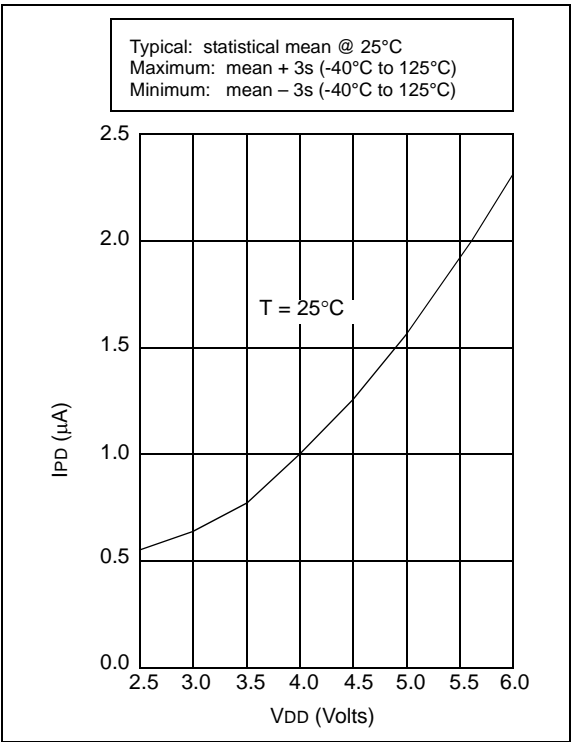


FIGURE 14-21: PORTA, B AND C IoL vs. VOL, VDD = 3 V

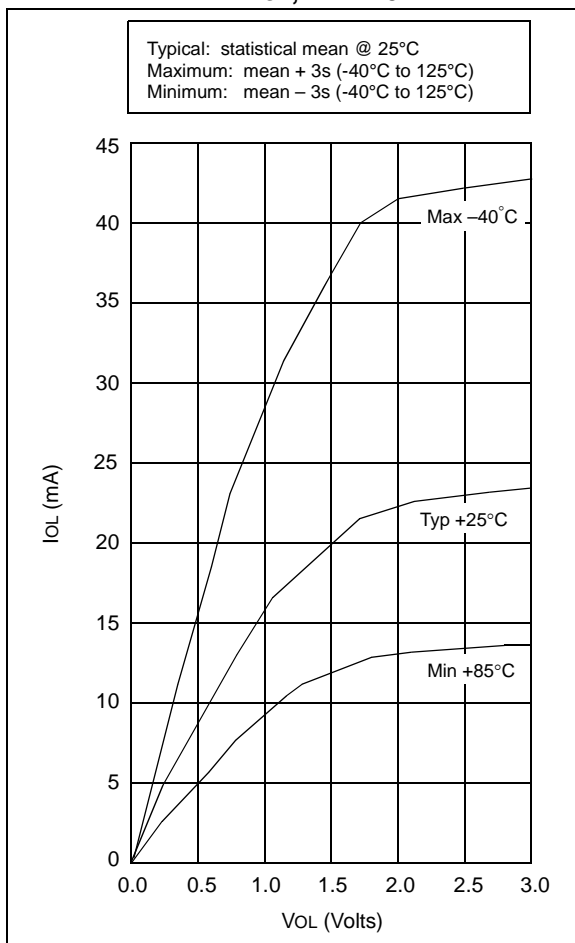
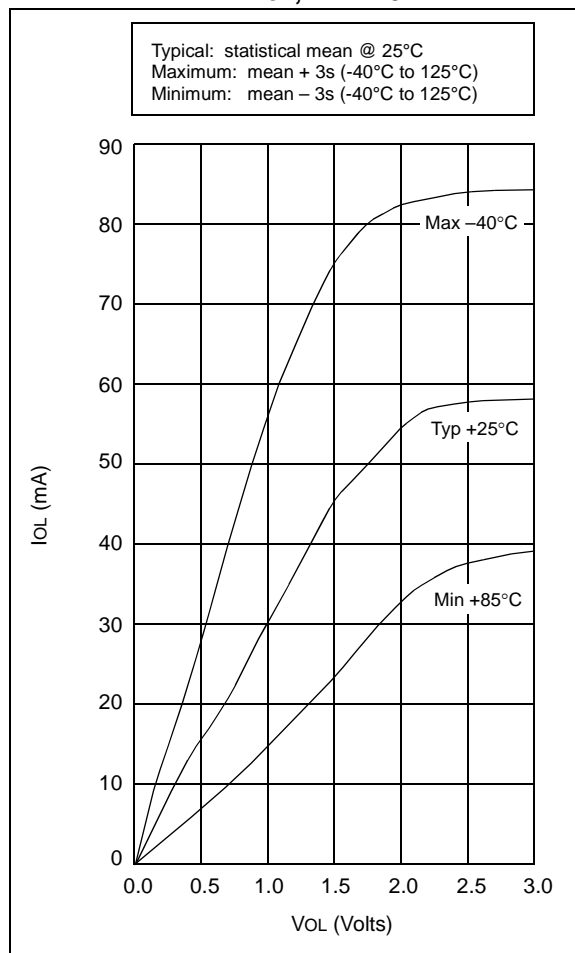


FIGURE 14-22: PORTA, B AND C IoL vs. VOL, VDD = 5 V



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15.3 DC Characteristics: PIC16LV54A-02 (Commercial) PIC16LV54A-02I (Industrial)

PIC16LV54A-02 PIC16LV54A-02I (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-20^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	V _{DD}	Supply Voltage RC and XT modes	2.0	—	3.8	V	
D002	V _{DR}	RAM Data Retention Voltage⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	V _{POR}	V_{DD} Start Voltage to ensure Power-on Reset	—	V _{SS}	—	V	See Section 5.1 for details on Power-on Reset
D004	S _{VDD}	V_{DD} Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	I _{DD}	Supply Current⁽²⁾ RC ⁽³⁾ and XT modes LP mode, Commercial LP mode, Industrial	— — —	0.5 11 14	— 27 35	mA μA μA	FOSC = 2.0 MHz, V _{DD} = 3.0V FOSC = 32 kHz, V _{DD} = 2.5V WDT disabled FOSC = 32 kHz, V _{DD} = 2.5V WDT disabled
D020	I _{PD}	Power-down Current^(2,4) Commercial Commercial Industrial Industrial	— — — —	2.5 0.25 3.5 0.3	12 4.0 14 5.0	μA μA μA μA	V _{DD} = 2.5V, WDT enabled V _{DD} = 2.5V, WDT disabled V _{DD} = 2.5V, WDT enabled V _{DD} = 2.5V, WDT disabled

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all I_{DD} measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS}, T0CKI = V_{DD}, MCLR = V_{DD}; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through R_{EXT}. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ.

4: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection on wake-up from SLEEP mode or during initial power-up.

15.5 Timing Parameter Symbolology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T	T
F Frequency	Time

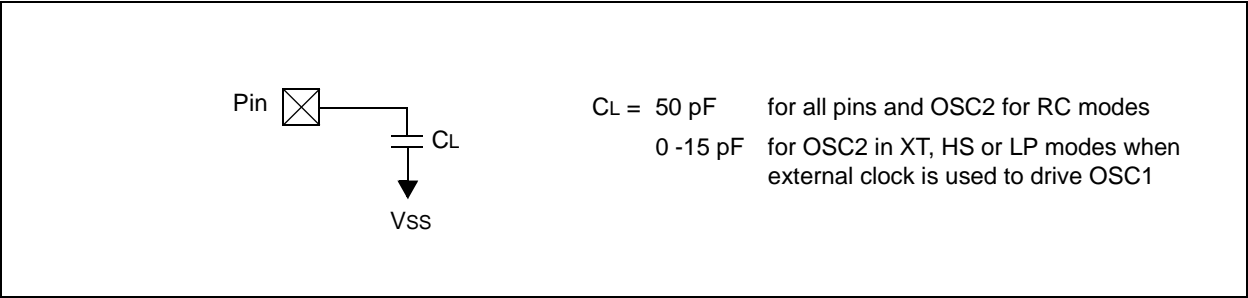
Lowercase letters (pp) and their meanings:

pp	
2 to	mc MCLR
ck CLKOUT	osc oscillator
cy cycle time	os OSC1
drt device reset timer	t0 T0CKI
io I/O port	wdt watchdog timer

Uppercase letters and their meanings:

S	
F Fall	P Period
H High	R Rise
I Invalid (Hi-impedance)	V Valid
L Low	Z Hi-impedance

FIGURE 15-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54A



16.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum” or “minimum” represents (mean + 3 σ) or (mean – 3 σ) respectively, where σ is a standard deviation, over the whole temperature range.

FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

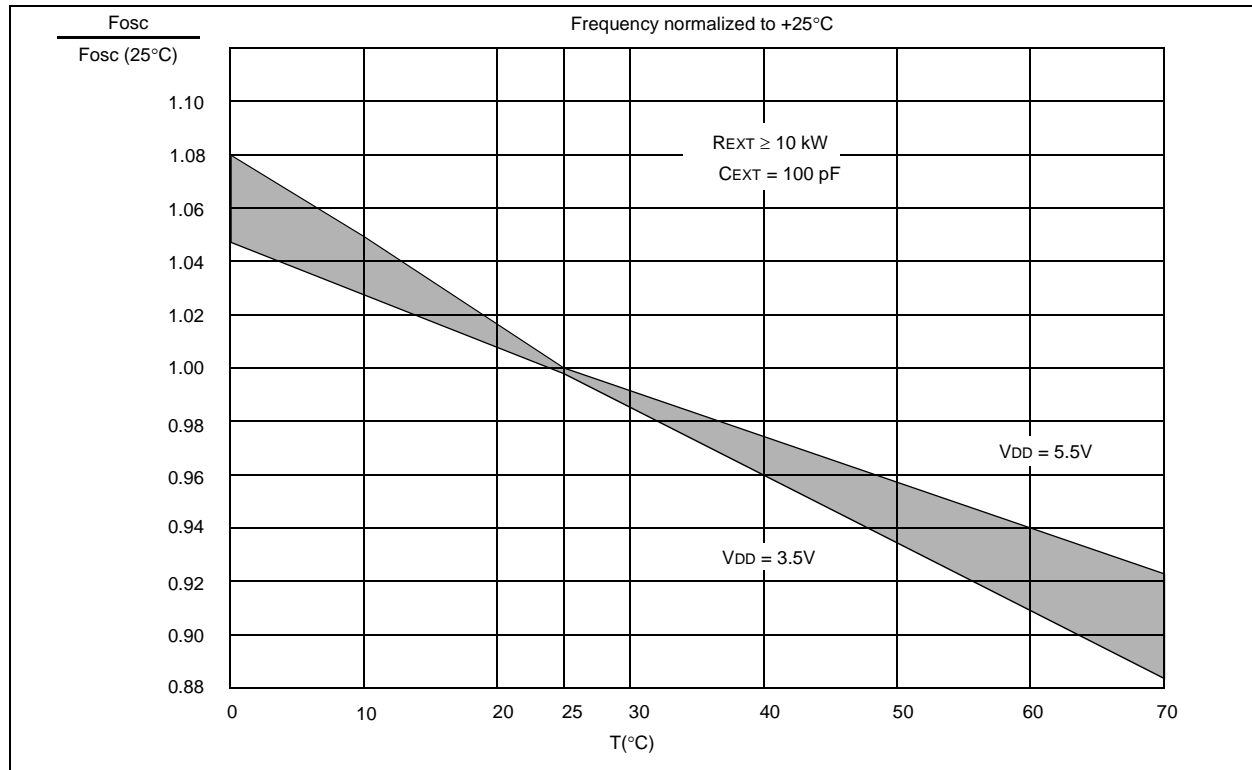


TABLE 16-1: RC OSCILLATOR FREQUENCIES

C_{EXT}	R_{EXT}	Average F_{osc} @ 5 V, 25°C	
20 pF	3.3K	5 MHz	± 27%
	5K	3.8 MHz	± 21%
	10K	2.2 MHz	± 21%
	100K	262 kHz	± 31%
100 pF	3.3K	1.6 MHz	± 13%
	5K	1.2 MHz	± 13%
	10K	684 kHz	± 18%
	100K	71 kHz	± 25%
300 pF	3.3K	660 kHz	± 10%
	5.0K	484 kHz	± 14%
	10K	267 kHz	± 15%
	100K	29 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for $V_{DD} = 5V$.

FIGURE 16-18: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

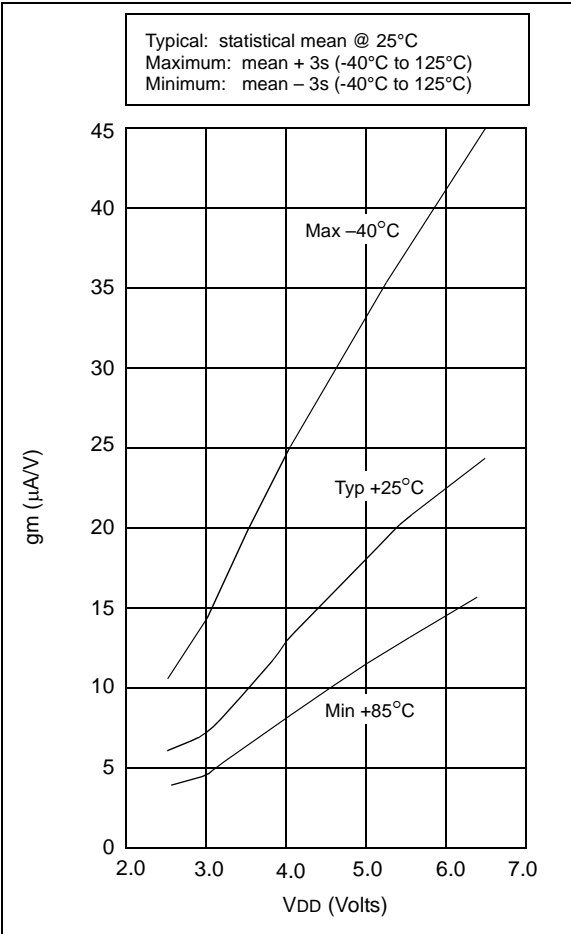


FIGURE 16-19: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

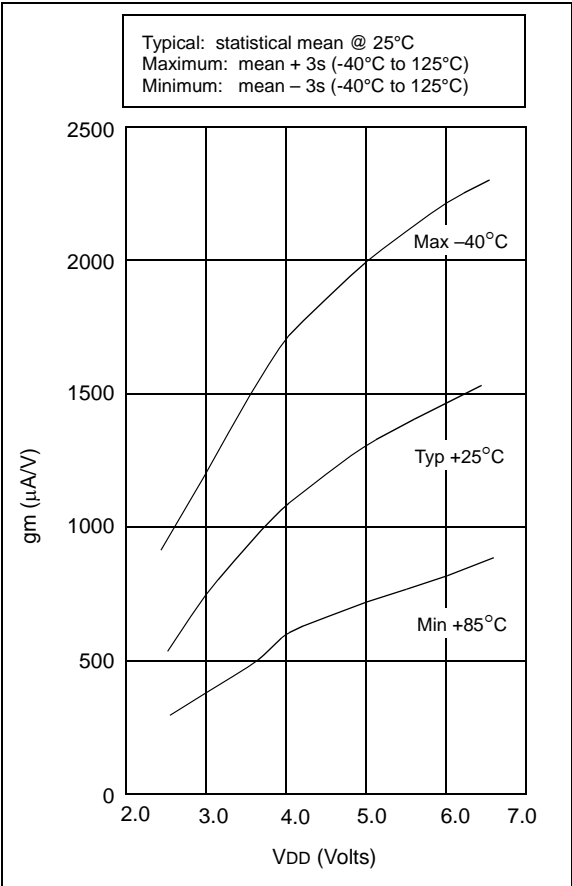


FIGURE 16-22: PORTA, B AND C IoL vs. VOL, VDD = 3V

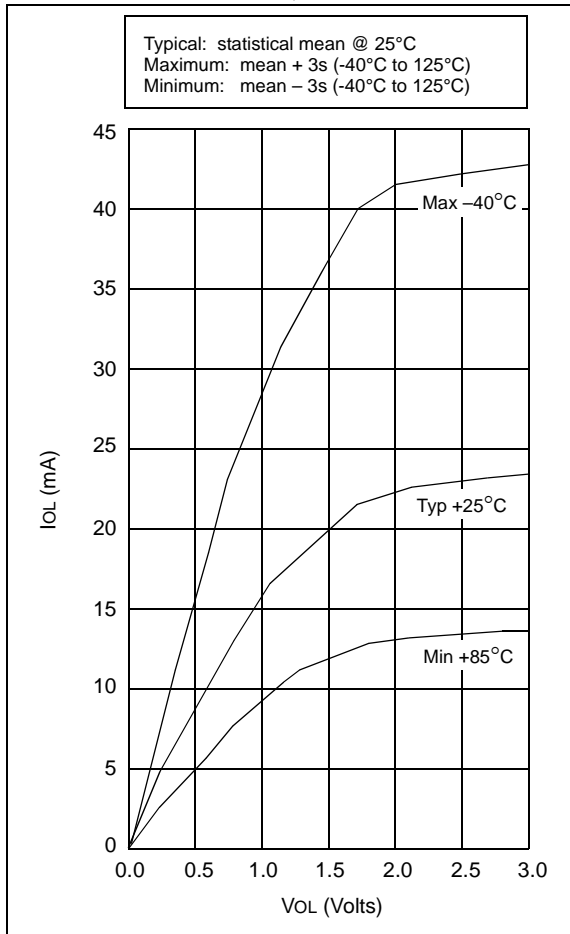


FIGURE 16-23: PORTA, B AND C IoL vs. VOL, VDD = 5V

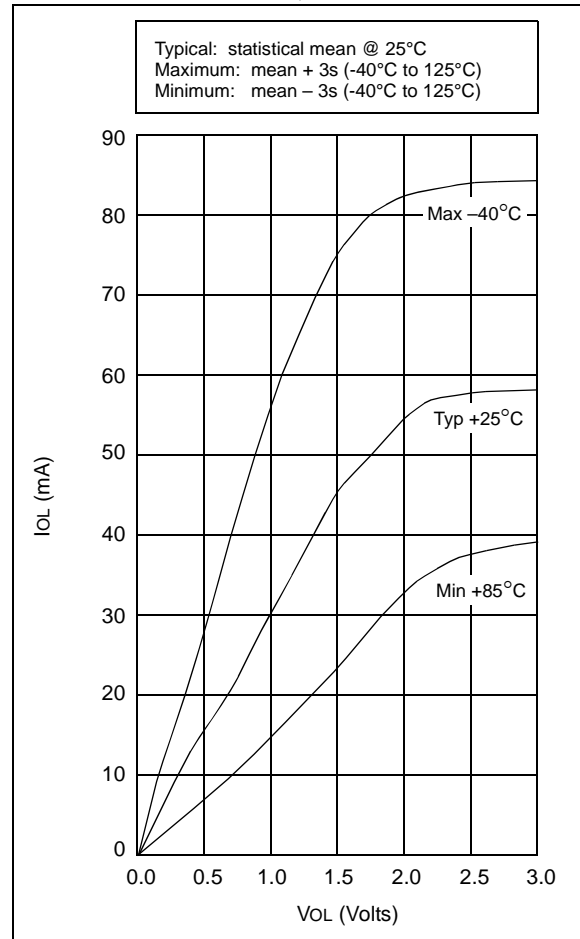


TABLE 16-2: INPUT CAPACITANCE FOR PIC16C54A/C58A

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
MCLR	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of $\pm 25\%$ (three standard deviations) should be taken into account.

17.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial)		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial					
PIC16C5X PIC16CR5X (Commercial, Industrial)		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
D010	IDD	Supply Current^(2,3)					
		PIC16LC5X	—	0.5	2.4	mA	FOSC = 4.0 MHz, VDD = 5.5V, XT and RC modes
			—	11	27	μA	FOSC = 32 kHz, VDD = 2.5V, LP mode, Commercial
D010A		PIC16C5X	—	14	35	μA	FOSC = 32 kHz, VDD = 2.5V, LP mode, Industrial
			—	1.8	2.4	mA	FOSC = 4 MHz, VDD = 5.5V, XT and RC modes
			—	2.6	3.6*	mA	FOSC = 10 MHz, VDD = 3.0V, HS mode
			—	4.5	16	mA	FOSC = 20 MHz, VDD = 5.5V, HS mode
			—	14	32	μA	FOSC = 32 kHz, VDD = 3.0V, LP mode, Commercial
			—	17	40	μA	FOSC = 32 kHz, VDD = 3.0V, LP mode, Industrial

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

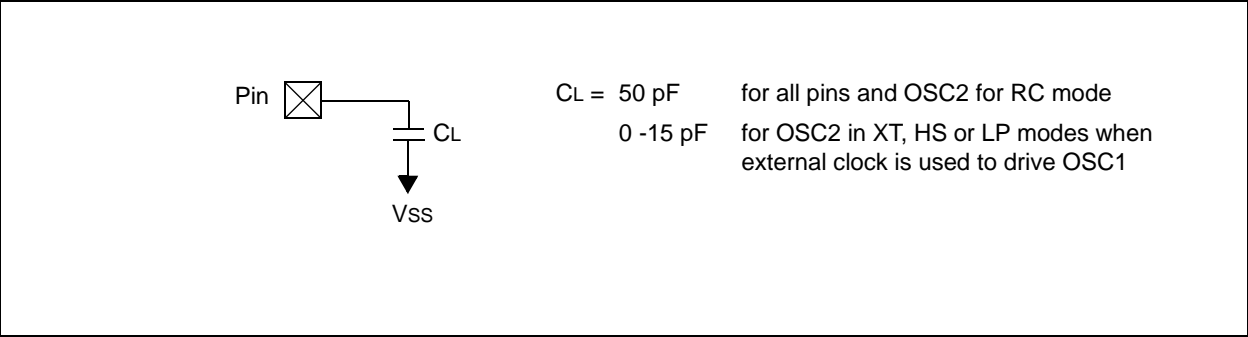
17.4 Timing Parameter Symbolology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T			
F	Frequency	T	Time
Lowercase letters (pp) and their meanings:			
pp		mc	MCLR
2	to	osc	oscillator
ck	CLKOUT	os	OSC1
cy	cycle time	t0	T0CKI
drt	device reset timer	wdt	watchdog timer
io	I/O port		
Uppercase letters and their meanings:			
S		P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	Hi-impedance
L	Low		

FIGURE 17-5: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B-04, 20



PIC16C5X

FIGURE 17-7: CLKOUT AND I/O TIMING - PIC16C5X, PIC16CR5X

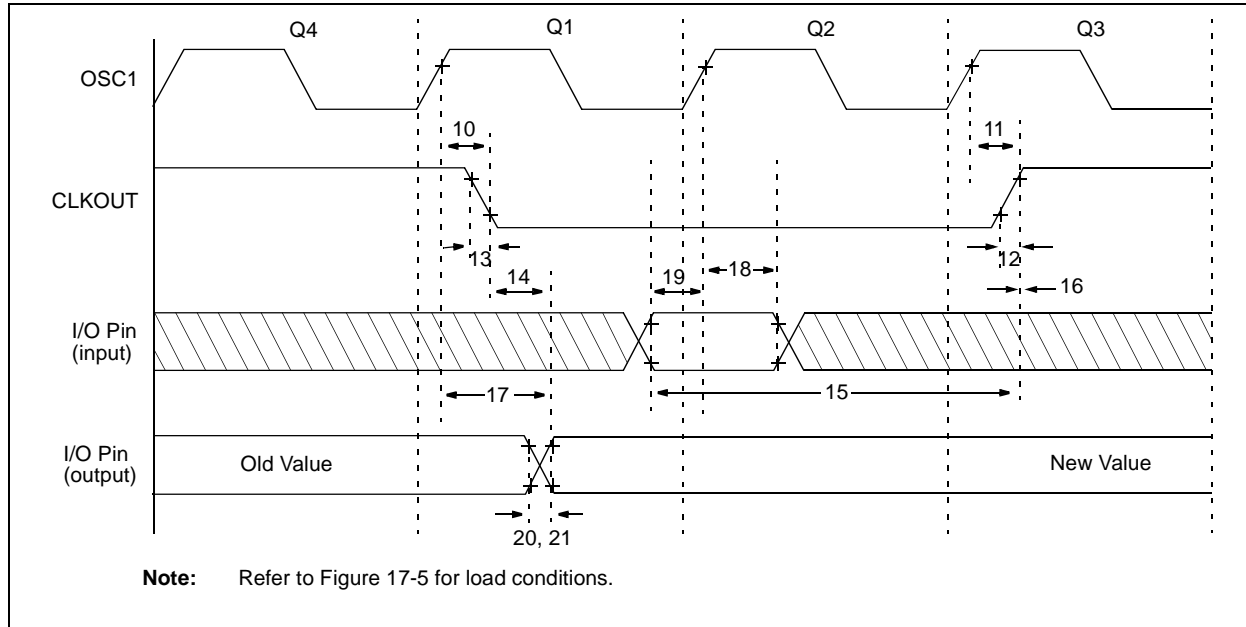


TABLE 17-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature				
		0°C ≤ TA ≤ +70°C for commercial				
		-40°C ≤ TA ≤ +85°C for industrial				
		-40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽¹⁾	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ ⁽¹⁾	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽²⁾	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽²⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

2: Refer to Figure 17-5 for load conditions.

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