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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3.25V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16c57-xte-so">https://www.e-xfl.com/product-detail/microchip-technology/pic16c57-xte-so</a>



# PIC16C5X

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## 8-Bit EPROM/ROM-Based CMOS Microcontrollers

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### 1.0 GENERAL DESCRIPTION

The PIC16C5X from Microchip Technology is a family of low cost, high performance, 8-bit fully static, EPROM/ROM-based CMOS microcontrollers. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle except for program branches which take two cycles. The PIC16C5X delivers performance in an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C5X products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external RESET circuitry. There are four oscillator configurations to choose from, including the power saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and Code Protection features improve system cost, power and reliability.

The UV erasable Cerdip packaged versions are ideal for code development, while the cost effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers, while benefiting from the OTP's flexibility.

The PIC16C5X products are supported by a full featured macro assembler, a software simulator, an in-circuit emulator, a low cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

### 1.1 Applications

The PIC16C5X series fits perfectly in applications ranging from high speed automotive and appliance motor control to low power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customizing application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low cost, low power, high performance ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, co-processor applications).

## 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle except for program branches.

The PIC16C54/CR54 and PIC16C55 address 512 x 12 of program memory, the PIC16C56/CR56 address 1K x 12 of program memory, and the PIC16C57/CR57 and PIC16C58/CR58 address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 (for PIC16C54/56/58) and Table 3-2 (for PIC16C55/57).

# PIC16C5X

FIGURE 8-3:       TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALER

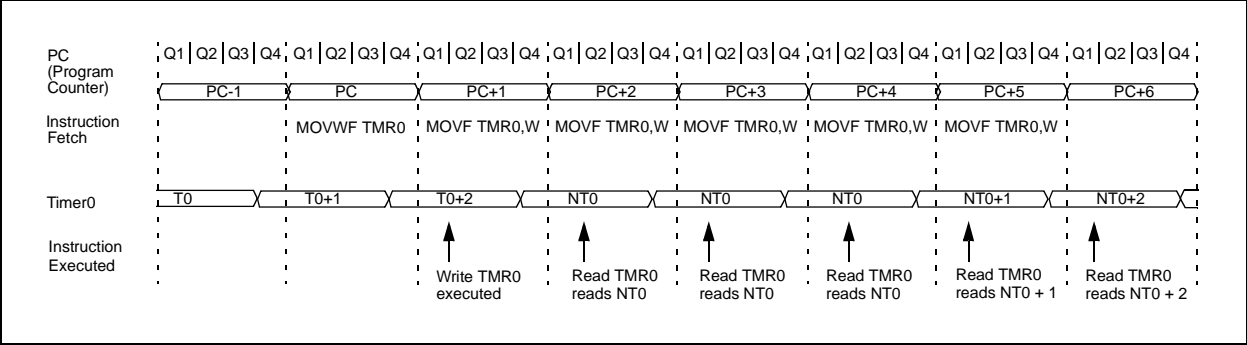


FIGURE 8-4:       TIMER0 TIMING: INTERNAL CLOCK/PRESCALER 1:2

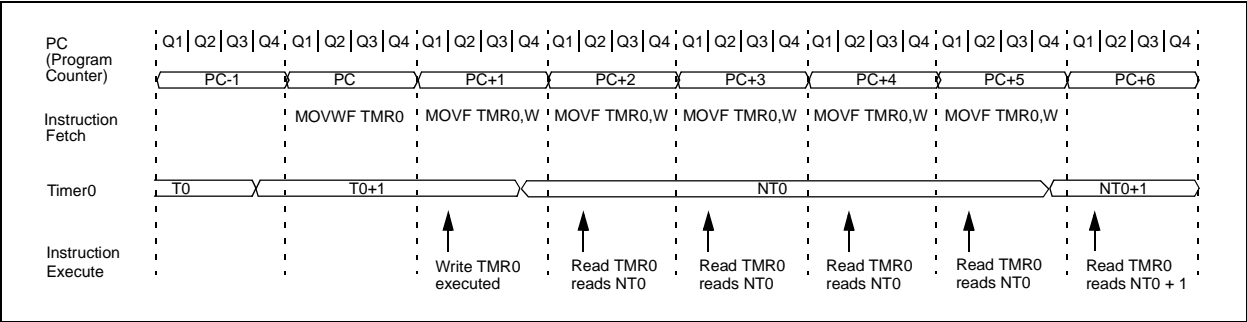


TABLE 8-1:       REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on MCLR and WDT Reset
01h	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells not used by Timer0.

# PIC16C5X

## IORLW Inclusive OR literal with W

Syntax: [ *label* ] IORLW *k*  
Operands:  $0 \leq k \leq 255$   
Operation: (W) .OR. (*k*)  $\rightarrow$  (W)  
Status Affected: Z  
Encoding: 

1101	kkkk	kkkk
------	------	------

  
Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.  
Words: 1  
Cycles: 1  
Example: IORLW 0x35

Before Instruction  
W = 0x9A  
After Instruction  
W = 0xBF  
Z = 0

## IORWF Inclusive OR W with f

Syntax: [ *label* ] IORWF *f*,*d*  
Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$   
Operation: (W).OR. (*f*)  $\rightarrow$  (*dest*)  
Status Affected: Z  
Encoding: 

0001	00df	ffff
------	------	------

  
Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.  
Words: 1  
Cycles: 1  
Example: IORWF RESULT, 0

Before Instruction  
RESULT = 0x13  
W = 0x91  
After Instruction  
RESULT = 0x13  
W = 0x93  
Z = 0

## MOVF Move f

Syntax: [ *label* ] MOVF *f*,*d*  
Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$   
Operation: (*f*)  $\rightarrow$  (*dest*)  
Status Affected: Z  
Encoding: 

0010	00df	ffff
------	------	------

  
Description: The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.  
Words: 1  
Cycles: 1  
Example: MOVF FSR, 0

After Instruction  
W = value in FSR register

## MOVLW Move Literal to W

Syntax: [ *label* ] MOVLW *k*  
Operands:  $0 \leq k \leq 255$   
Operation: *k*  $\rightarrow$  (W)  
Status Affected: None  
Encoding: 

1100	kkkk	kkkk
------	------	------

  
Description: The eight bit literal 'k' is loaded into the W register.  
Words: 1  
Cycles: 1  
Example: MOVLW 0x5A

After Instruction  
W = 0x5A

## SUBWF Subtract W from f

Syntax: `[label] SUBWF f,d`  
 Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$   
 Operation:  $(f) - (W) \rightarrow (\text{dest})$   
 Status Affected: C, DC, Z  
 Encoding: 

0000	10df	ffff
------	------	------

  
 Description: Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1: `SUBWF REG1, 1`

Before Instruction

REG1 = 3  
 W = 2  
 C = ?

After Instruction

REG1 = 1  
 W = 2  
 C = 1 ; result is positive

Example 2:

Before Instruction

REG1 = 2  
 W = 2  
 C = ?

After Instruction

REG1 = 0  
 W = 2  
 C = 1 ; result is zero

Example 3:

Before Instruction

REG1 = 1  
 W = 2  
 C = ?

After Instruction

REG1 = 0xFF  
 W = 2  
 C = 0 ; result is negative

## SWAPF Swap Nibbles in f

Syntax: `[label] SWAPF f,d`  
 Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$   
 Operation:  $(f<3:0>) \rightarrow (\text{dest}<7:4>);$   
 $(f<7:4>) \rightarrow (\text{dest}<3:0>)$

Status Affected: None

Encoding: 

0011	10df	ffff
------	------	------

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example `SWAPF REG1, 0`

Before Instruction

REG1 = 0xA5

After Instruction

REG1 = 0xA5  
 W = 0x5A

## TRIS Load TRIS Register

Syntax: `[label] TRIS f`  
 Operands:  $f = 5, 6 \text{ or } 7$   
 Operation:  $(W) \rightarrow \text{TRIS register } f$   
 Status Affected: None  
 Encoding: 

0000	0000	0fff
------	------	------

  
 Description: TRIS register 'f' ( $f = 5, 6, \text{ or } 7$ ) is loaded with the contents of the W register.

Words: 1

Cycles: 1

Example `TRIS PORTB`

Before Instruction

W = 0xA5

After Instruction

TRISB = 0xA5

## 11.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/  
MPLIB™ Object Librarian
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM 2 Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - KEELQ® Demonstration Board

### 11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows®-based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

### 11.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

### 11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

## 11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for pre-compiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

## 11.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

## 11.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows environment were chosen to best make these features available to you, the end user.

## 11.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.



TABLE 11-1: DEVELOPMENT TOOLS FROM MICROCHIP

	PIC12CXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXX	PIC16C7X	PIC16C7XX	PIC16C8X	PIC16F8XX	PIC16G9XX	PIC17C4X	PIC17C7XX	PIC18CXX2	PIC18FXX	24CXX/ 25CXX/ 93CXX	HCXXX	MCRFXXX	MCP2510
Software Tools	MPLAB® Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	MPLAB® C17 C Compiler										✓		✓					
	MPLAB® C18 C Compiler												✓					
Emulators	MPASM™ Assembler/ MPLINK™ Object Linker	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	MPLAB® ICE In-Circuit Emulator	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
	ICEPIC™ In-Circuit Emulator	✓		✓	✓		✓	✓		✓								
Debugger	MPLAB® ICD In-Circuit Debugger			✓	✓	✓			✓					✓				
Programmers	PICSTART® Plus Entry Level Development Programmer	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓			
	PRO MATE® II Universal Device Programmer	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓		
Demo Boards and Eval Kits	PICDEM™ 1 Demonstration Board		✓			†		✓			✓							
	PICDEM™ 2 Demonstration Board				†	†							✓					
	PICDEM™ 3 Demonstration Board									✓								
	PICDEM™ 14A Demonstration Board		✓															
	PICDEM™ 17 Demonstration Board											✓						
	KEELOQ® Evaluation Kit															✓		
	KEELOQ® Transponder Kit															✓		
	microID™ Programmer's Kit																✓	
	125 kHz microID™ Developer's Kit																✓	
	125 kHz Anticollision Developer's Kit																✓	
	13.56 MHz Anticollision microID™ Developer's Kit																✓	
	MCP2510 CAN Developer's Kit																✓	✓

\* Contact the Microchip Technology Inc. web site at [www.microchip.com](http://www.microchip.com) for information on how to use the MPLAB® ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77.

\*\* Contact Microchip Technology Inc. for availability date.

† Development tool is available on select devices.

## 12.2 DC Characteristics: PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
D001	VDD	<b>Supply Voltage</b>					
		PIC16C5X-RCI	3.0	—	6.25	V	
		PIC16C5X-XTI	3.0	—	6.25	V	
		PIC16C5X-10I	4.5	—	5.5	V	
		PIC16C5X-HSI	4.5	—	5.5	V	
		PIC16C5X-LPI	2.5	—	6.25	V	
D002	VDR	<b>RAM Data Retention Voltage<sup>(1)</sup></b>	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	<b>VDD Start Voltage</b> to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	<b>VDD Rise Rate</b> to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	<b>Supply Current<sup>(2)</sup></b>					
		PIC16C5X-RCI <sup>(3)</sup>	—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
		PIC16C5X-XTI	—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
		PIC16C5X-10I	—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
		PIC16C5X-HSI	—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
		PIC16C5X-HSI	—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
		PIC16C5X-LPI	—	15	40	μA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020	IPD	<b>Power-down Current<sup>(2)</sup></b>	—	4.0	14	μA	VDD = 3.0V, WDT enabled
			—	0.6	12	μA	VDD = 3.0V, WDT disabled

\* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula:  $I_R = VDD/2R_{EXT}$  (mA) with REXT in kΩ.

12.6 Timing Parameter Symbolology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T		T
F	Frequency	Time

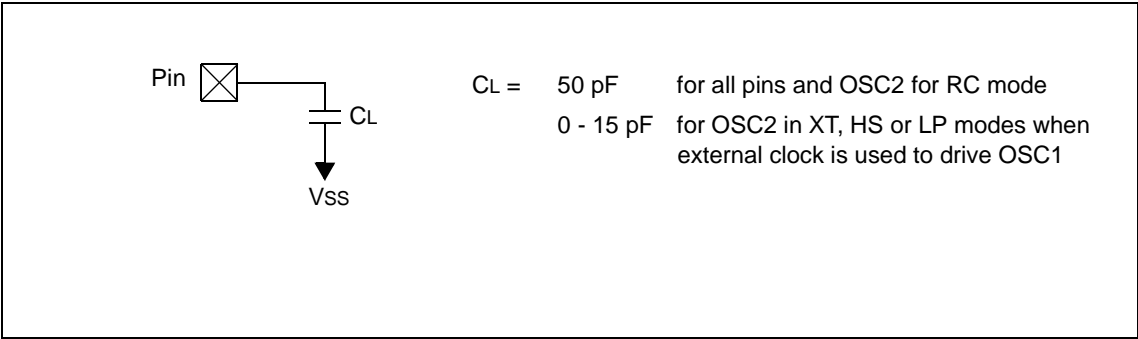
Lowercase letters (pp) and their meanings:

pp		mc	MCLR
2	to	osc	oscillator
ck	CLKOUT	os	OSC1
cy	cycle time	t0	T0CKI
drt	device reset timer	wdt	watchdog timer
io	I/O port		

Uppercase letters and their meanings:

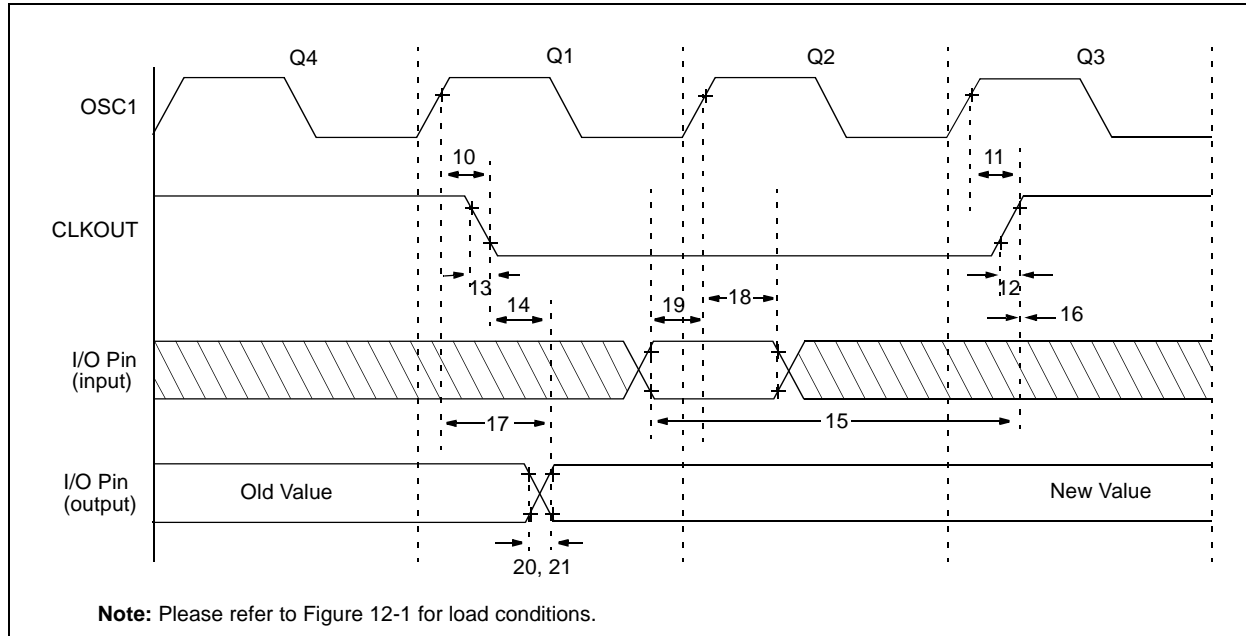
S		P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	Hi-impedance
L	Low		

FIGURE 12-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54/55/56/57



# PIC16C5X

**FIGURE 12-3: CLKOUT AND I/O TIMING - PIC16C54/55/56/57**



**TABLE 12-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54/55/56/57**

Standard Operating Conditions (unless otherwise specified)						
Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended						
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ <sup>(1)</sup>	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ <sup>(1)</sup>	—	15	30**	ns
12	TckR	CLKOUT rise time <sup>(1)</sup>	—	5.0	15**	ns
13	TckF	CLKOUT fall time <sup>(1)</sup>	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid <sup>(1)</sup>	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ <sup>(1)</sup>	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ <sup>(1)</sup>	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid <sup>(2)</sup>	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time <sup>(2)</sup>	—	10	25**	ns
21	TioF	Port output fall time <sup>(2)</sup>	—	10	25**	ns

\* These parameters are characterized but not tested.

\*\* These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

**2:** Please refer to Figure 12-1 for load conditions.

FIGURE 13-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR54A

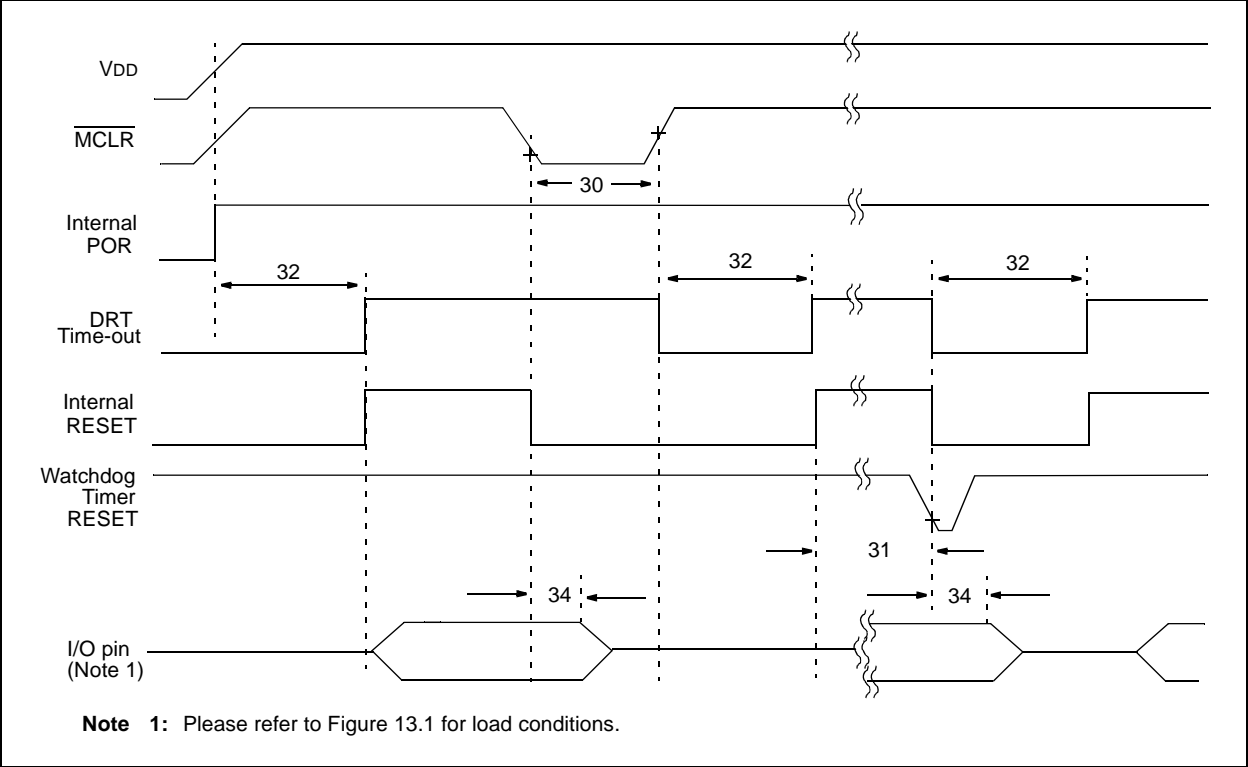


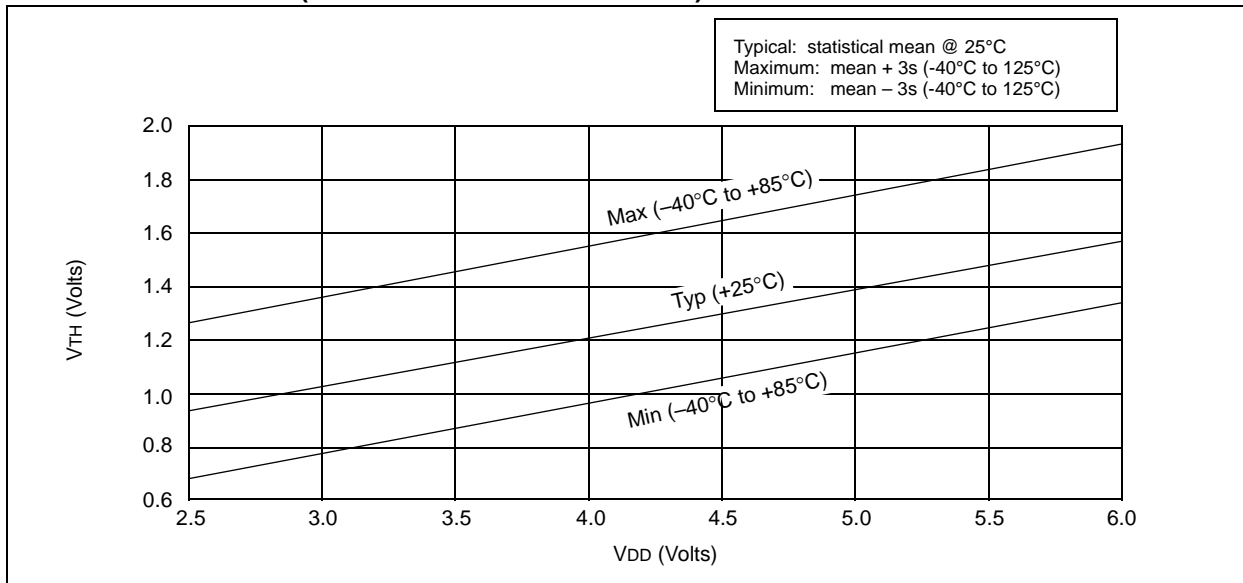
TABLE 13-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR54A

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics		Operating Temperature					
		0°C ≤ TA ≤ +70°C for commercial					
		-40°C ≤ TA ≤ +85°C for industrial					
		-40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	1.0*	—	—	μs	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7.0*	18*	40*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	7.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	TioZ	I/O Hi-impedance from MCLR Low	—	—	1.0*	μs	

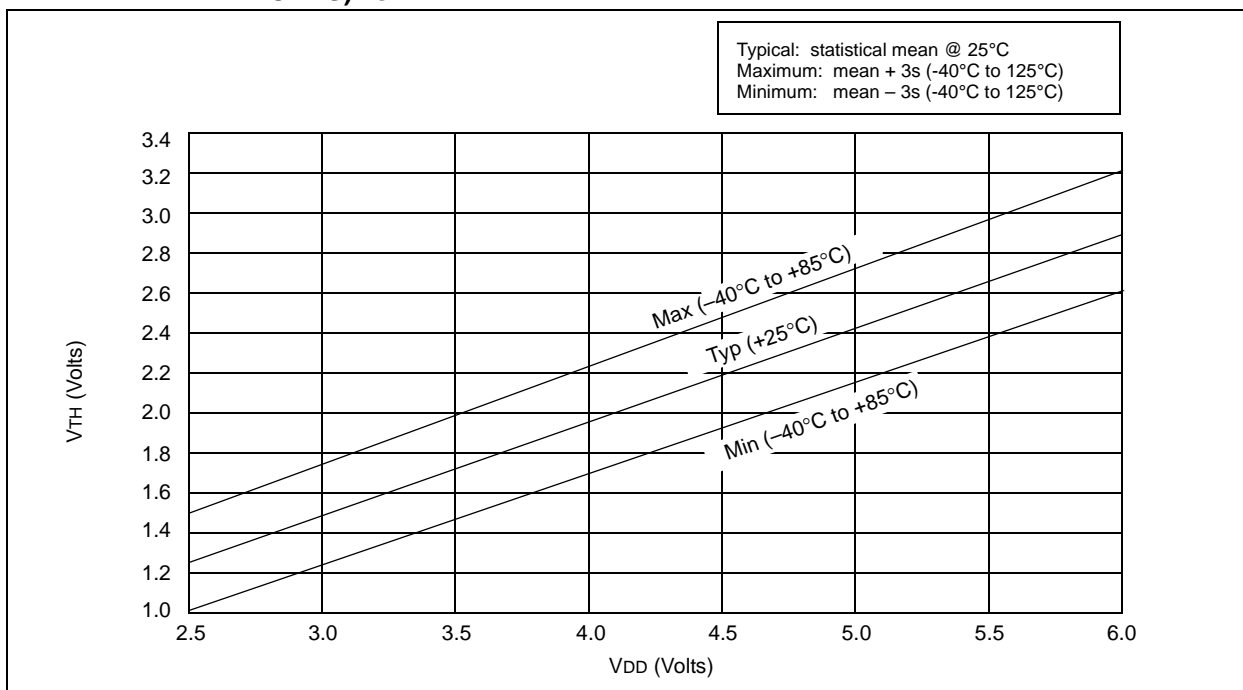
\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 16-7:  $V_{TH}$  (INPUT THRESHOLD VOLTAGE) OF I/O PINS -  $V_{DD}$**



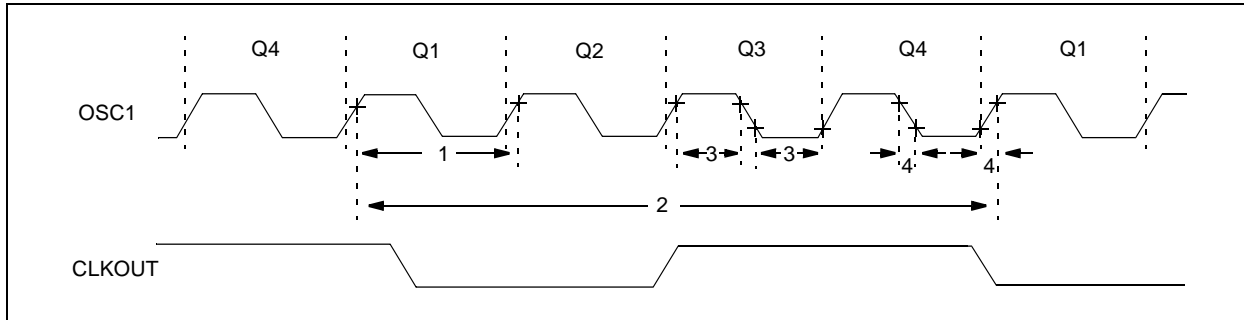
**FIGURE 16-8:  $V_{TH}$  (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs.  $V_{DD}$**



# PIC16C5X

## 17.5 Timing Diagrams and Specifications

**FIGURE 17-6: EXTERNAL CLOCK TIMING - PIC16C5X, PIC16CR5X**



**TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X**

<b>Standard Operating Conditions (unless otherwise specified)</b> <b>AC Characteristics</b> Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency <sup>(1)</sup>	DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency <sup>(1)</sup>	DC	—	4.0	MHz	RC osc mode
			0.45	—	4.0	MHz	XT osc mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	20	MHz	HS osc mode (20)
1	TOSC	External CLKIN Period <sup>(1)</sup>	250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	μs	LP osc mode
		Oscillator Period <sup>(1)</sup>	250	—	—	ns	RC osc mode
			250	—	2,200	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	μs	LP osc mode

\* These parameters are characterized but not tested.

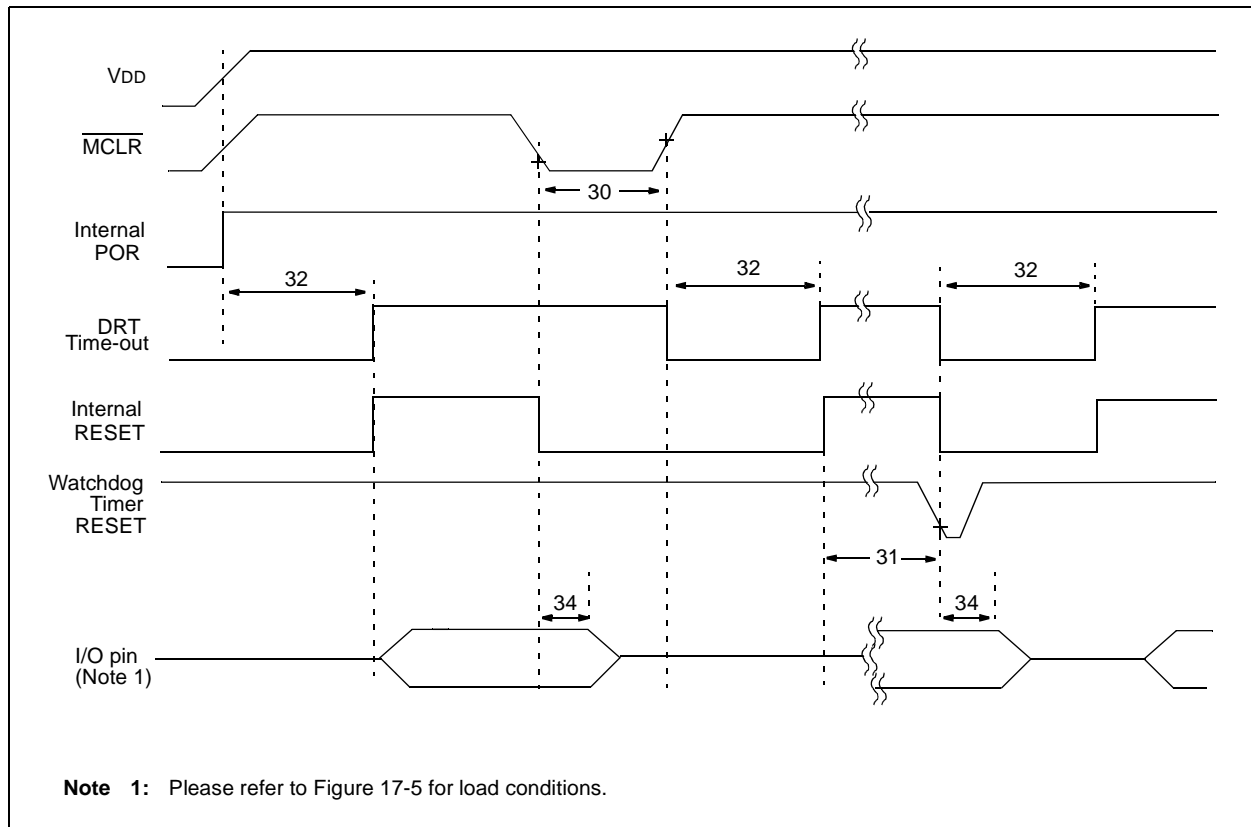
† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

**FIGURE 17-8: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X, PIC16CR5X**



**TABLE 17-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X, PIC16CR5X**

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics							
Operating Temperature    0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1000*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns	

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF, 25°C

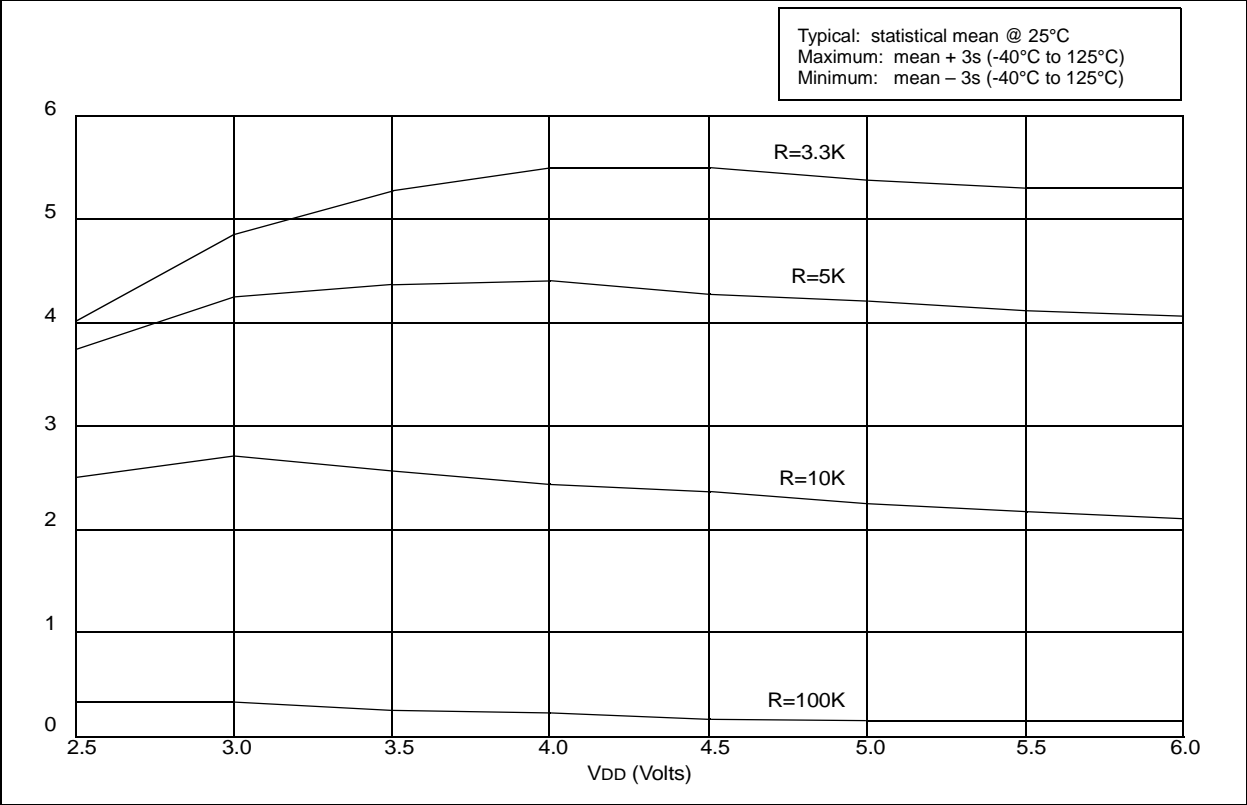


FIGURE 18-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF, 25°C

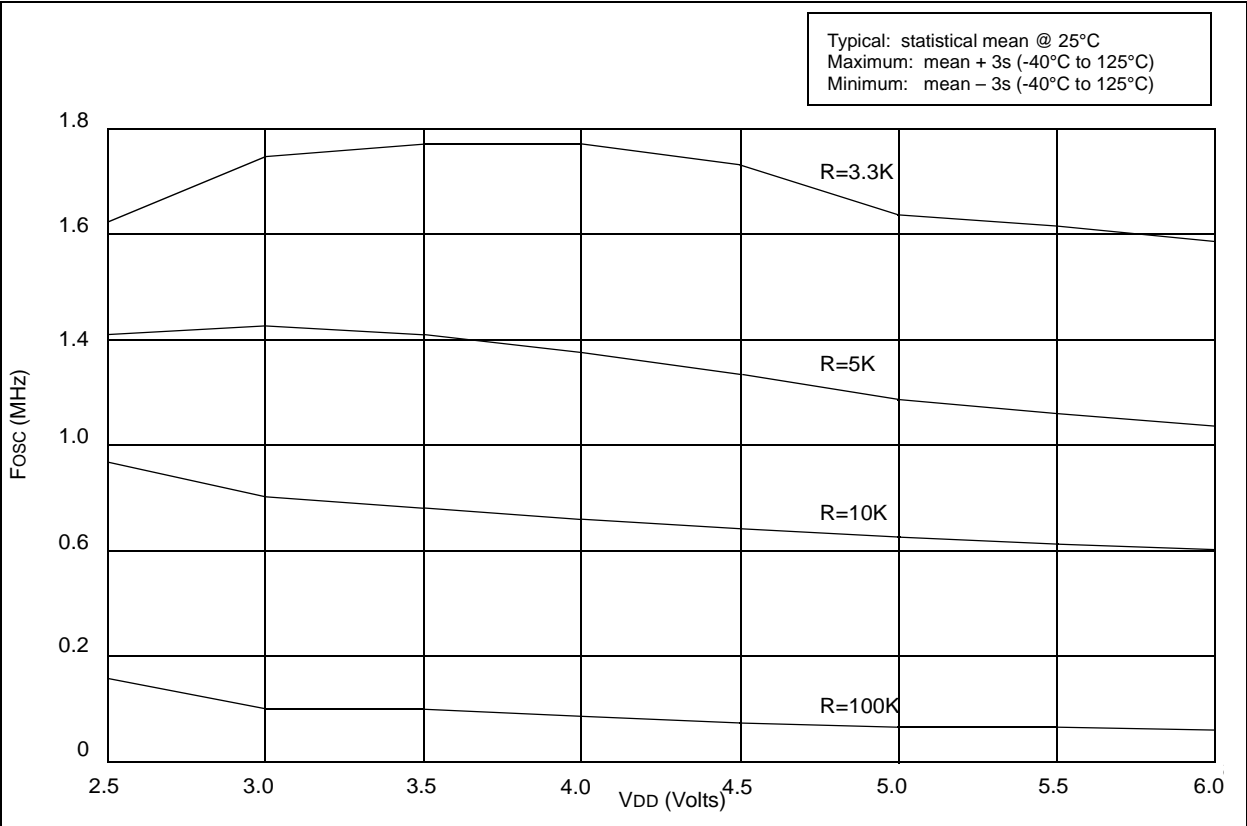


FIGURE 18-6: TYPICAL  $I_{PD}$  vs.  $V_{DD}$ , WATCHDOG ENABLED (25°C)

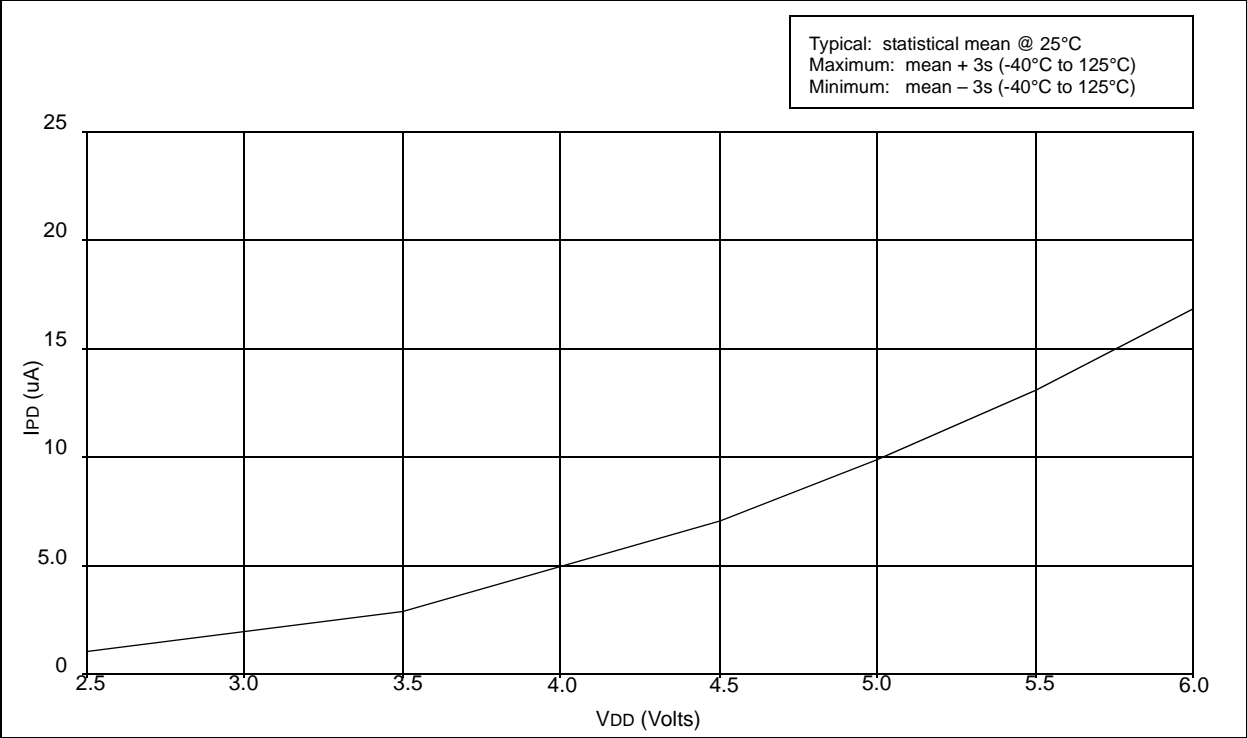


FIGURE 18-7: TYPICAL  $I_{PD}$  vs.  $V_{DD}$ , WATCHDOG ENABLED (-40°C, 85°C)

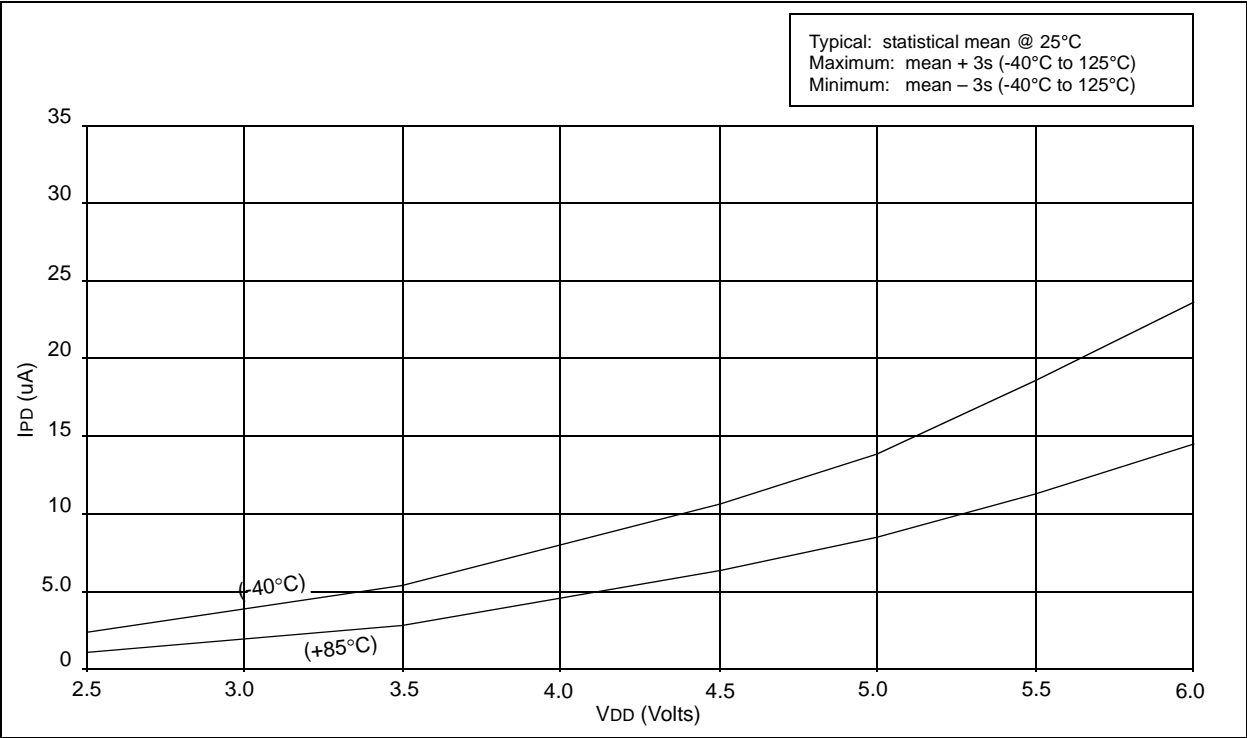


FIGURE 18-10: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (IN XT, HS AND LP MODES) vs. VDD

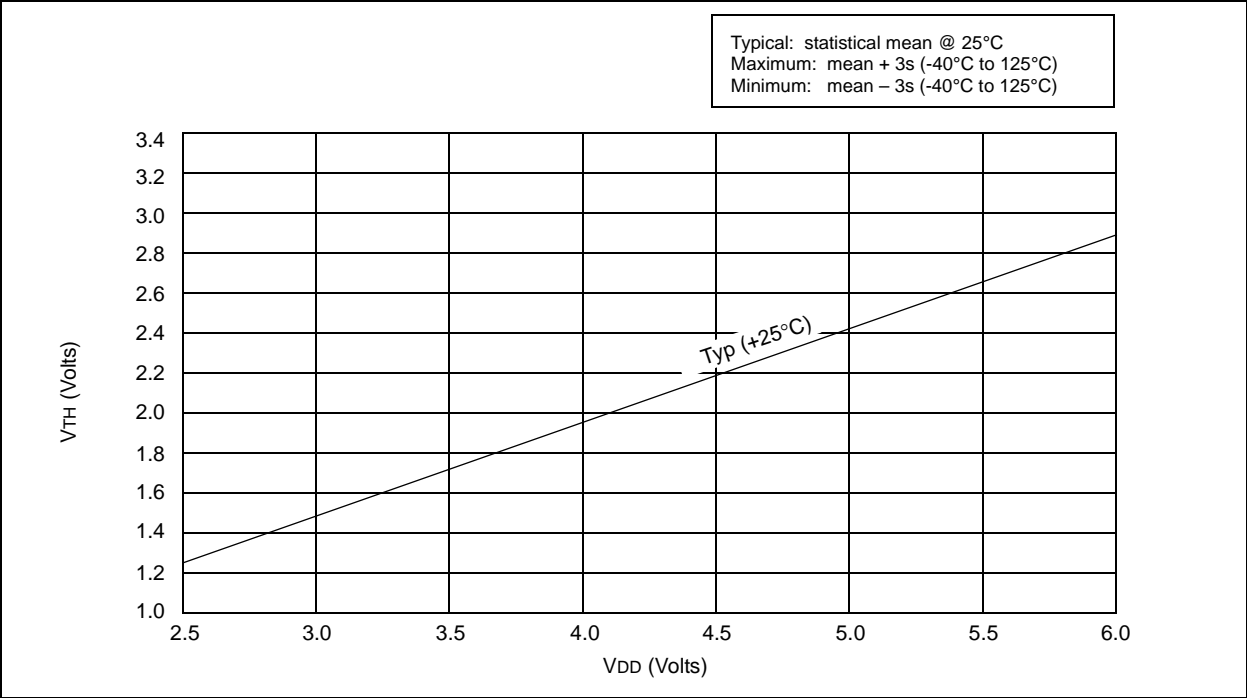


FIGURE 18-11: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, 25°C)

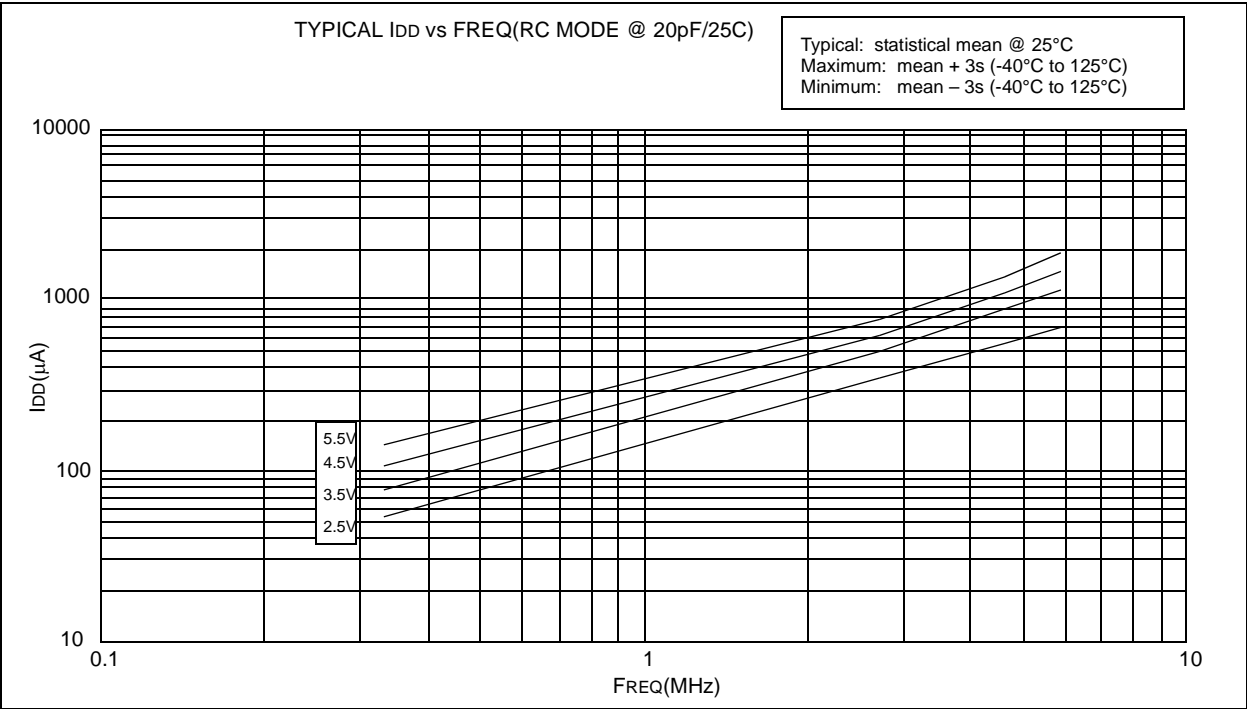


FIGURE 20-2: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (25°C)

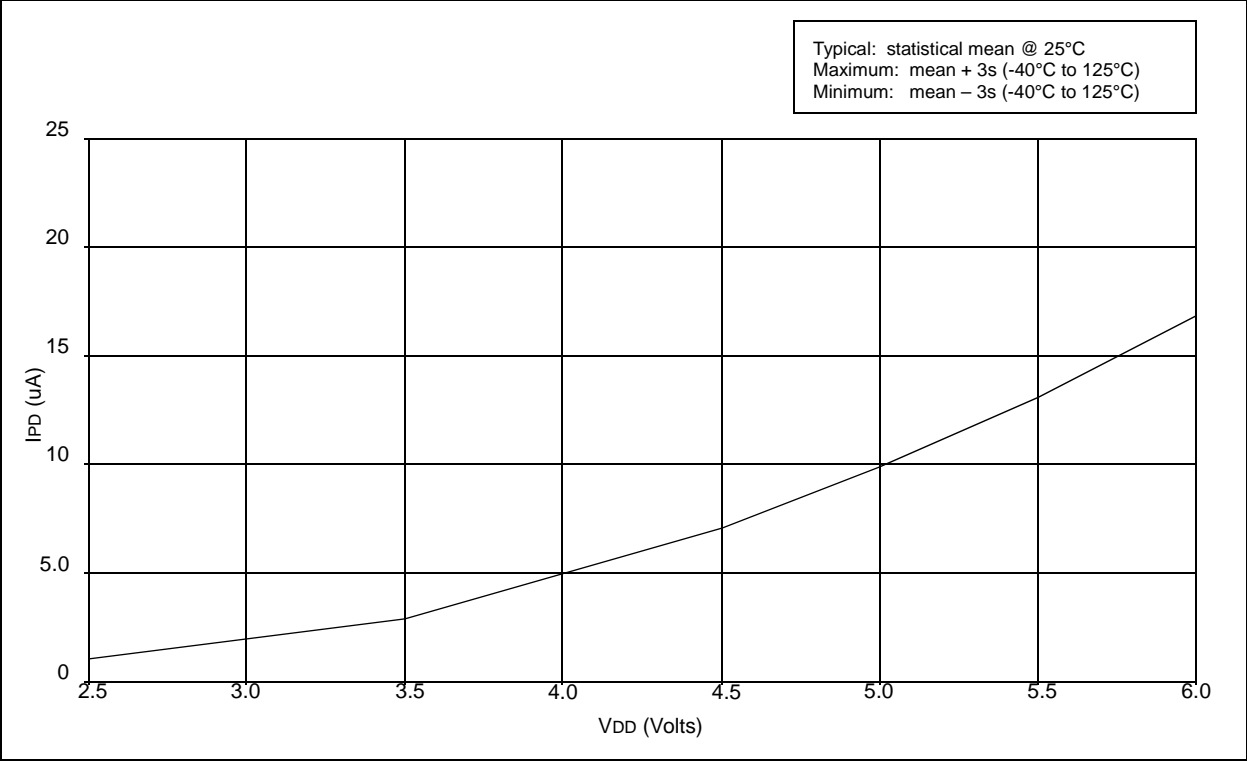


FIGURE 20-3: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (-40°C, 85°C)

