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What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57c-04-sp

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2 and Example 3-1.
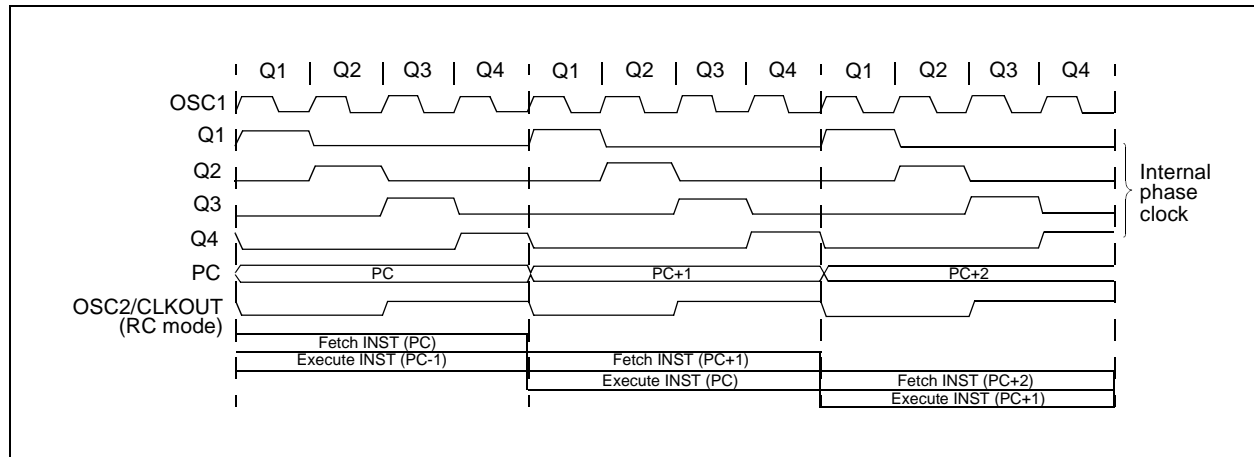
3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).
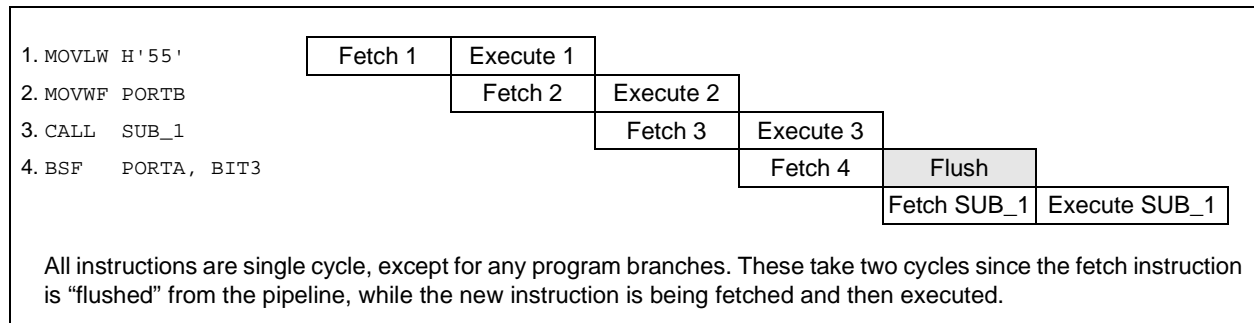
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2:   CLOCK/INSTRUCTION CYCLE

EXAMPLE 3-1:   INSTRUCTION PIPELINE FLOW

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline, while the new instruction is being fetched and then executed.

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FIGURE 8-3: **TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALER**
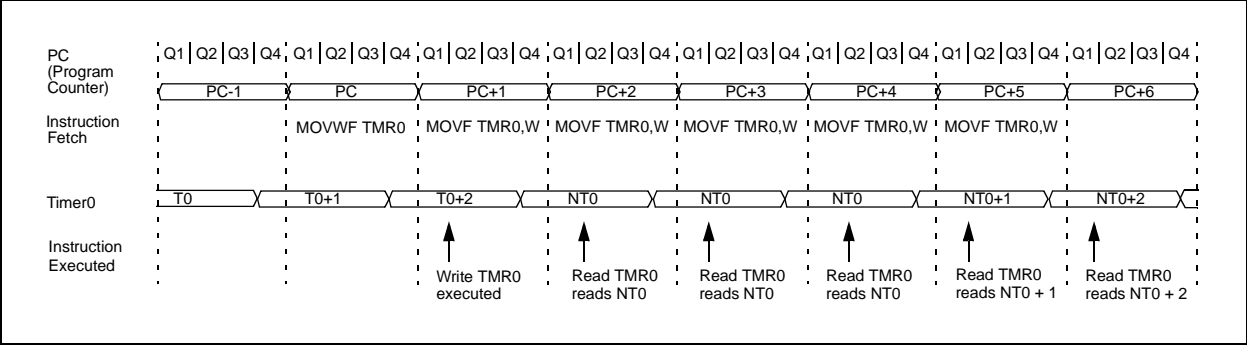
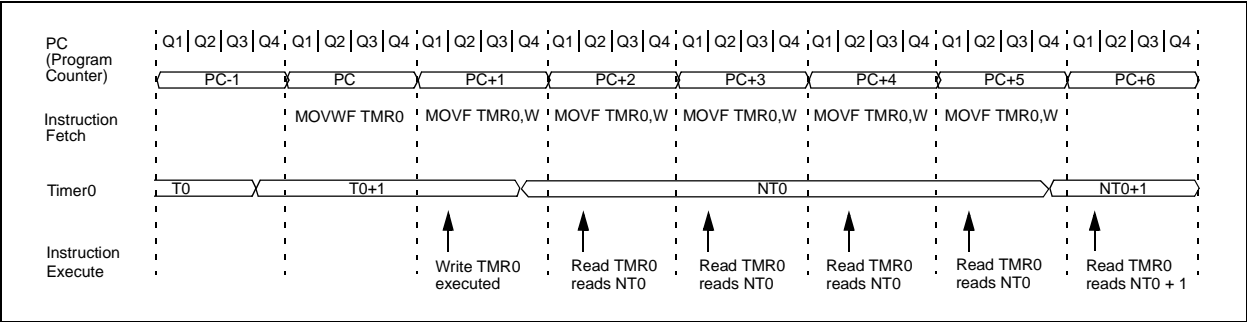**FIGURE 8-4:** **TIMER0 TIMING: INTERNAL CLOCK/PRESCALER 1:2**

TABLE 8-1: **REGISTERS ASSOCIATED WITH TIMER0**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on MCLR and WDT Reset
01h	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: `x` = unknown, `u` = unchanged, `-` = unimplemented. Shaded cells not used by Timer0.

Preliminary

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	0 ≤ k ≤ 511
Operation:	k → PC<8:0>; STATUS<6:5> → PC<10:9>
Status Affected:	None
Encoding:	`101k` `kkkk` `kkkk`
Description:	GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two-cycle instruction.
Words:	1
Cycles:	2
Example:	GOTO THERE

    After Instruction
        PC = address (THERE)

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	(f) + 1 → (dest)
Status Affected:	Z
Encoding:	`0010` `10df` `ffff`
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
Words:	1
Cycles:	1
Example:	INCF CNT, 1

    Before Instruction
        CNT = 0xFF
        Z   = 0
    After Instruction
        CNT = 0x00
        Z   = 1

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	(f) + 1 → (dest), skip if result = 0
Status Affected:	None
Encoding:	`0011` `11df` `ffff`
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.
Words:	1
Cycles:	1(2)
Example:	HERE INCFSZ CNT, 1 GOTO LOOP CONTINUE •

                •
                •

    Before Instruction
        PC   = address (HERE)
    After Instruction
        CNT   = CNT + 1;
        if CNT = 0,
        PC   = address (CONTINUE);
        if CNT ≠ 0,
        PC   = address (HERE +1)

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11.13 PICDEM 3 Low Cost PIC16CXXX Demonstration Board

The PICDEM 3 demonstration board is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with an LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 3 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer with an adapter socket, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 3 demonstration board to test firmware. A prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM 3 demonstration board is a LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM 3 demonstration board provides an additional RS-232 interface and Windows software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

11.14 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included and the user may erase it and program it with the other sample programs using the PRO MATE II device programmer, or the PICSTART Plus development programmer, and easily debug and test the sample code. In addition, the PICDEM 17 demonstration board supports downloading of programs to and executing out of external FLASH memory on board. The PICDEM 17 demonstration board is also usable with the MPLAB ICE in-circuit emulator, or the PICMASTER emulator and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

11.15 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchip's HCS Secure Data Products. The HCS evaluation kit includes a LCD display to show changing codes, a decoder to decode transmissions and a programming interface to program test transmitters.

Preliminary

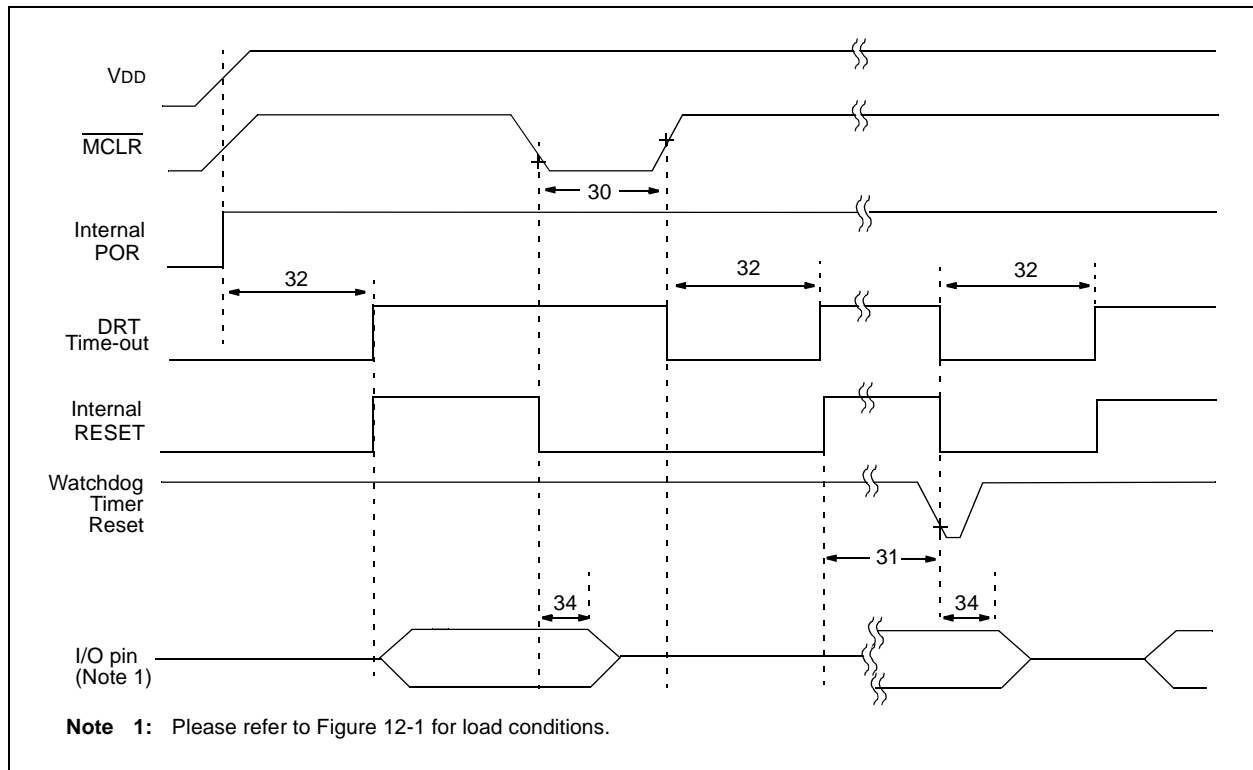**FIGURE 12-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54/55/56/57**

Note 1: Please refer to Figure 12-1 for load conditions.

TABLE 12-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial –40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	100*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	—	—	100*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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15.3 DC Characteristics: PIC16LV54A-02 (Commercial)
PIC16LV54A-02I (Industrial)

PIC16LV54A-02 PIC16LV54A-02I (Commercial, Industrial)							Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C $\leq$ TA $\leq$ +70°C for commercial −20°C $\leq$ TA $\leq$ +85°C for industrial
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	**Supply Voltage** RC and XT modes	2.0	—	3.8	V	
D002	VDR	**RAM Data Retention Voltage**[1]	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	**Supply Current**[2] RC[3] and XT modes LP mode, Commercial LP mode, Industrial	— — —	0.5 11 14	— 27 35	mA μA μA	FOSC = 2.0 MHz, VDD = 3.0V FOSC = 32 kHz, VDD = 2.5V WDT disabled FOSC = 32 kHz, VDD = 2.5V WDT disabled
D020	IPD	**Power-down Current**[2,4] Commercial Commercial Industrial Industrial	— — — —	2.5 0.25 3.5 0.3	12 4.0 14 5.0	μA μA μA μA	VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled

    *   These parameters are characterized but not tested.

    †   Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

    2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

        a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

        b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

    3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

    4: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection on wake-up from SLEEP mode or during initial power-up.

        Preliminary
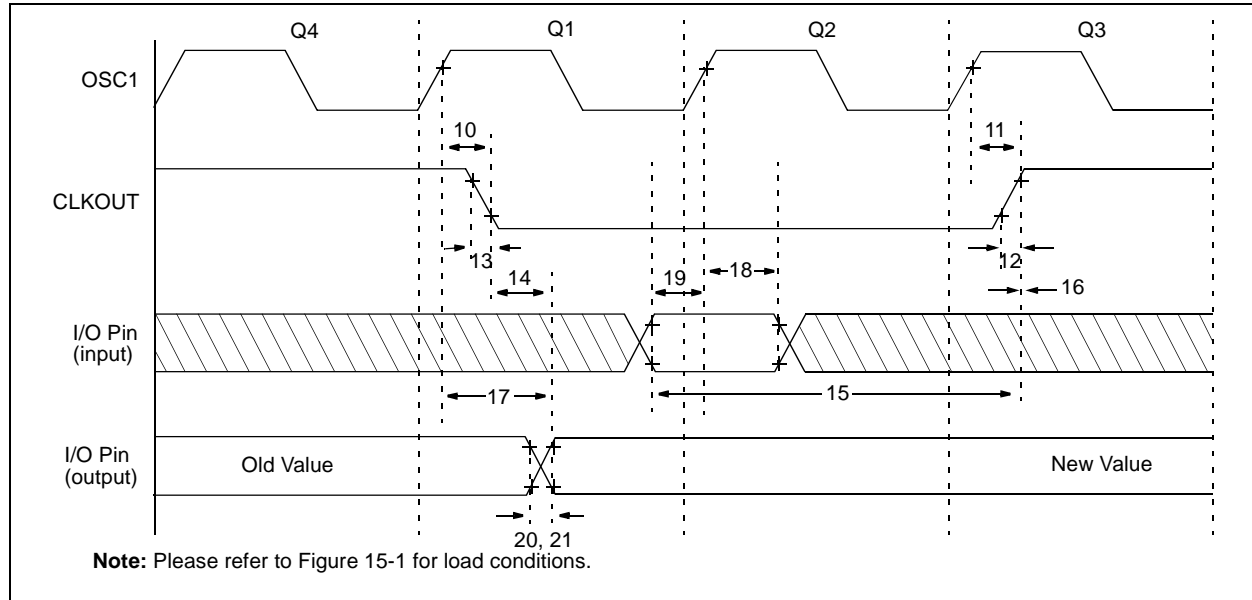
FIGURE 15-3: **CLKOUT AND I/O TIMING - PIC16C54A**

Note: Please refer to Figure 15-1 for load conditions.

TABLE 15-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54A

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \leq T_A \leq +70°C$ for commercial $-40°C \leq T_A \leq +85°C$ for industrial $-20°C \leq T_A \leq +85°C$ for industrial - PIC16LV54A-02I $-40°C \leq T_A \leq +125°C$ for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓[1]	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑[1]	—	15	30**	ns
12	TckR	CLKOUT rise time[1]	—	5.0	15**	ns
13	TckF	CLKOUT fall time[1]	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid[1]	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑[1]	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑[1]	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid[2]	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time[2]	—	10	25**	ns
21	TioF	Port output fall time[2]	—	10	25**	ns

  * These parameters are characterized but not tested.

  ** These parameters are design targets and are not tested. No characterization data available at this time.

    † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

    2: Please refer to Figure 15-1 for load conditions.

FIGURE 16-18: **TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. V$_{DD}$**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean − 3s (-40°C to 125°C)
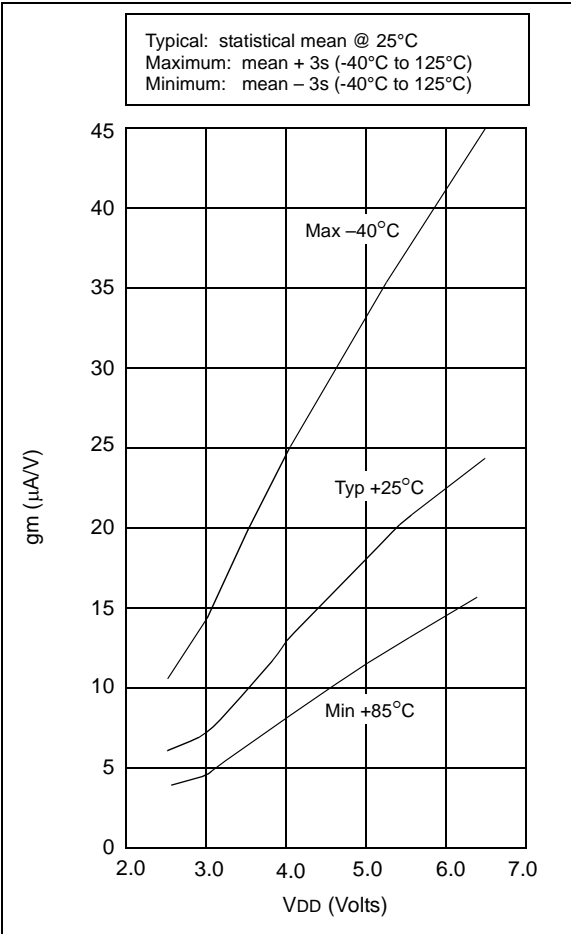
FIGURE 16-19: **TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. V$_{DD}$**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean − 3s (-40°C to 125°C)
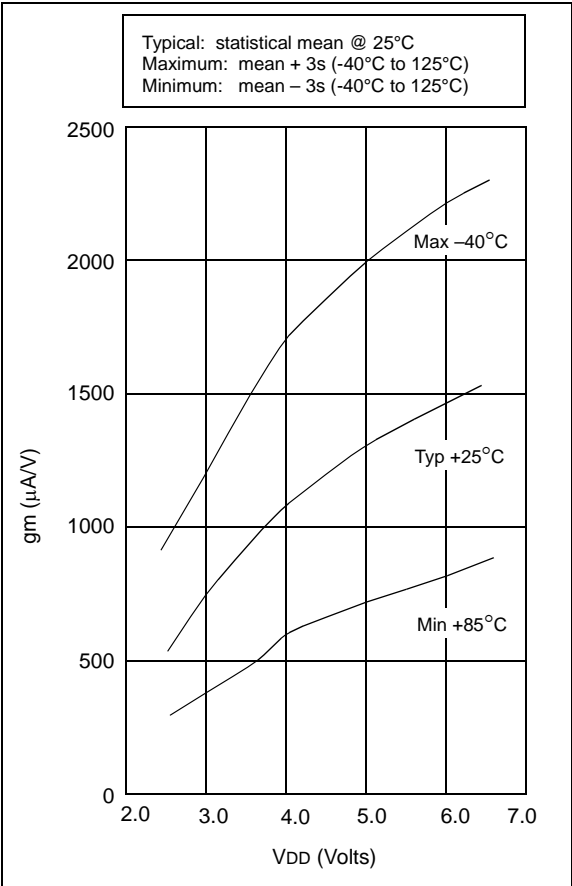
FIGURE 17-3: **PIC16LC54C/55A/56A/57C/58B VOLTAGE-FREQUENCY GRAPH,**
0°C ≤ T$_A$ ≤ +85°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
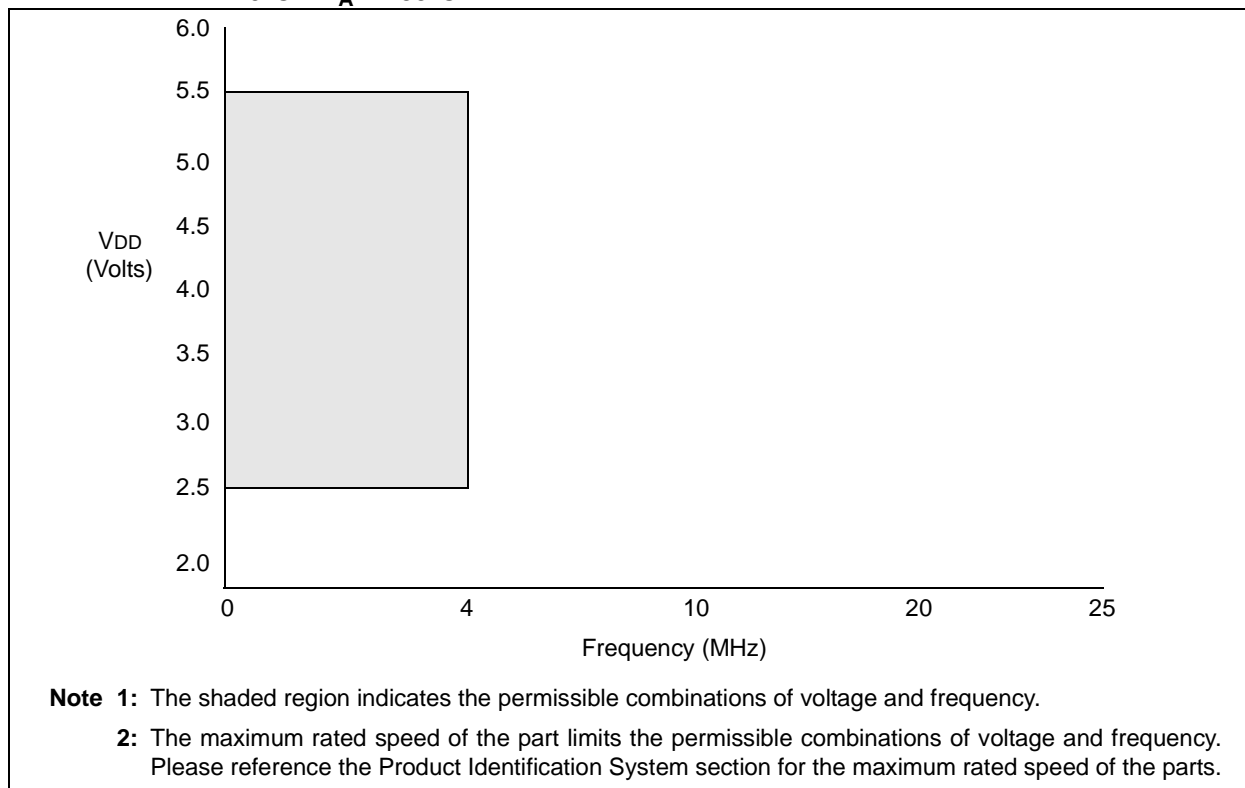
FIGURE 17-4: **PIC16LC54C/55A/56A/57C/58B VOLTAGE-FREQUENCY GRAPH,**
-40°C ≤ T$_A$ ≤ 0°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
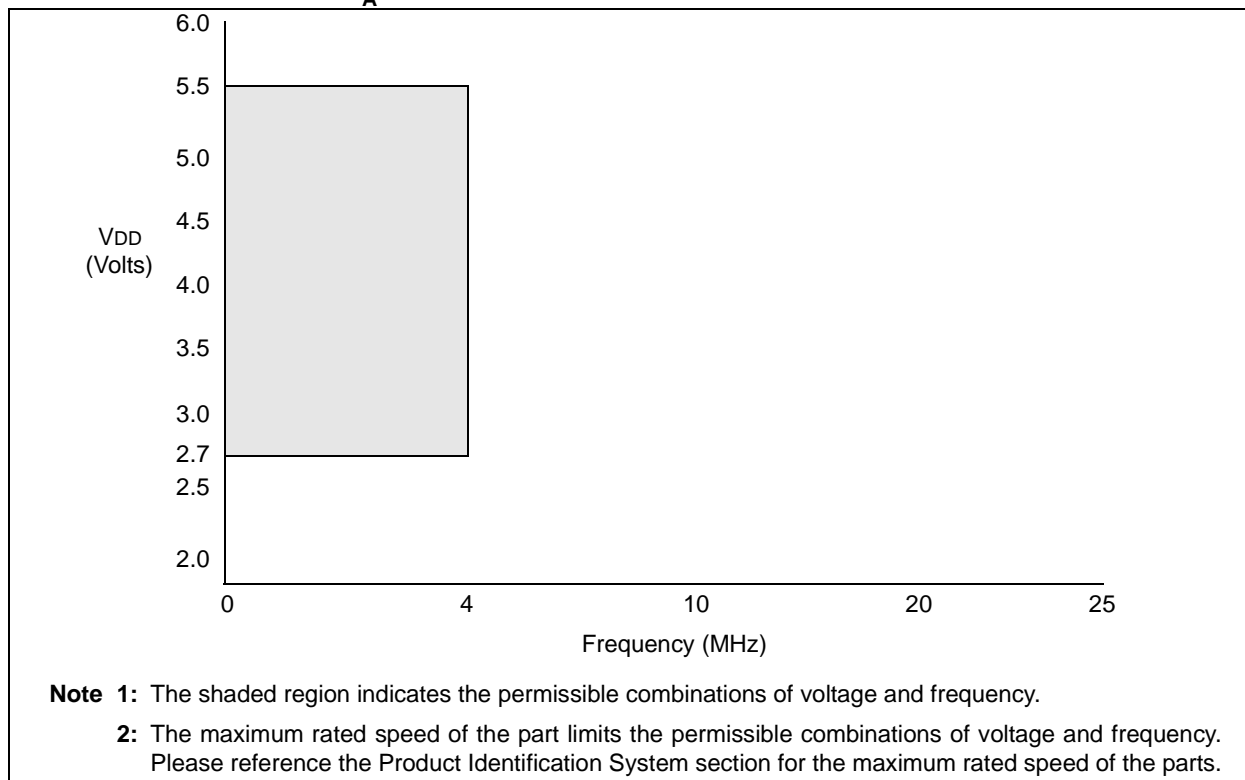
17.2   DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended)
PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)							Standard Operating Conditions (unless otherwise specified) Operating Temperature −40°C ≤ TA ≤ +125°C for extended
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	**Supply Voltage**	3.0 4.5	— —	5.5 5.5	V V	RC, XT, LP, and HS mode from 0 - 10 MHz from 10 - 20 MHz
D002	VDR	**RAM Data Retention Voltage**[1]	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD start voltage** to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD rise rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	**Supply Current**[2] XT and RC[3] modes HS mode	— —	1.8 9.0	3.3 20	mA mA	FOSC = 4.0 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V
D020	IPD	**Power-down Current**[2]	— — — — — —	0.3 10 12 4.8 18 26	17 50* 60* 31* 68* 90*	μA μA μA μA μA μA	VDD = 3.0V, WDT disabled VDD = 4.5V, WDT disabled VDD = 5.5V, WDT disabled VDD = 3.0V, WDT enabled VDD = 4.5V, WDT enabled VDD = 5.5V, WDT enabled

    *   These parameters are characterized but not tested.

    †   Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
     2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
         a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
         b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
     3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

17.4   Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
2	to	mc	$\overline{MCLR}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 17-5:   LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B-04, 20
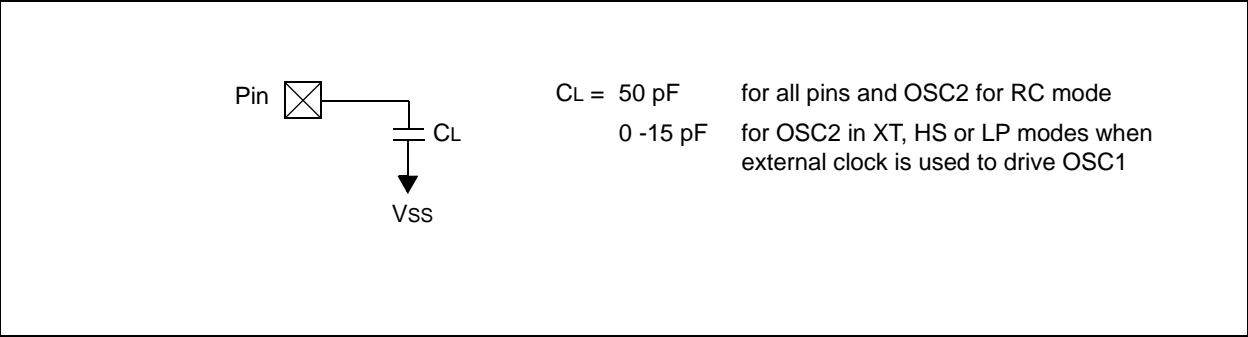
Pin

C_L

Vss

$C_L =$ 50 pF   for all pins and OSC2 for RC mode

0 -15 pF   for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \leq T_A \leq +70°C$ for commercial $-40°C \leq T_A \leq +85°C$ for industrial $-40°C \leq T_A \leq +125°C$ for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions	
2	Tcy	Instruction Cycle Time[2]	—	4/Fosc	—	—		
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator	
			20*	—	—	ns	HS oscillator	
			2.0*	—	—	μs	LP oscillator	
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator	
			—	—	25*	ns	HS oscillator	
			—	—	50*	ns	LP oscillator	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

PIC16C5X

FIGURE 17-9: **TIMER0 CLOCK TIMINGS - PIC16C5X, PIC16CR5X**

Note: Please refer to Figure 17-5 for load conditions.
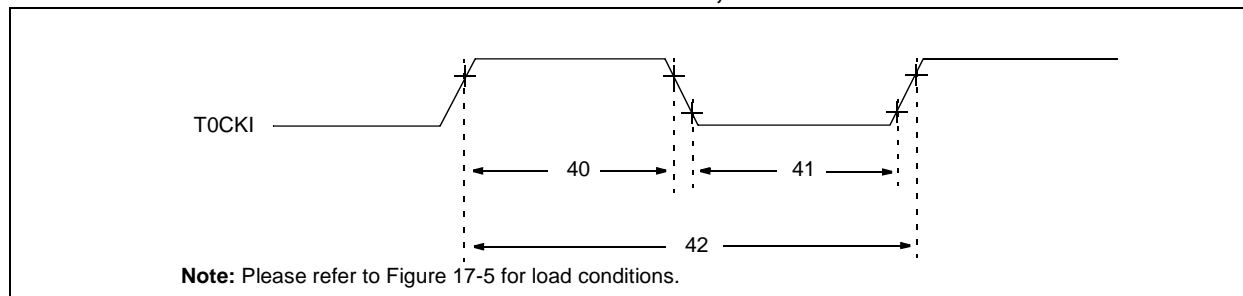
TABLE 17-4: **TIMER0 CLOCK REQUIREMENTS - PIC16C5X, PIC16CR5X**

AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature $\quad$ 0°C $\leq$ TA $\leq$ +70°C for commercial $\quad$ −40°C $\leq$ TA $\leq$ +85°C for industrial $\quad$ −40°C $\leq$ TA $\leq$ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width					
		$\quad$ - No Prescaler	0.5 TCY + 20*	—	—	ns	
		$\quad$ - With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width					
		$\quad$ - No Prescaler	0.5 TCY + 20*	—	—	ns	
		$\quad$ - With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	$\frac{20 \text{ or } \underline{\text{TCY} + 40}^*}{N}$	—	—	ns	Whichever is greater. N = Prescale Value $\quad$ (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 18-8: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. VDD

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)
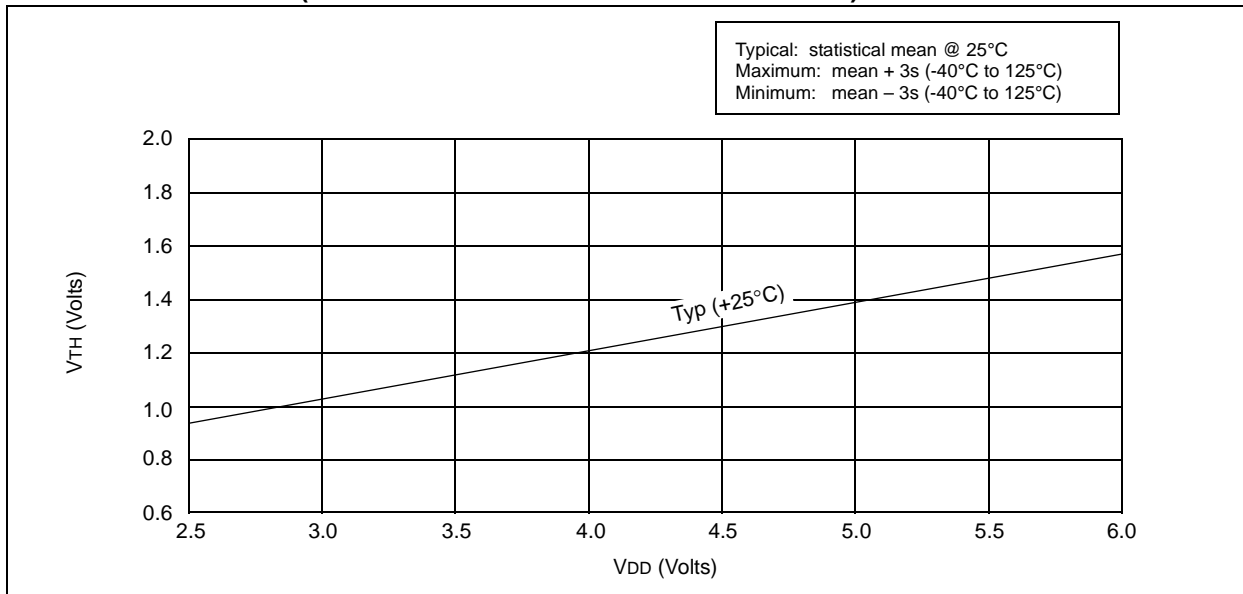
FIGURE 18-9: VIH, VIL OF MCLR, T0CKI AND OSC1 (IN RC MODE) vs. VDD

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Note: These input pins have Schmitt Trigger input buffers.
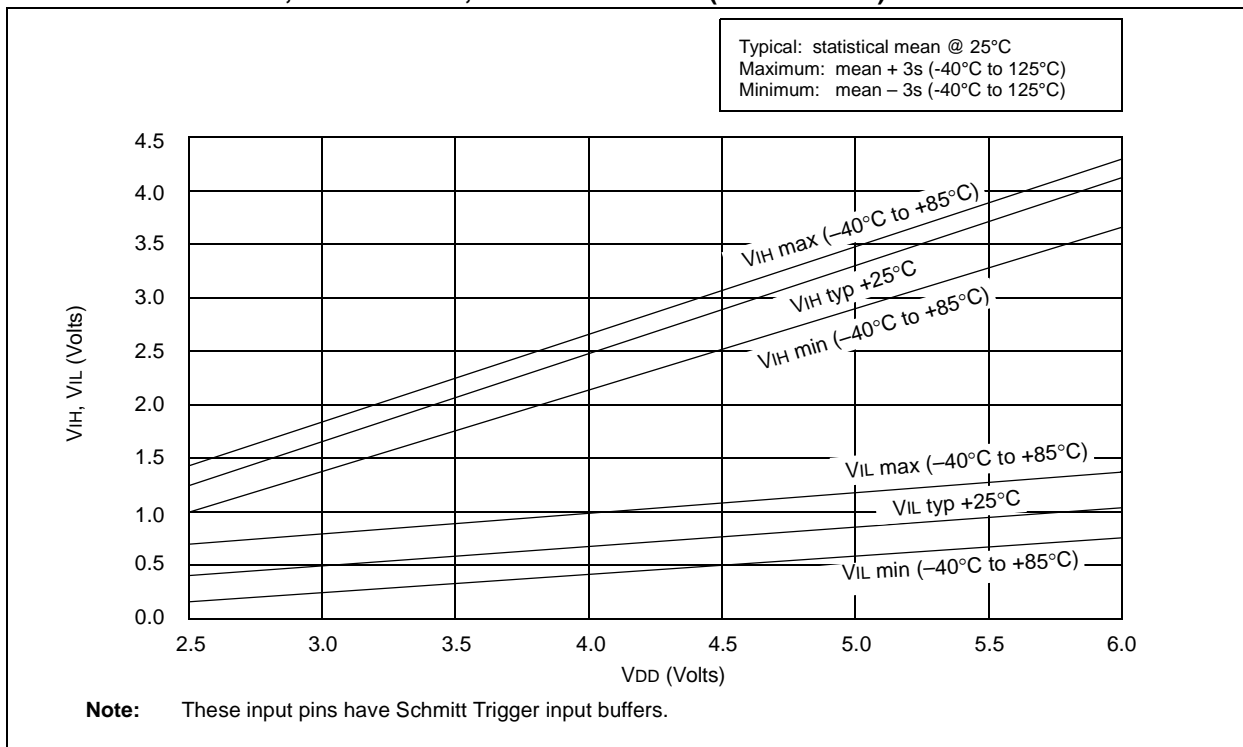
PIC16C5X

19.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)[1]

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $0°C \leq T_A \leq +70°C$ for commercial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	V$_{IL}$	**Input Low Voltage** I/O Ports $\overline{MCLR}$ (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1	Vss Vss Vss Vss	— — — —	0.8 0.15 V$_{DD}$ 0.15 V$_{DD}$ 0.2 V$_{DD}$	V V V V	4.5V <V$_{DD}$ ≤ 5.5V HS, 20 MHz ≤ F$_{OSC}$ ≤ 40 MHz
D040	V$_{IH}$	**Input High Voltage** I/O ports $\overline{MCLR}$ (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1	2.0 0.85 V$_{DD}$ 0.85 V$_{DD}$ 0.8 V$_{DD}$	— — — —	V$_{DD}$ V$_{DD}$ V$_{DD}$ V$_{DD}$	V V V V	4.5V < V$_{DD}$ ≤ 5.5V HS, 20 MHz ≤ F$_{OSC}$ ≤ 40 MHz
D050	V$_{HYS}$	**Hysteresis of Schmitt Trigger inputs**	0.15 V$_{DD}$*	—	—	V	
D060	I$_{IL}$	**Input Leakage Current[2,3]** I/O ports $\overline{MCLR}$ $\overline{MCLR}$ T0CKI OSC1	-1.0 -5.0 — -3.0 -3.0	0.5 — 0.5 0.5 0.5	+1.0 +5.0 +3.0 +3.0 —	μA μA μA μA μA	**For V$_{DD}$ ≤ 5.5V:** V$_{SS}$ ≤ V$_{PIN}$ ≤ V$_{DD}$, pin at hi-impedance V$_{PIN}$ = V$_{SS}$ +0.25V V$_{PIN}$ = V$_{DD}$ V$_{SS}$ ≤ V$_{PIN}$ ≤ V$_{DD}$ V$_{SS}$ ≤ V$_{PIN}$ ≤ V$_{DD}$, HS
D080	V$_{OL}$	**Output Low Voltage** I/O ports	—	—	0.6	V	I$_{OL}$ = 8.7 mA, V$_{DD}$ = 4.5V
D090	V$_{OH}$	**Output High Voltage[3]** I/O ports	V$_{DD}$ - 0.7	—	—	V	I$_{OH}$ = -5.4 mA, V$_{DD}$ = 4.5V

*   These parameters are characterized but not tested.

†   Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Device operation between 20 MHz to 40 MHz requires the following: V$_{DD}$ between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected and HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 17.3.

2: The leakage current on the $\overline{MCLR}$/V$_{PP}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

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FIGURE 20-2: **TYPICAL I**PD **vs. V**DD**, WATCHDOG ENABLED (25°C)**
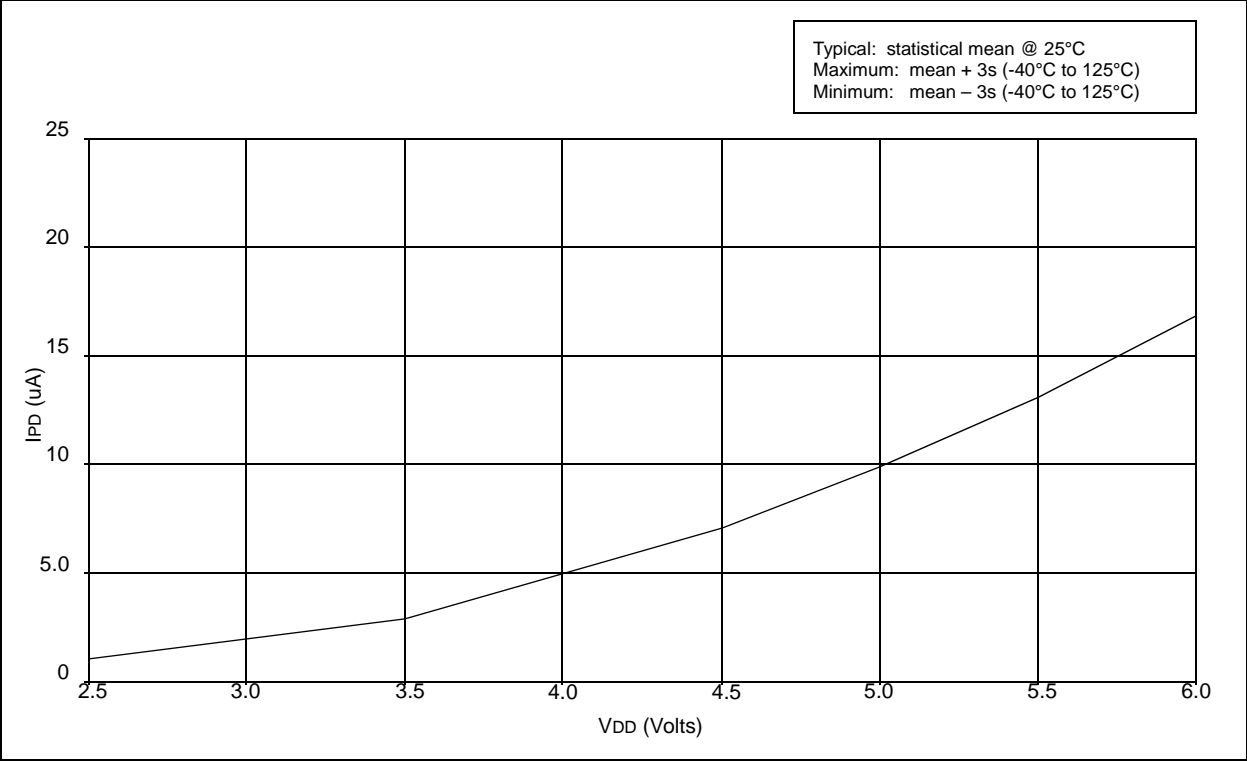
FIGURE 20-3: **TYPICAL I**PD **vs. V**DD**, WATCHDOG ENABLED (−40°C, 85°C)**

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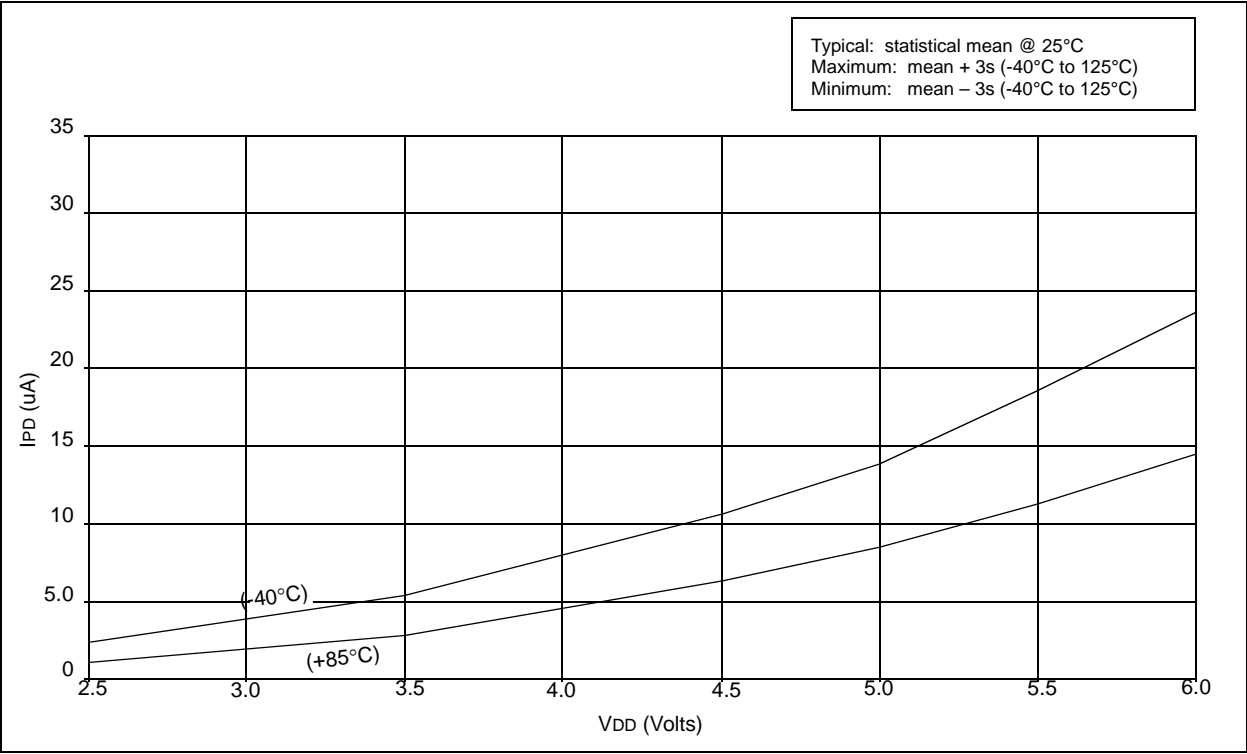
FIGURE 20-4: V_TH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. V_DD

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Typ (+25°C)

V_TH (Volts)

V_DD (Volts)
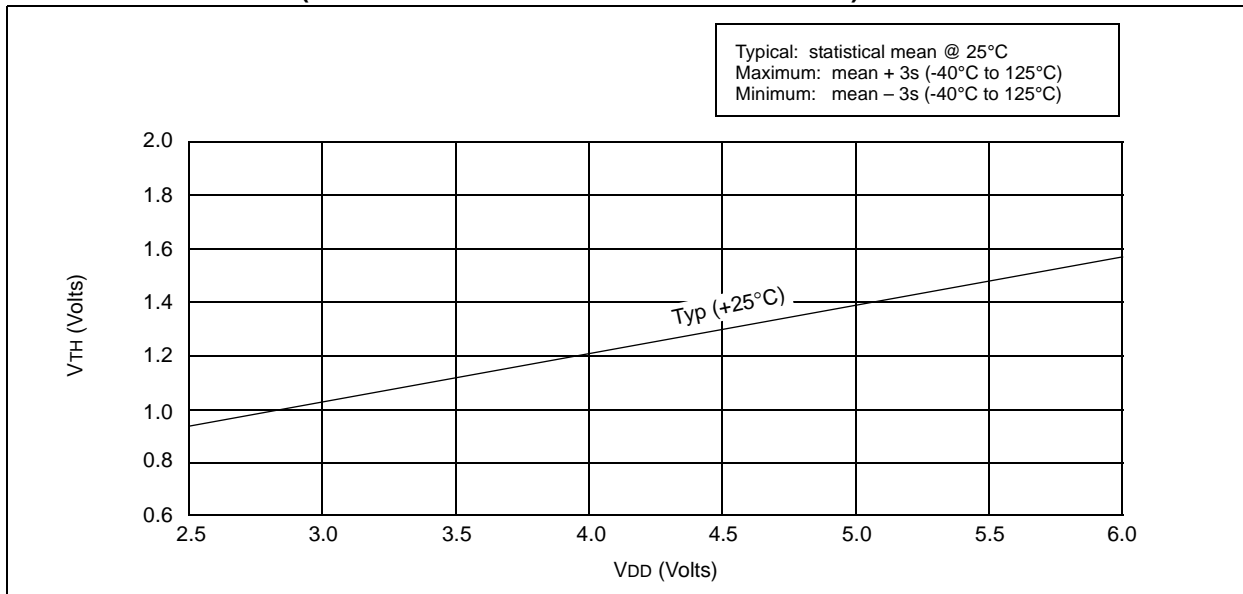
FIGURE 20-5: V_TH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (HS MODE) vs. V_DD

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Typ (+25°C)

V_TH (Volts)

V_DD (Volts)
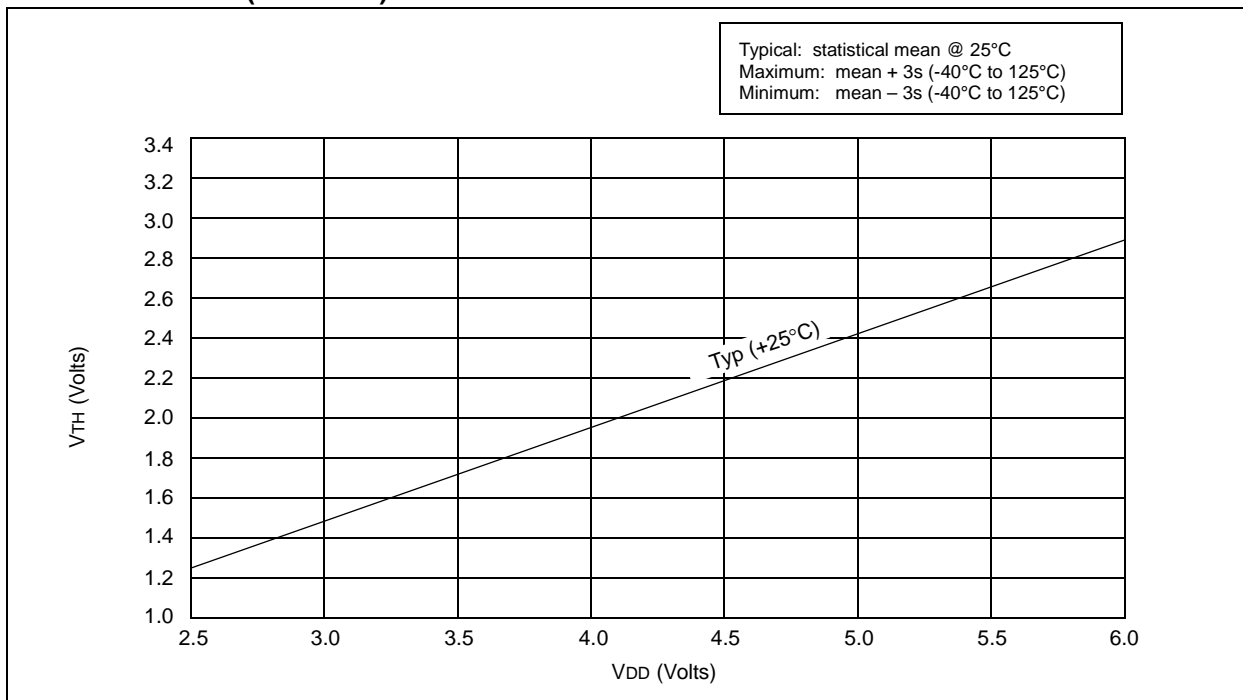
FIGURE 20-7: WDT TIMER TIME-OUT PERIOD vs. V_{DD}[1]

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean − 3s (-40°C to 125°C)

Note 1: Prescaler set to 1:1.
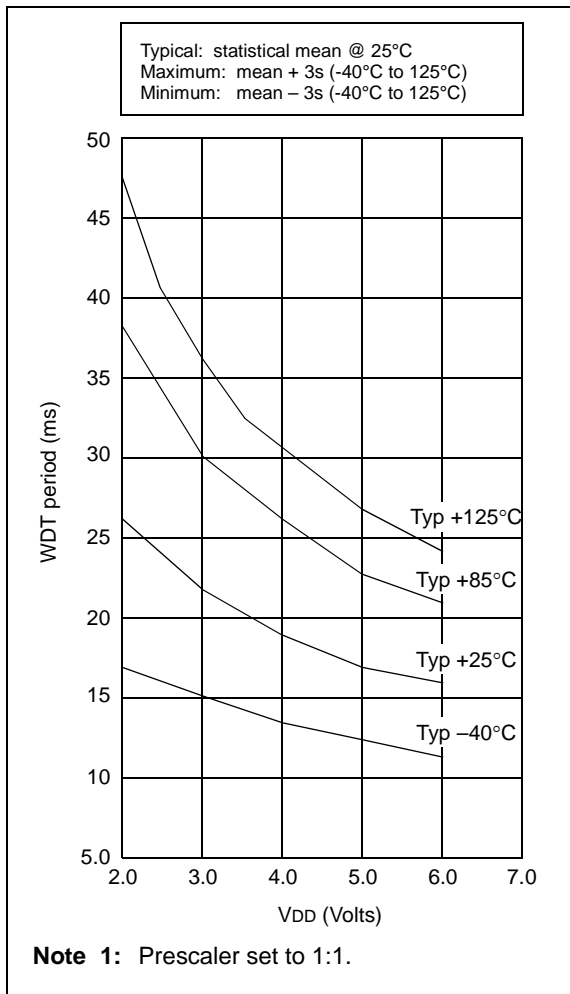
FIGURE 20-8: I_{OH} vs. V_{OH}, V_{DD} = 5 V

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean − 3s (-40°C to 125°C)
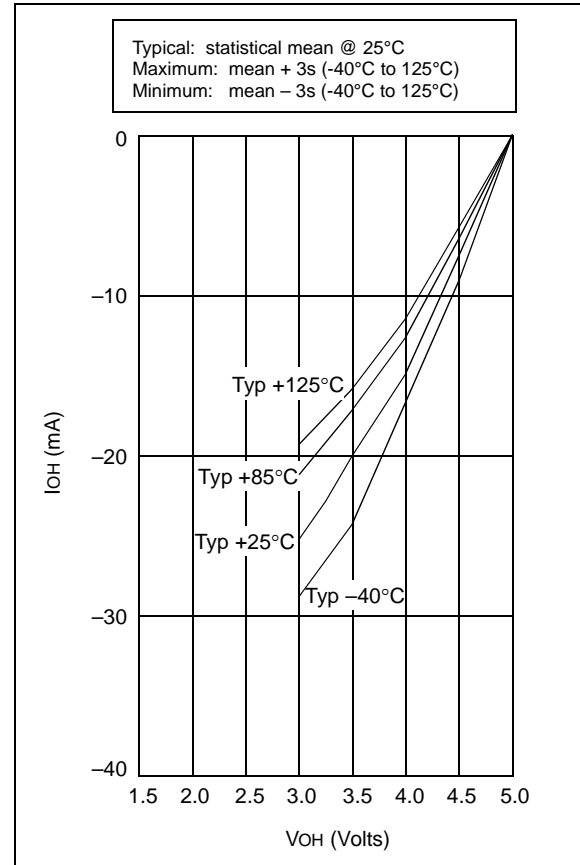
TABLE 20-1: INPUT CAPACITANCE

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
MCLR	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

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FIGURE 20-9: **I_{OL} vs. V_{OL}, V_{DD} = 5 V**

FIGURE 20-9: I_{OL} vs. V_{OL}, V_{DD} = 5 V

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