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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57c-04e-p

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Pin Diagrams



Device Differences

Device	Voltage Range	Oscillator Selection (Program)	Oscillator	Process Technology (Microns)	ROM Equivalent	MCLR Filter
PIC16C54	2.5-6.25	Factory	See Note 1	1.2	PIC16CR54A	No
PIC16C54A	2.0-6.25	User	See Note 1	0.9	—	No
PIC16C54C	2.5-5.5	User	See Note 1	0.7	PIC16CR54C	Yes
PIC16C55	2.5-6.25	Factory	See Note 1	1.7	_	No
PIC16C55A	2.5-5.5	User	See Note 1	0.7	—	Yes
PIC16C56	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C56A	2.5-5.5	User	See Note 1	0.7	PIC16CR56A	Yes
PIC16C57	2.5-6.25	Factory	See Note 1	1.2	—	No
PIC16C57C	2.5-5.5	User	See Note 1	0.7	PIC16CR57C	Yes
PIC16C58B	2.5-5.5	User	See Note 1	0.7	PIC16CR58B	Yes
PIC16CR54A	2.5-6.25	Factory	See Note 1	1.2	N/A	Yes
PIC16CR54C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR56A	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR57C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR58B	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

Note: The table shown above shows the generic names of the PIC16C5X devices. For device varieties, please refer to Section 2.0.

3.1 **Clocking Scheme/Instruction** Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2 and Example 3-1.

3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).



FIGURE 3-2: **CLOCK/INSTRUCTION CYCLE**

EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



is "flushed" from the pipeline, while the new instruction is being fetched and then executed.

4.0 OSCILLATOR CONFIGURATIONS

4.1 Oscillator Types

PIC16C5Xs can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- 1. LP: Low Power Crystal
- 2. XT: Crystal/Resonator
- 3. HS: High Speed Crystal/Resonator
- 4. RC: Resistor/Capacitor

Note: Not all oscillator selections available for all parts. See Section 9.1.

4.2 Crystal Oscillator/Ceramic Resonators

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 4-1). The PIC16C5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 4-2).

FIGURE 4-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



FIGURE 4-2:

EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)



TABLE 4-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS -PIC16C5X, PIC16CR5X

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	68-100 pF	68-100 pF
	2.0 MHz	15-33 pF	15-33 pF
	4.0 MHz	10-22 pF	10-22 pF
HS	8.0 MHz	10-22 pF	10-22 pF
	16.0 MHz	10 pF	10 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 4-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR -PIC16C5X. PIC16CR5X

Osc Type	Crystal Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz ⁽¹⁾	15 pF	15 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Note 1: For VDD > 4.5V, C1 = C2 \approx 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

Note: If you change from this device to another device, please verify oscillator characteristics in your application.

6.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 6-1).

The Special Registers can be classified into two sets. The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Details on Page
N/A	TRIS	I/O Cont	/O Control Registers (TRISA, TRISB, TRISC)							1111 1111	35
N/A	OPTION	Contains	s control b	oits to cor	figure Ti	mer0 and	Timer0/V	VDT pres	caler	11 1111	30
00h	INDF	Uses co	ntents of	FSR to ac	ddress da	ata memo	ory (not a	physical ı	egister)	XXXX XXXX	32
01h	TMR0	Timer0 I	Timer0 Module Register							XXXX XXXX	38
02h ⁽¹⁾	PCL	Low ord	er 8 bits c	of PC						1111 1111	31
03h	STATUS	PA2	PA1	PA0	TO	PD	Z	DC	С	0001 1xxx	29
04h	FSR	Indirect	Indirect data memory address pointer						•	1xxx xxxx (3)	32
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	xxxx	35
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	XXXX XXXX	35
07h ⁽²⁾	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	XXXX XXXX	35

|--|

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 6.5 for an explanation of how to access these bits.

2: File address 07h is a General Purpose Register on the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16CR58 and PIC16CR58.

3: These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for MCLR and WDT Reset, the value is 111u uuuu.

GOTO	Unconditional Branch							
Syntax:	[label]	GOTO	k					
Operands:	$0 \le k \le 511$							
Operation:	$k \rightarrow PC < 8:0>;$ STATUS<6:5> $\rightarrow PC < 10:9>$							
Status Affected:	None							
Encoding:	101k	kkkk	kkkk					
Description:	GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two- cycle instruction.							
Words:	1							
Cycles:	2							
Example:	GOTO TH	IERE						
After Instructi PC =	on address	G (THER	E)					

INCF	Increment f
Syntax:	[label] INCF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$
Operation:	(f) + 1 \rightarrow (dest)
Status Affected:	Z
Encoding:	0010 10df ffff
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
Words:	1
Cycles:	1
Example:	INCF CNT, 1
Before Instru CNT Z After Instructi CNT Z	ction = 0xFF = 0 ion = 0x00 = 1

INCFSZ	Increment f, Skip if 0					
Syntax:	[label] INCFSZ f,d					
Operands:	$\begin{array}{l} 0\leq f\leq 31\\ d\in [0,1] \end{array}$					
Operation:	(f) + 1 \rightarrow (dest), skip if result = 0					
Status Affected:	None					
Encoding:	0011 11df ffff					
Description:	I he contents of register 't' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-					
Words:	1					
Cycles:	1(2)					
Example:	HERE INCFSZ CNT, 1 GOTO LOOP					
	CONTINUE • • •					
Before Instru	iction					
PC	= address (HERE)					
After Instruct	ion					
CNT	= CNT + 1;					
if CNT	= 0,					
PC	= address (CONTINUE);					
if CNT	≠ 0, 					
PC	= address (HERE +1)					

11.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PIC MCUs and can be used to develop for this and other PIC microcontrollers. The MPLAB ICD utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial ProgrammingTM protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

11.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in Stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable VDD and VPP supplies, which allow it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In Stand-alone mode, the PRO MATE II device programmer can read, verify, or program PIC devices. It can also set code protection in this mode.

11.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PIC devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

11.11 PICDEM 1 Low Cost PIC MCU Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A). PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE incircuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

11.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I^2C^{TM} bus and separate headers for connection to an LCD module and a keypad.

11.13 PICDEM 3 Low Cost PIC16CXXX Demonstration Board

The PICDEM 3 demonstration board is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with an LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 3 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer with an adapter socket, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 3 demonstration board to test firmware. A prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM 3 demonstration board is a LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM 3 demonstration board provides an additional RS-232 interface and Windows software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

11.14 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included and the user may erase it and program it with the other sample programs using the PRO MATE II device programmer, or the PICSTART Plus development programmer, and easily debug and test the sample code. In addition, the PICDEM 17 demonstration board supports downloading of programs to and executing out of external FLASH memory on board. The PICDEM 17 demonstration board is also usable with the MPLAB ICE in-circuit emulator, or the PICMASTER emulator and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

11.15 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchip's HCS Secure Data Products. The HCS evaluation kit includes a LCD display to show changing codes, a decoder to decode transmissions and a programming interface to program test transmitters.

13.3 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

DC CH	DC CHARACTERISTICS			$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array} $					
Param No.	Symbol	Characteristic Min T		Typ† Max		Units	Conditions		
D030	VIL	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD	> > > > >	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes		
D040	Vih	Input High Voltage I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	2.0 0.6 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD		VDD VDD VDD VDD VDD VDD	V V V V V	VDD = 3.0V to 5.5V ⁽⁴⁾ Full VDD range ⁽⁴⁾ RC mode only ⁽³⁾ XT, HS and LP modes		
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	_	_	V			
D060	lı∟	Input Leakage Current ^(1,2) I/O ports	-1.0	_	+1.0	μA	For VDD \leq 5.5V: VSS \leq VPIN \leq VDD, pin at hi-impedance		
		MCLR MCLR TOCKI OSC1	-5.0 -3.0 -3.0	 0.5 0.5 0.5		μΑ μΑ μΑ μΑ	$VPIN = VSS + 0.25V$ $VPIN = VDD$ $VSS \le VPIN \le VDD$ $VSS \le VPIN \le VDD,$ $XT, HS and LP modes$		
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.5 0.5	V V	IOL = 10 mA, VDD = 6.0 V IOL = 1.9 mA, VDD = 6.0 V, RC mode only		
D090	Vон	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	Vdd – 0.5 Vdd – 0.5	_		V V	IOH = -4.0 mA, VDD = 6.0 V IOH = -0.8 mA, VDD = 6.0 V, RC mode only		

* These parameters are characterized but not tested.

- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- **Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
 - 2: Negative current is defined as coming out of the pin.
 - **3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
 - 4: The user may use the better of the two specifications.



FIGURE 13-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR54A

TABLE 13-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR54A

AC Characteristics $\begin{array}{c} \mbox{Standard Operating Conditions (unless otherwise specified)}\\ Operating Temperature & 0°C \leq TA \leq +70°C for commercial \\ -40°C \leq TA \leq +85°C for industrial \\ -40°C \leq TA \leq +125°C for extended \end{array}$							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1.0*	_	_	μS	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7.0*	18*	40*	ms	VDD = 5.0V (Comm)
32	Tdrt	Device Reset Timer Period	7.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	_	_	1.0*	μS	

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

15.3 DC Characteristics: PIC16LV54A-02 (Commercial) PIC16LV54A-02I (Industrial)

PIC16LV54A-02 PIC16LV54A-02I (Commercial, Industrial)									
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions		
D001	Vdd	Supply Voltage RC and XT modes	2.0	_	3.8	V			
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode		
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	-	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset		
D010	IDD	Supply Current⁽²⁾ RC ⁽³⁾ and XT modes LP mode, Commercial LP mode, Industrial		0.5 11 14	 27 35	mA μA μA	Fosc = 2.0 MHz, VDD = 3.0V Fosc = 32 kHz, VDD = 2.5V WDT disabled Fosc = 32 kHz, VDD = 2.5V WDT disabled		
D020	IPD	Power-down Current^(2,4) Commercial Commercial Industrial Industrial		2.5 0.25 3.5 0.3	12 4.0 14 5.0	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled		

These parameters are characterized but not tested.

- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- **Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.
 - 4: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection on wake-up from SLEEP mode or during initial power-up.

15.6 Timing Diagrams and Specifications

FIGURE 15-2: EXTERNAL CLOCK TIMING - PIC16C54A



TABLE 15-1:	EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

AC Chara	acteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
	Fosc	External CLKIN Fre-	DC		4.0	MHz	XT OSC mode	
		quency ⁽¹⁾	DC	—	2.0	MHz	XT osc mode (PIC16LV54A)	
			DC	—	4.0	MHz	HS osc mode (04)	
			DC	—	10	MHz	HS osc mode (10)	
			DC	—	20	MHz	HS osc mode (20)	
			DC	—	200	kHz	LP osc mode	
	Oscillator Freque		DC	_	4.0	MHz	RC osc mode	
			DC	—	2.0	MHz	RC osc mode (PIC16LV54A)	
			0.1	—	4.0	MHz	XT osc mode	
			0.1	—	2.0	MHz	XT osc mode (PIC16LV54A)	
			4.0	—	4.0	MHz	HS osc mode (04)	
			4.0	—	10	MHz	HS osc mode (10)	
			4.0	—	20	MHz	HS osc mode (20)	
			5.0		200	kHz	LP osc mode	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.
 - Instruction cycle period (TcY) equals four times the input oscillator time base period.

16.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.



FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

TABLE 16-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Ave Fosc @	rage 5 V, 25°C
20 pF	3.3K	5 MHz	± 27%
	5K	3.8 MHz	± 21%
	10K	2.2 MHz	± 21%
	100K	262 kHz	± 31%
100 pF	3.3K	1.6 MHz	± 13%
	5K	1.2 MHz	± 13%
	10K	684 kHz	± 18%
	100K	71 kHz	± 25%
300 pF	3.3K	660 kHz	± 10%
	5.0K	484 kHz	± 14%
	10K	267 kHz	± 15%
	100K	29 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for VDD = 5V.



FIGURE 16-12: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 PF, 25°C)

FIGURE 16-13: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 PF, -40°C to +85°C)



19.0 ELECTRICAL CHARACTERISTICS - PIC16LC54C 40MHz

Absolute Maximum Ratings^(†)

Ambient temperature under bias	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	
Total power dissipation ⁽¹⁾	
Max. current out of Vss pin	
Max. current into Vod pin	
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, IIK (VI < 0 or VI > VDD)	±20 mA
Output clamp current, Iок (Vo < 0 or Vo > Voo)	±20 mA
Max. output current sunk by any I/O pin	
Max. output current sourced by any I/O pin	
Max. output current sourced by a single I/O (Port A, B or C)	
Max. output current sunk by a single I/O (Port A, B or C)	
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH} + \sum {(VI	ор-Voн) x Ioн} + ∑(Vol x Iol)

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



	ALVAUT AND VA THING BEALIDENENTS - DIA AASY (A
TABLE 19-2:	CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X-40

AC Chara	acteristics	Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units			
10	TosH2ckL	OSC1↑ to CLKOUT↓ ^(1,2)		15	30**	ns			
11	TosH2ckH	OSC1↑ to CLKOUT↑ ^(1,2)	—	15	30**	ns			
12	TckR	CLKOUT rise time ^(1,2)	—	5.0	15**	ns			
13	TckF	CLKOUT fall time ^(1,2)	—	5.0	15**	ns			
14	TckL2ioV	CLKOUT↓ to Port out valid ^(1,2)	—		40**	ns			
15	TioV2ckH	Port in valid before CLKOUT ^(1,2)	0.25 TCY+30*	—	—	ns			
16	TckH2iol	Port in hold after CLKOUT ^(1,2)	0*	—	—	ns			
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽²⁾	—	—	100	ns			
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns			
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—		ns			
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns			
21	TioF	Port output fall time ⁽²⁾		10	25**	ns			

* These parameters are characterized but not tested.

- ** These parameters are design targets and are not tested. No characterization data available at this time.
- † Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Refer to Figure 19-2 for load conditions.

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NOTES:

FIGURE 20-9: IOL vs. VOL, VDD = 5 V



18-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging



	INCHES*			MILLIMETERS			
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	р		.050			1.27	
Overall Height	Α	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	¢	0	4	8	0	4	8
Lead Thickness	С	.009	.011	.012	0.23	0.27	0.30
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013 Drawing No. C04-051

20-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	INCHES*			MILLIMETERS			
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	р		.026			0.65	
Overall Height	А	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	Е	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25
Foot Angle	φ	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-150 Drawing No. C04-072

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