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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57c-04e-sp

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

4.3 External Crystal Oscillator Circuit

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A welldesigned crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 4-3 shows an implementation example of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 k Ω resistor provides the negative feedback for stability. The 10 k Ω potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 4-3: EXAMPLE OF EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)



Figure 4-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 k Ω resistors provide the negative feedback to bias the inverters in their linear region.



6.4 **OPTION Register**

The OPTION Register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W Register will be transferred to the OPTION Register. A RESET sets the OPTION<5:0> bits.

REGISTER 6-2: OPTION REGISTER

U-0	U-0	W-1	W-1	W-1	W-1	W-1	W-1
_	—	T0CS	TOSE	PSA	PS2	PS1	PS0
bit 7							bit 0

- bit 7-6: Unimplemented: Read as '0'
- bit 5: **TOCS**: Timer0 clock source select bit
 - 1 = Transition on T0CKI pin
 - 0 = Internal instruction cycle clock (CLKOUT)
- bit 4: **TOSE**: Timer0 source edge select bit
 - 1 = Increment on high-to-low transition on T0CKI pin
 - 0 = Increment on low-to-high transition on T0CKI pin
- bit 3: **PSA**: Prescaler assignment bit
 - 1 = Prescaler assigned to the WDT
 - 0 = Prescaler assigned to Timer0

bit 2-0: **PS<2:0>:** Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1:64	1:32
110	1 : 128	1:64
111	1 : 256	1 : 128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

8.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

8.1.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 8-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

8.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 8-5 shows the delay from the external clock edge to the timer incrementing.



the error in measuring the interval between two edges on Timer0 input = ± 4 Tosc max.

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12.3 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions	
D001	Vdd	Supply Voltage PIC16C5X-RCE PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-LPE	3.25 3.25 4.5 4.5 2.5		6.0 6.0 5.5 5.5 6.0	V V V V V		
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	_	V	Device in SLEEP mode	
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset	
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset	
D010	IDD	Supply Current ⁽²⁾ PIC16C5X-RCE ⁽³⁾ PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-HSE PIC16C5X-LPE		1.8 1.8 4.8 9.0 19	3.3 3.3 10 10 20 55	mA mA mA mA μA	Fosc = 4 MHz, VDD = $5.5V$ Fosc = 4 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 16 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $3.25V$, WDT disabled	
D020	IPD	Power-down Current ⁽²⁾	_	5.0 0.8	22 18	μΑ μΑ	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled	

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .



TABLE 13-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR54A

AC Chara	acteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$	s otherwise sp ≤ +70°C for com ≤ +85°C for indu ≤ +125°C for ext	ecified) mercial strial ended		
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units
10	TosH2ckL	OSC1 [↑] to CLKOUT↓ ⁽¹⁾	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	_	40**	ns
15	TioV2ckH	Port in valid before CLKOUT ⁽¹⁾	0.25 TCY+30*	_	_	ns
16	TckH2iol	Port in hold after CLKOUT ⁽¹⁾	0*	_	_	ns
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽²⁾	—	_	100*	ns
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD		_	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD		_	ns
20	TioR	Port output rise time ⁽²⁾		10	25**	ns
21	TioF	Port output fall time ⁽²⁾	_	10	25**	ns

* These parameters are characterized but not tested.

- ** These parameters are design targets and are not tested. No characterization data available at this time.
- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Please refer to Figure 13.1 for load conditions.

FIGURE 14-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD









FIGURE 14-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD



15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16L0 PIC16L0 (Comm	PIC16LC54A-04 PIC16LC54A-04I (Commercial, Industrial)				perating	j Cond i ure 	itions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $40^{\circ}C \le TA \le +85^{\circ}C$ for industrial	
PIC16C PIC16C (Comm	PIC16C54A-04, 10, 20 PIC16C54A-04I, 10I, 20I (Commercial, Industrial)			$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)}\\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$				
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions	
	Vdd	Supply Voltage						
D001		PIC16LC54A	3.0 2.5	_	6.25 6.25	V V	XT and RC modes LP mode	
D001A		PIC16C54A	3.0 4.5	_	6.25 5.5	V V	RC, XT and LP modes HS mode	
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode	
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset	
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	-	V/ms	See Section 5.1 for details on Power-on Reset	
	IDD	Supply Current ⁽²⁾						
D005		PIC16LC5X	_	0.5	2.5	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes	
				11	27	μΑ	Fosc = 32 kHz, VDD = 2.5V, WDT disabled, LP mode, Commercial	
			_	11	35	μΑ	Fosc = 32 kHz, VDD = 2.5V, WDT disabled, LP mode, Industrial	
D005A		PIC16C5X	—	1.8	2.4	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes	
			—	2.4	8.0	mA	FOSC = 10 MHz, VDD = 5.5V, HS mode	
			—	4.5	16	mA	FOSC = 20 MHz, VDD = 5.5V, HS mode	
				14	29	μA	HOSC = 32 kHz, VDD = 3.0V,	
			-	17	37	μΑ	Fosc = 32 kHz, VDD = 3.0V, WDT disabled, LP mode, Industrial	

Legend: Rows with standard voltage device data only are shaded for improved readability.

These parameters are characterized but not tested.

- † Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- **Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04Standard Operating Conditions (unless other Operating TemperaturePIC16LC54A-04I (Commercial, Industrial)0°C ≤ TA ≤ +70°C -40°C ≤ TA ≤ +85°C					tions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $40^{\circ}C \le TA \le +85^{\circ}C$ for industrial			
PIC16C54A-04, 10, 20 PIC16C54A-04I, 10I, 20I (Commercial, Industrial)				ard Ope ting Tem	perating	J Condi ure 	tions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $40^{\circ}C \le TA \le +85^{\circ}C$ for industrial	
Param No.	Symbol	Characteristic/Device	Min Typ† Max Units Conditions					
	IPD	Power-down Current ⁽²⁾						
D006		PIC16LC5X	—	2.5	12	μΑ	VDD = 2.5V, WDT enabled, Commercial	
			—	0.25	4.0	μΑ	VDD = 2.5V, WDT disabled, Commercial	
			_	0.25	5.0	μΑ μΑ	VDD = 2.5V, WDT enabled, industrial $VDD = 2.5V$, WDT disabled, Industrial	
D006A		PIC16C5X	_	4.0	12	μΑ	VDD = 3.0V, WDT enabled, Commercial	
			—	0.25	4.0	μA	VDD = 3.0V, WDT disabled, Commercial	
			—	5.0	14	μΑ	VDD = 3.0V, WDT enabled, Industrial	
				0.3	5.0	μA	$v \Box U = 3.0v, v U T uisabled, industrial$	

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

15.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended) PIC16LC54A-04E (Extended)

PIC16I	C54A-04F	•	Stand	, ard One	ratino	, Condi	tions (unless otherwise specified)		
(Exten	ded)	-	Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended						
PIC16C54A-04E, 10E, 20E (Extended)			Standard Operating Conditions (unless otherwise specified Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended						
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions		
	Vdd	Supply Voltage							
D001		PIC16LC54A	3.0 2.5		6.25 6.25	V V	XT and RC modes LP mode		
D001A		PIC16C54A	3.5 4.5		5.5 5.5	V V	RC and XT modes HS mode		
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾		1.5*	—	V	Device in SLEEP mode		
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	-	Vss	_	V	See Section 5.1 for details on Power-on Reset		
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset		
	IDD	Supply Current ⁽²⁾							
D010		PIC16LC54A	-	0.5	25	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes		
			-	11	27	μA	Fosc = 32 kHz, VDD = 2.5V, LP mode, Commercial		
				11	35	μA	Fosc = 32 kHz, VDD = 2.5V, LP mode, Industrial		
			—	11	37	μA	Fosc = 32 kHz, VDD = 2.5V, LP mode, Extended		
D010A		PIC16C54A	—	1.8	3.3	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes		
			-	4.8	10	mA	Fosc = 10 MHz, VDD = 5.5V, HS mode		
			-	9.0	20	mA	Fosc = 20 MHz, VDD = 5.5V, HS mode		

Legend: Rows with standard voltage device data only are shaded for improved readability.

- * These parameters are characterized but not tested.
- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.



FIGURE 16-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD





FIGURE 16-21: PORTA, B AND C IOH vs. VOH, VDD = 5V



PIC16C5X







2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.





2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency.

Please reference the Product Identification System section for the maximum rated speed of the parts.



FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 PF, 25°C







	ALVAUT AND VA TIMINA DEALIDEMENTA DIA AASY (A
TABLE 19-2:	CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X-40

AC Chara	acteristics	Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial								
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units				
10	TosH2ckL	OSC1↑ to CLKOUT↓ ^(1,2)		15	30**	ns				
11	TosH2ckH	OSC1↑ to CLKOUT↑ ^(1,2)	—	15	30**	ns				
12	TckR	CLKOUT rise time ^(1,2)	—	5.0	15**	ns				
13	TckF	CLKOUT fall time ^(1,2)	—	5.0	15**	ns				
14	TckL2ioV	CLKOUT↓ to Port out valid ^(1,2)	—		40**	ns				
15	TioV2ckH	Port in valid before CLKOUT ^(1,2)	0.25 TCY+30*	—	—	ns				
16	TckH2iol	Port in hold after CLKOUT ^(1,2)	0*	—	—	ns				
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽²⁾	—	—	100	ns				
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns				
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns				
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns				
21	TioF	Port output fall time ⁽²⁾		10	25**	ns				

* These parameters are characterized but not tested.

- ** These parameters are design targets and are not tested. No characterization data available at this time.
- † Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Refer to Figure 19-2 for load conditions.

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21.0 PACKAGING INFORMATION

21.1 Package Marketing Information

18-Lead PDIP



28-Lead Skinny PDIP (.300")



28-Lead PDIP (.600")



18-Lead SOIC



28-Lead SOIC



20-Lead SSOP



28-Lead SSOP





Example



Example



Example



Example



Example



Example



28-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging







		INCHES*		MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.050			1.27	
Overall Height	А	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	Е	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59
Overall Length	D	.695	.704	.712	17.65	17.87	18.08
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle Top	¢	0	4	8	0	4	8
Lead Thickness	С	.009	.011	.013	0.23	0.28	0.33
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013 Drawing No. C04-052

APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

- 1. Check any CALL, GOTO or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
- 2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change RESET vector to proper value for processor used.
- 6. Remove any use of the ADDLW, RETURN and SUBLW instructions.
- 7. Rewrite any code segments that use interrupts.

APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.

w

W Register	
Value on reset	20
Wake-up from SLEEP	19, 47
Watchdog Timer (WDT)	43, 46
Period	
Programming Considerations	
Register values on reset	
WWW, On-Line Support	3
X	
XORLW	60
XORWF	60
Z	
Zero (Z) bit	9, 29

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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