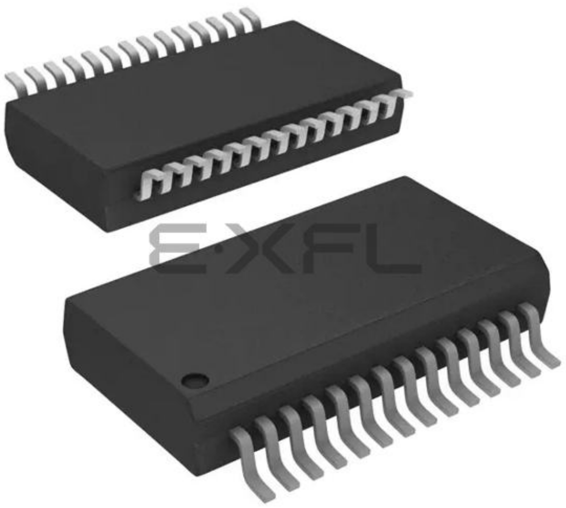

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 20 |
| Program Memory Size | 3KB (2K x 12) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 72 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16c57c-04i-ss |

# PIC16C5X

## 8-Bit EPROM/ROM-Based CMOS Microcontrollers

### 1.0 GENERAL DESCRIPTION

The PIC16C5X from Microchip Technology is a family of low cost, high performance, 8-bit fully static, EPROM/ROM-based CMOS microcontrollers. It employs a RISC architecture with only 33 single word/ single cycle instructions. All instructions are single cycle except for program branches which take two cycles. The PIC16C5X delivers performance in an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C5X products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external RESET circuitry. There are four oscillator configurations to choose from, including the power saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and Code Protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers, while benefiting from the OTP's flexibility.

The PIC16C5X products are supported by a full featured macro assembler, a software simulator, an in-circuit emulator, a low cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

### 1.1 Applications

The PIC16C5X series fits perfectly in applications ranging from high speed automotive and appliance motor control to low power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customizing application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low cost, low power, high performance ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, co-processor applications).

## 7.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., `MOVF PORTB,W`) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

### 7.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used (RA<3:0>). Bits 7-4 are unimplemented and read as '0's.

### 7.2 PORTB

PORTB is an 8-bit I/O Register (PORTB<7:0>).

### 7.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58 and PIC16CR58.

### 7.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the `TRIS f` instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

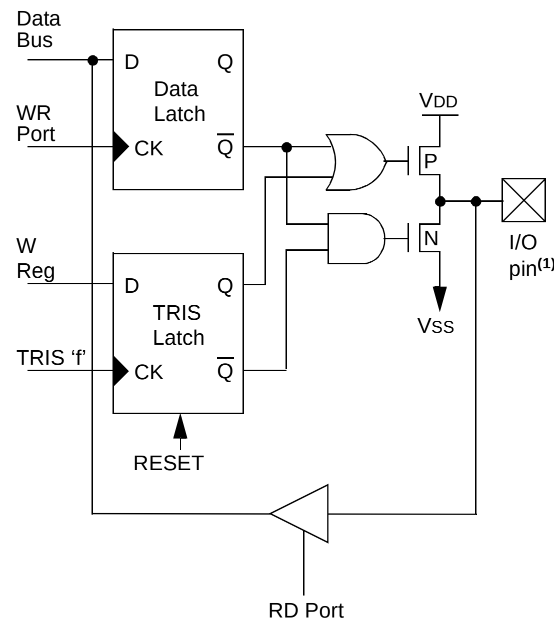
| | |
|---|---|
| **Note:** | A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low. |

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

### 7.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 7-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF PORTB, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

**FIGURE 7-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN**




**Note 1:** I/O pins have protection diodes to $V_{DD}$ and $V_{SS}$.

**TABLE 7-1: SUMMARY OF PORT REGISTERS**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on MCLR and WDT Reset |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N/A | TRIS | I/O Control Registers (TRISA, TRISB, TRISC) | | | | | | | | 1111 1111 | 1111 1111 |
| 05h | PORTA | — | — | — | — | RA3 | RA2 | RA1 | RA0 | ---- xxxx | ---- uuuu |
| 06h | PORTB | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx xxxx | uuuu uuuu |
| 07h | PORTC | RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | xxxx xxxx | uuuu uuuu |

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'

## 9.3 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

### 9.3.1 SLEEP

The Power-down mode is entered by executing a `SLEEP` instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the `SLEEP` instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{MCLR}/V_{PP}$ pin low.

For lowest current consumption while powered down, the T0CKI input should be at $V_{DD}$ or $V_{SS}$ and the $\overline{MCLR}/V_{PP}$ pin must be at a logic high level ($\overline{MCLR} = V_{IH}$).

### 9.3.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. An external RESET input on $\overline{MCLR}/V_{PP}$ pin.
2. A Watchdog Timer Time-out Reset (if WDT was enabled).

Both of these events cause a device RESET. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the cause of device RESET. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when `SLEEP` is invoked.

The WDT is cleared when the device wakes from SLEEP, regardless of the wake-up source.

## 9.4 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

| Note: | Microchip does not recommend code protecting windowed devices. |
|---|---|

## 9.5 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

| Note: | Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code. |
|---|---|

### SUBWF — Subtract W from f

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – (W) → (dest)

Status Affected: C, DC, Z

Encoding:

| | | |
|---|---|---|
| `0000` | `10df` | `ffff` |

Description: Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1: `SUBWF REG1, 1`

Before Instruction
REG1 = 3
W = 2
C = ?
After Instruction
REG1 = 1
W = 2
C = 1 ; result is positive

Example 2:

Before Instruction
REG1 = 2
W = 2
C = ?
After Instruction
REG1 = 0
W = 2
C = 1 ; result is zero

Example 3:

Before Instruction
REG1 = 1
W = 2
C = ?
After Instruction
REG1 = 0xFF
W = 2
C = 0 ; result is negative

### SWAPF — Swap Nibbles in f

Syntax: [ *label* ] SWAPF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f<3:0>) → (dest<7:4>);
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

| | | |
|---|---|---|
| `0011` | `10df` | `ffff` |

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example `SWAPF REG1, 0`

Before Instruction
REG1 = 0xA5
After Instruction
REG1 = 0xA5
W = 0x5A

### TRIS — Load TRIS Register

Syntax: [ *label* ] TRIS f

Operands: f = 5, 6 or 7

Operation: (W) → TRIS register f

Status Affected: None

Encoding:

| | | |
|---|---|---|
| `0000` | `0000` | `0fff` |

Description: TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register.

Words: 1

Cycles: 1

Example `TRIS PORTB`

Before Instruction
W = 0xA5
After Instruction
TRISB = 0xA5

**TABLE 11-1: DEVELOPMENT TOOLS FROM MICROCHIP**

| | | PIC12CXXX | PIC14000 | PIC16C5X | PIC16C6X | PIC16CXXX | PIC16F62X | PIC16C7X | PIC16C7XX | PIC16C8X | PIC16F8XX | PIC16C9XX | PIC17C4X | PIC17C7XX | PIC18CXX2 | PIC18FXXX | 24CXX/ 25CXX/ 93CXX | HCSXXX | MCRFXXX | MCP2510 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Software Tools | MPLAB® Integrated Development Environment | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | MPLAB® C17 C Compiler | | | | | | | | | | | | ✓ | ✓ | | | | | | |
| | MPLAB® C18 C Compiler | | | | | | | | | | | | | | ✓ | ✓ | | | | |
| | MPASM™ Assembler/ MPLINK™ Object Linker | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| Emulators | MPLAB® ICE In-Circuit Emulator | ✓ | ✓ | ✓ | ✓ | ✓ | ✓** | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | ICEPIC™ In-Circuit Emulator | ✓ | | ✓ | ✓ | ✓ | | ✓ | ✓ | ✓ | | ✓ | | | | | | | | |
| Debugger | MPLAB® ICD In-Circuit Debugger | | | | ✓* | | | ✓* | | | ✓ | | | | | ✓ | | | | |
| Programmers | PICSTART® Plus Entry Level Development Programmer | ✓ | ✓ | ✓ | ✓ | ✓ | ✓** | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | PRO MATE® II Universal Device Programmer | ✓ | ✓ | ✓ | ✓ | ✓ | ✓** | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| Demo Boards and Eval Kits | PICDEM™ 1 Demonstration Board | | | ✓ | | ✓ | | ✓† | | ✓ | | | ✓ | | | | | | | |
| | PICDEM™ 2 Demonstration Board | | | | ✓† | | | ✓† | | | | | | | ✓ | ✓ | | | | |
| | PICDEM™ 3 Demonstration Board | | | | | | | | | | | ✓ | | | | | | | | |
| | PICDEM™ 14A Demonstration Board | | ✓ | | | | | | | | | | | | | | | | | |
| | PICDEM™ 17 Demonstration Board | | | | | | | | | | | | | ✓ | | | | | | |
| | KEELOQ® Evaluation Kit | | | | | | | | | | | | | | | | | ✓ | | |
| | KEELOQ® Transponder Kit | | | | | | | | | | | | | | | | | ✓ | | |
| | microID™ Programmer's Kit | | | | | | | | | | | | | | | | | | ✓ | |
| | 125 kHz microID™ Developer's Kit | | | | | | | | | | | | | | | | | | ✓ | |
| | 125 kHz Anticollision microID™ Developer's Kit | | | | | | | | | | | | | | | | | | ✓ | |
| | 13.56 MHz Anticollision microID™ Developer's Kit | | | | | | | | | | | | | | | | | | ✓ | |
| | MCP2510 CAN Developer's Kit | | | | | | | | | | | | | | | | | | | ✓ |

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB® ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77.

** Contact Microchip Technology Inc. for availability date.

† Development tool is available on select devices.

**TABLE 13-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 1 | TOSC | External CLKIN Period(1) | 250 | — | — | ns | XT OSC mode |
| | | | 250 | — | — | ns | HS OSC mode (04) |
| | | | 100 | — | — | ns | HS OSC mode (10) |
| | | | 50 | — | — | ns | HS OSC mode (20) |
| | | | 5.0 | — | — | μs | LP OSC mode |
| | | Oscillator Period(1) | 250 | — | — | ns | RC OSC mode |
| | | | 250 | — | 10,000 | ns | XT OSC mode |
| | | | 250 | — | 250 | ns | HS OSC mode (04) |
| | | | 100 | — | 250 | ns | HS OSC mode (10) |
| | | | 50 | — | 250 | ns | HS OSC mode (20) |
| | | | 5.0 | — | 200 | μs | LP OSC mode |
| 2 | TCY | Instruction Cycle Time(2) | — | 4/FOSC | — | — | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 50* | — | — | ns | XT oscillator |
| | | | 20* | — | — | ns | HS oscillator |
| | | | 2.0* | — | — | μs | LP oscillator |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 25* | ns | XT oscillator |
| | | | — | — | 25* | ns | HS oscillator |
| | | | — | — | 50* | ns | LP oscillator |

* These parameters are characterized but not tested.

† Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

**FIGURE 14-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED**

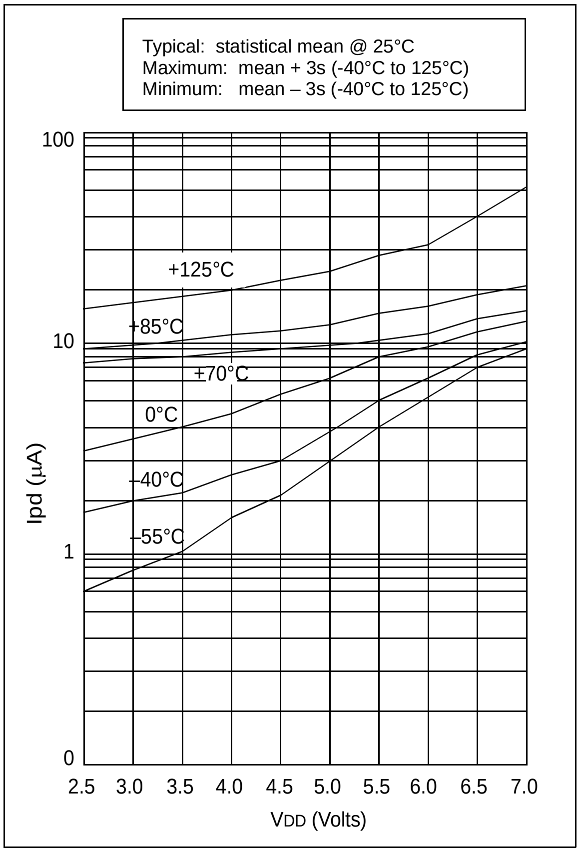



**FIGURE 14-7: TYPICAL IPD vs. VDD, WATCHDOG ENABLED**

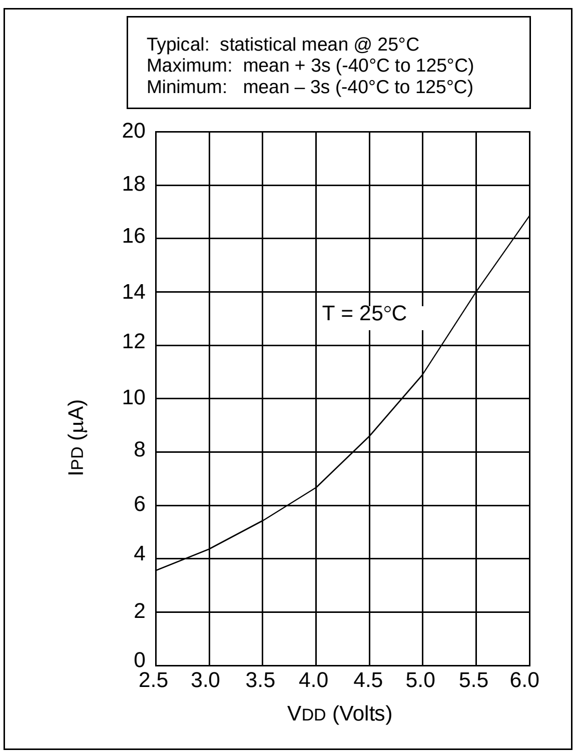
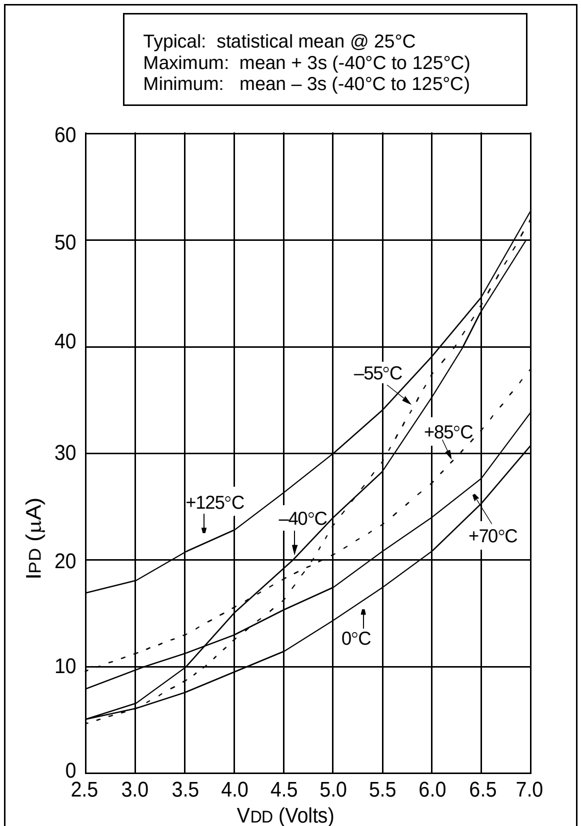



**FIGURE 14-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED**




IPD, with WDT enabled, has two components:
The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At –40°C, the latter dominates explaining the apparently anomalous behavior.

**FIGURE 14-19: PORTA, B AND C IOH vs. VOH, VDD = 3 V**

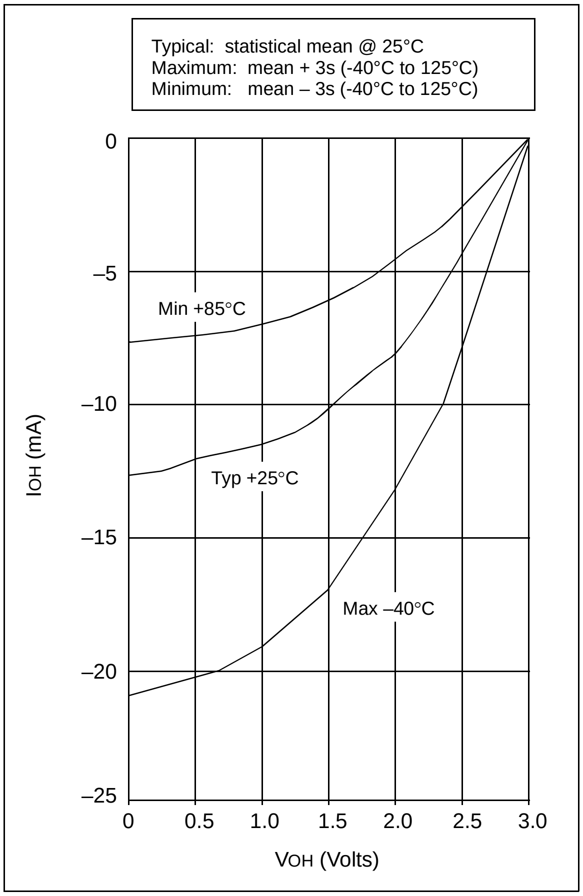
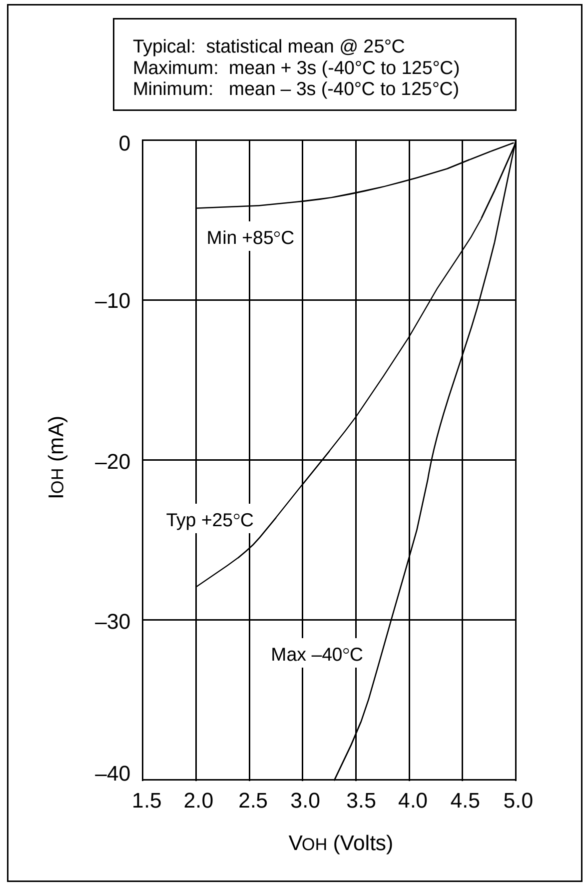



**FIGURE 14-20: PORTA, B AND C IOH vs. VOH, VDD = 5 V**




 Preliminary 

### TABLE 14-2: INPUT CAPACITANCE FOR PIC16C54/56

| Pin | Typical Capacitance (pF) | |
|---|---|---|
| | 18L PDIP | 18L SOIC |
| RA port | 5.0 | 4.3 |
| RB port | 5.0 | 4.3 |
| $\overline{\text{MCLR}}$ | 17.0 | 17.0 |
| OSC1 | 4.0 | 3.5 |
| OSC2/CLKOUT | 4.3 | 3.5 |
| T0CKI | 3.2 | 2.8 |

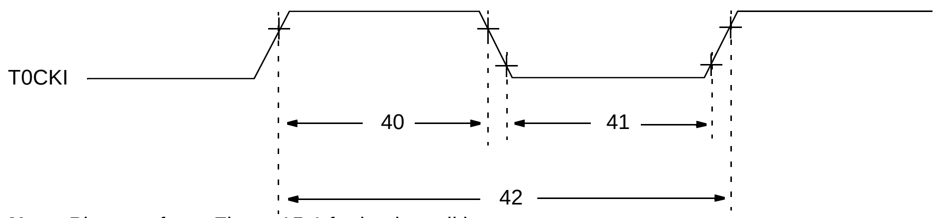
All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

### TABLE 14-3: INPUT CAPACITANCE FOR PIC16C55/57

| Pin | Typical Capacitance (pF) | |
|---|---|---|
| | 28L PDIP (600 mil) | 28L SOIC |
| RA port | 5.2 | 4.8 |
| RB port | 5.6 | 4.7 |
| RC port | 5.0 | 4.1 |
| $\overline{\text{MCLR}}$ | 17.0 | 17.0 |
| OSC1 | 6.6 | 3.5 |
| OSC2/CLKOUT | 4.6 | 3.5 |
| T0CKI | 4.5 | 3.5 |

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

**FIGURE 15-5: TIMER0 CLOCK TIMINGS - PIC16C54A**




**Note:** Please refer to Figure 15-1 for load conditions.

**TABLE 15-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54A**

| AC Characteristics | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I<br>–40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 40 | Tt0H | T0CKI High Pulse Width | | | | | |
| | | - No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width | | | | | |
| | | - No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | 20 or (TCY + 40)/N* | — | — | ns | Whichever is greater.<br>N = Prescale Value (1, 2, 4,..., 256) |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 16-14: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, 25°C)**

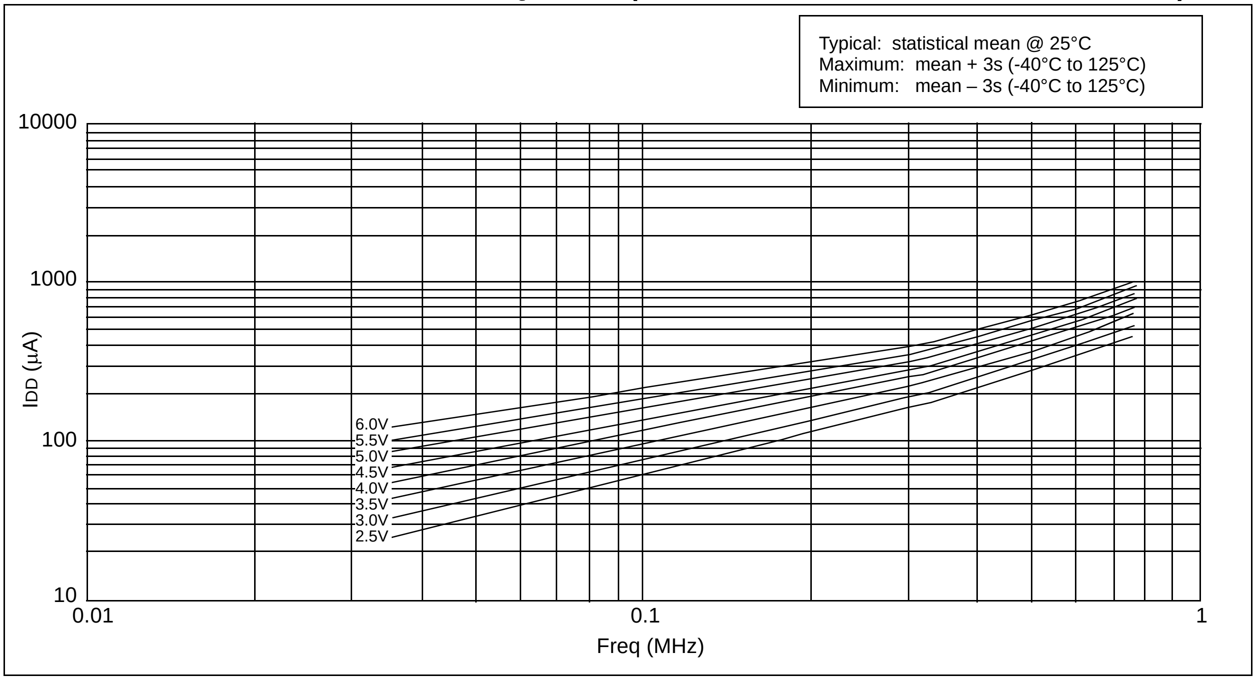
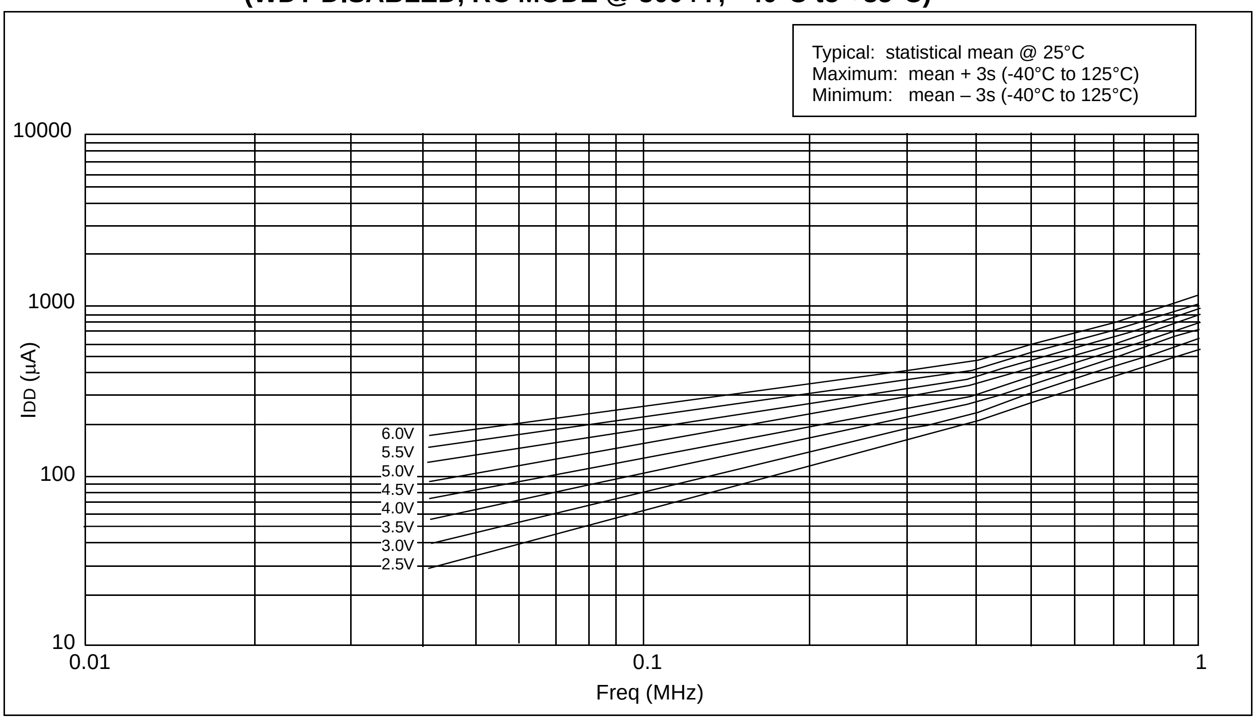



**FIGURE 16-15: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, –40°C to +85°C)**



## 17.0 ELECTRICAL CHARACTERISTICS - PIC16LC54A

**Absolute Maximum Ratings(†)**

Ambient temperature under bias .......... –55°C to +125°C
Storage temperature .......... –65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ .......... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ .......... 0 to +14V
Voltage on all other pins with respect to $V_{SS}$ .......... –0.6V to ($V_{DD}$ + 0.6V)
Total power dissipation[(1)] .......... 800 mW
Max. current out of $V_{SS}$ pin .......... 150 mA
Max. current into $V_{DD}$ pin .......... 100 mA
Max. current into an input pin (T0CKI only) .......... ±500 μA
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) .......... ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) .......... ±20 mA
Max. output current sunk by any I/O pin .......... 25 mA
Max. output current sourced by any I/O pin .......... 20 mA
Max. output current sourced by a single I/O (Port A, B or C) .......... 50 mA
Max. output current sunk by a single I/O (Port A, B or C) .......... 50 mA

**Note 1:** Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 17.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

| | |
|---|---|
| **PIC16LC5X**<br>**PIC16LCR5X**<br>(Commercial, Industrial) | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial |
| **PIC16C5X**<br>**PIC16CR5X**<br>(Commercial, Industrial) | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial |

| Param No. | Symbol | Characteristic/Device | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | IDD | **Supply Current(2,3)** | | | | | |
| D010 | | PIC16LC5X | —<br>—<br><br>— | 0.5<br>11<br><br>14 | 2.4<br>27<br><br>35 | mA<br>μA<br><br>μA | FOSC = 4.0 MHz, VDD = 5.5V, XT and RC modes<br>FOSC = 32 kHz, VDD = 2.5V, LP mode, Commercial<br>FOSC = 32 kHz, VDD = 2.5V, LP mode, Industrial |
| D010A | | PIC16C5X | —<br>—<br>—<br>—<br><br>— | 1.8<br>2.6<br>4.5<br>14<br><br>17 | 2.4<br>3.6*<br>16<br>32<br><br>40 | mA<br>mA<br>mA<br>μA<br><br>μA | FOSC = 4 MHz, VDD = 5.5V, XT and RC modes<br>FOSC = 10 MHz, VDD = 3.0V, HS mode<br>FOSC = 20 MHz, VDD = 5.5V, HS mode<br>FOSC = 32 kHz, VDD = 3.0V, LP mode, Commercial<br>FOSC = 32 kHz, VDD = 3.0V, LP mode, Industrial |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

## 17.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended) PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

| **PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E**<br>**PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E**<br>(Extended) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | <br>3.0<br>4.5 | <br>—<br>— | <br>5.5<br>5.5 | <br>V<br>V | RC, XT, LP, and HS mode<br>from 0 - 10 MHz<br>from 10 - 20 MHz |
| D002 | VDR | **RAM Data Retention Voltage**(1) | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD start voltage** to ensure Power-on Reset | — | Vss | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD rise rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D010 | IDD | **Supply Current**(2)<br>XT and RC(3) modes<br>HS mode | <br>—<br>— | <br>1.8<br>9.0 | <br>3.3<br>20 | <br>mA<br>mA | <br>FOSC = 4.0 MHz, VDD = 5.5V<br>FOSC = 20 MHz, VDD = 5.5V |
| D020 | IPD | **Power-down Current**(2) | —<br>—<br>—<br>—<br>—<br>— | 0.3<br>10<br>12<br>4.8<br>18<br>26 | 17<br>50*<br>60*<br>31*<br>68*<br>90* | μA<br>μA<br>μA<br>μA<br>μA<br>μA | VDD = 3.0V, WDT disabled<br>VDD = 4.5V, WDT disabled<br>VDD = 5.5V, WDT disabled<br>VDD = 3.0V, WDT enabled<br>VDD = 4.5V, WDT enabled<br>VDD = 5.5V, WDT enabled |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

## 18.0 DEVICE CHARACTERIZATION - PIC16LC54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean – 3σ) respectively, where σ is a standard deviation, over the whole temperature range.

**FIGURE 18-1: TYPICAL RC OSCILLATOR FREQUENCY VS. TEMPERATURE**

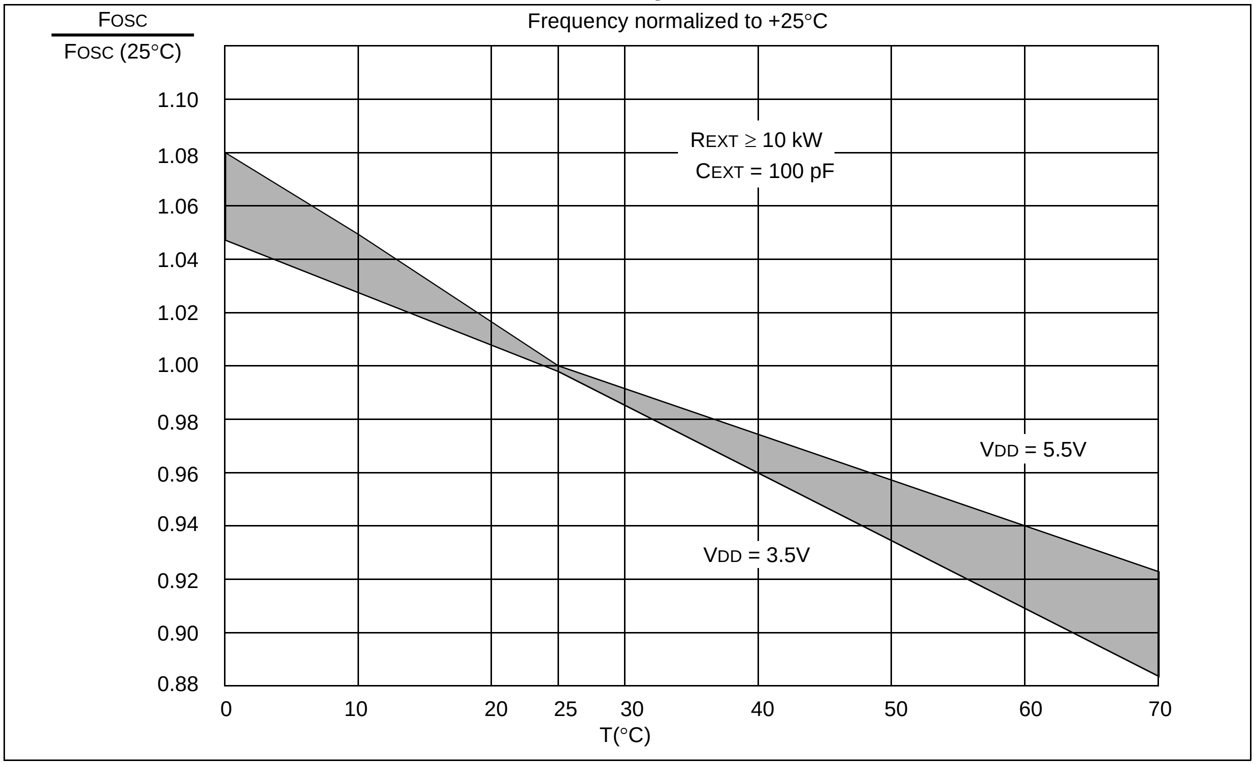


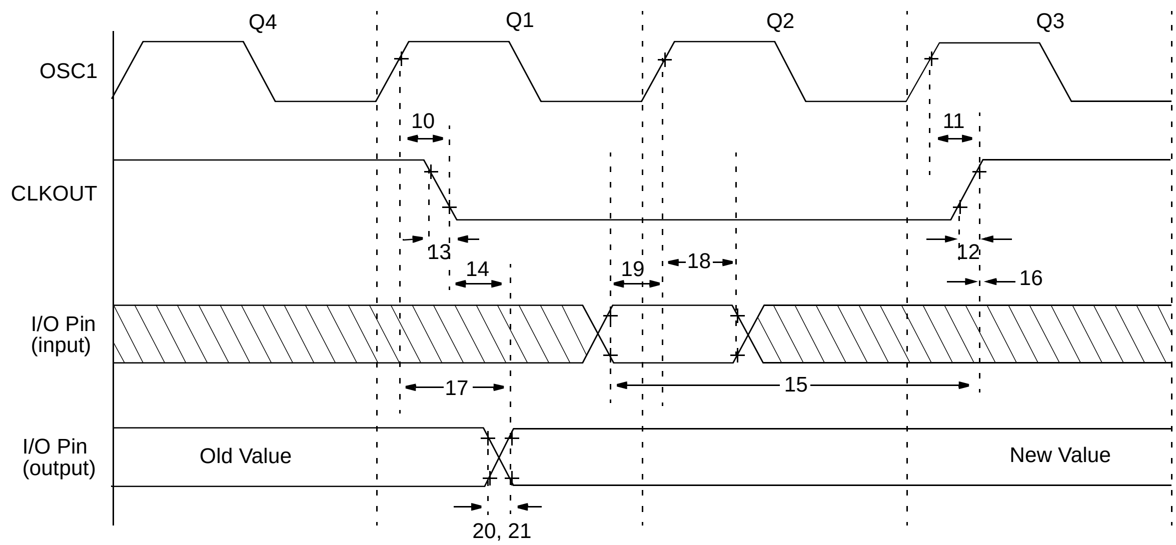

**TABLE 18-1: RC OSCILLATOR FREQUENCIES**

| CEXT | REXT | Average Fosc @ 5V, 25°C | |
|---|---|---|---|
| 20 pF | 3.3K | 5 MHz | ± 27% |
| | 5K | 3.8 MHz | ± 21% |
| | 10K | 2.2 MHz | ± 21% |
| | 100K | 262 kHz | ± 31% |
| 100 pF | 3.3K | 1.63 MHz | ± 13% |
| | 5K | 1.2 MHz | ± 13% |
| | 10K | 684 kHz | ± 18% |
| | 100K | 71 kHz | ± 25% |
| 300 pF | 3.3K | 660 kHz | ± 10% |
| | 5.0K | 484 kHz | ± 14% |
| | 10K | 267 kHz | ± 15% |
| | 100K | 29 kHz | ± 19% |

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5V.

**FIGURE 19-4: CLKOUT AND I/O TIMING - PIC16C5X-40**




**Note:** Refer to Figure 19-2 for load conditions.

**TABLE 19-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X-40**

| AC Characteristics | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** |
| 10 | TosH2ckL | OSC1↑ to CLKOUT↓(1,2) | — | 15 | 30** | ns |
| 11 | TosH2ckH | OSC1↑ to CLKOUT↑(1,2) | — | 15 | 30** | ns |
| 12 | TckR | CLKOUT rise time(1,2) | — | 5.0 | 15** | ns |
| 13 | TckF | CLKOUT fall time(1,2) | — | 5.0 | 15** | ns |
| 14 | TckL2ioV | CLKOUT↓ to Port out valid(1,2) | — | — | 40** | ns |
| 15 | TioV2ckH | Port in valid before CLKOUT↑(1,2) | 0.25 TCY+30* | — | — | ns |
| 16 | TckH2ioI | Port in hold after CLKOUT↑(1,2) | 0* | — | — | ns |
| 17 | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid(2) | — | — | 100 | ns |
| 18 | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | TBD | — | — | ns |
| 19 | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | TBD | — | — | ns |
| 20 | TioR | Port output rise time(2) | — | 10 | 25** | ns |
| 21 | TioF | Port output fall time(2) | — | 10 | 25** | ns |

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

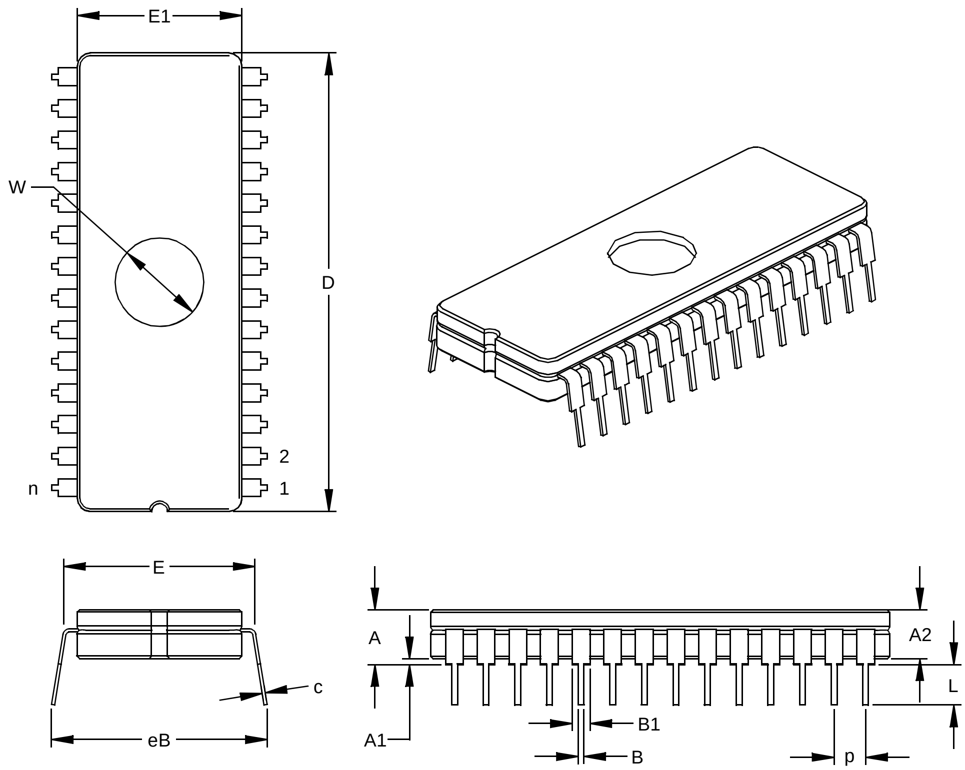
† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

**2:** Refer to Figure 19-2 for load conditions.

## 28-Lead Ceramic Dual In-line with Window (JW) – 600 mil (CERDIP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| | Units | INCHES* | | | MILLIMETERS | | |
| | Dimension Limits | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .195 | .210 | .225 | 4.95 | 5.33 | 5.72 |
| Ceramic Package Height | A2 | .155 | .160 | .165 | 3.94 | 4.06 | 4.19 |
| Standoff | A1 | .015 | .038 | .060 | 0.38 | 0.95 | 1.52 |
| Shoulder to Shoulder Width | E | .595 | .600 | .625 | 15.11 | 15.24 | 15.88 |
| Ceramic Pkg. Width | E1 | .514 | .520 | .526 | 13.06 | 13.21 | 13.36 |
| Overall Length | D | 1.430 | 1.460 | 1.490 | 36.32 | 37.08 | 37.85 |
| Tip to Seating Plane | L | .125 | .138 | .150 | 3.18 | 3.49 | 3.81 |
| Lead Thickness | c | .008 | .010 | .012 | 0.20 | 0.25 | 0.30 |
| Upper Lead Width | B1 | .050 | .058 | .065 | 1.27 | 1.46 | 1.65 |
| Lower Lead Width | B | .016 | .020 | .023 | 0.41 | 0.51 | 0.58 |
| Overall Row Spacing § | eB | .610 | .660 | .710 | 15.49 | 16.76 | 18.03 |
| Window Diameter | W | .270 | .280 | .290 | 6.86 | 7.11 | 7.37 |

* Controlling Parameter
§ Significant Characteristic
JEDEC Equivalent: MO-103
Drawing No. C04-013

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