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#### Details

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57c-20e-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## **Pin Diagrams**



## **Device Differences**

Device	Voltage Range	Oscillator Selection (Program)	Oscillator	Process Technology (Microns)	ROM Equivalent	MCLR Filter
PIC16C54	2.5-6.25	Factory	See Note 1	1.2	PIC16CR54A	No
PIC16C54A	2.0-6.25	User	See Note 1	0.9	—	No
PIC16C54C	2.5-5.5	User	See Note 1	0.7	PIC16CR54C	Yes
PIC16C55	2.5-6.25	Factory	See Note 1	1.7	_	No
PIC16C55A	2.5-5.5	User	See Note 1	0.7	—	Yes
PIC16C56	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C56A	2.5-5.5	User	See Note 1	0.7	PIC16CR56A	Yes
PIC16C57	2.5-6.25	Factory	See Note 1	1.2	—	No
PIC16C57C	2.5-5.5	User	See Note 1	0.7	PIC16CR57C	Yes
PIC16C58B	2.5-5.5	User	See Note 1	0.7	PIC16CR58B	Yes
PIC16CR54A	2.5-6.25	Factory	See Note 1	1.2	N/A	Yes
PIC16CR54C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR56A	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR57C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR58B	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

**Note:** The table shown above shows the generic names of the PIC16C5X devices. For device varieties, please refer to Section 2.0.

# 5.0 RESET

PIC16C5X devices may be RESET in one of the following ways:

- Power-On Reset (POR)
- MCLR Reset (normal operation)
- MCLR Wake-up Reset (from SLEEP)
- WDT Reset (normal operation)
- WDT Wake-up Reset (from SLEEP)

Table 5-1 shows these RESET conditions for the PCL and STATUS registers.

Some registers are not affected in any RESET condition. Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-On Reset (POR), MCLR or WDT Reset. A MCLR or WDT wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP. The  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits (STATUS <4:3>) are set or cleared depending on the different RESET conditions (Table 5-1). These bits may be used to determine the nature of the RESET.

Table 5-3 lists a full description of RESET states of all registers. Figure 5-1 shows a simplified block diagram of the On-chip Reset circuit.

## TABLE 5-1: STATUS BITS AND THEIR SIGNIFICANCE

Condition	то	PD
Power-On Reset	1	1
MCLR Reset (normal operation)	u	u
MCLR Wake-up (from SLEEP)	1	0
WDT Reset (normal operation)	0	1
WDT Wake-up (from SLEEP)	0	0

Legend: u = unchanged, x = unknown, - = unimplemented read as '0'.

#### TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH RESET

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	<u>Value</u> on MCLR and WDT Reset
03h	STATUS	PA2	PA1	PA0	TO	PD	Z	DC	С	0001 1xxx	000q quuu

Legend: u = unchanged, x = unknown, q = see Table 5-1 for possible values.

# 6.0 MEMORY ORGANIZATION

PIC16C5X memory is organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one or two STATUS Register bits. For devices with a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Selection Register (FSR).

# 6.1 Program Memory Organization

The PIC16C54, PIC16CR54 and PIC16C55 have a 9bit Program Counter (PC) capable of addressing a 512 x 12 program memory space (Figure 6-1). The PIC16C56 and PIC16CR56 have a 10-bit Program Counter (PC) capable of addressing a 1K x 12 program memory space (Figure 6-2). The PIC16CR57, PIC16C58 and PIC16CR58 have an 11-bit Program Counter capable of addressing a 2K x 12 program memory space (Figure 6-3). Accessing a location above the physically implemented address will cause a wraparound.

A NOP at the RESET vector location will cause a restart at location 000h. The RESET vector for the PIC16C54, PIC16CR54 and PIC16C55 is at 1FFh. The RESET vector for the PIC16C56 and PIC16CR56 is at 3FFh. The RESET vector for the PIC16C57, PIC16CR57, PIC16C58, and PIC16CR58 is at 7FFh. See Section 6.5 for additional information using CALL and GOTO instructions.

#### FIGURE 6-1: PIC16C54/CR54/C55 PROGRAM MEMORY MAP AND STACK



#### FIGURE 6-2:

#### PIC16C56/CR56 PROGRAM MEMORY MAP AND STACK



FIGURE 6-3:

PIC16C57/CR57/C58/ CR58 PROGRAM MEMORY MAP AND STACK



# 6.7 Indirect Data Addressing; INDF and FSR Registers

The INDF Register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR Register (FSR is a *pointer*). This is indirect addressing.

#### EXAMPLE 6-1: INDIRECT ADDRESSING

- Register file 08 contains the value 10h
- Register file 09 contains the value 0Ah
- Load the value 08 into the FSR Register
- A read of the INDF Register will return the value of 10h
- Increment the value of the FSR Register by one (FSR = 09h)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF Register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 6-2.

## EXAMPLE 6-2:

#### HOW TO CLEAR RAM USING INDIRECT ADDRESSING

	MOVLW	H'10'	;initialize pointer
	MOVWF	FSR	; to RAM
NEXT	CLRF	INDF	;clear INDF Register
	INCF	FSR,F	;inc pointer
	BTFSC	FSR,4	;all done?
	GOTO	NEXT	;NO, clear next
CONTINUE			
	:		;YES, continue

The FSR is either a 5-bit (PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56) or 7-bit (PIC16C57, PIC16CR57, PIC16CR58, PIC16CR58) wide register. It is used in conjunction with the INDF Register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

**PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56:** These do not use banking. FSR<6:5> bits are unimplemented and read as '1's.

**PIC16C57**, **PIC16CR57**, **PIC16C58**, **PIC16CR58**: FSR<6:5> are the bank select bits and are used to select the bank to be addressed (00 = bank 0, 01 = bank 1, 10 = bank 2, 11 = bank 3).



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# 8.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Readable and writable
- 8-bit software programmable prescaler
- · Internal or external clock select
- Edge select for external clock

Figure 8-1 is a simplified block diagram of the Timer0 module, while Figure 8-2 shows the electrical structure of the Timer0 input.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 8-3 and Figure 8-4). The user can work around this by writing an adjusted value to the TMR0 register.



Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 8.1.

Note: The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both.

The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 8.2 details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 8-1.



#### FIGURE 8-2: ELECTRICAL STRUCTURE OF TOCKI PIN



Mnemonic,		Description	Cualas	12-1	Bit Opc	ode	Status	Natas
Opera	nds	Description	Cycles	MSb		LSb	Affected	Notes
ADDWF	f,d	Add W and f	1	0001	11df	ffff	C,DC,Z	1,2,4
ANDWF	f,d	AND W with f	1	0001	01df	ffff	Z	2,4
CLRF	f	Clear f	1	0000	011f	ffff	Z	4
CLRW	_	Clear W	1	0000	0100	0000	Z	
COMF	f, d	Complement f	1	0010	01df	ffff	Z	
DECF	f, d	Decrement f	1	0000	11df	ffff	Z	2,4
DECFSZ	f, d	Decrement f, Skip if 0	1 <sup>(2)</sup>	0010	11df	ffff	None	2,4
INCF	f, d	Increment f	1	0010	10df	ffff	Z	2,4
INCFSZ	f, d	Increment f, Skip if 0	1 <sup>(2)</sup>	0011	11df	ffff	None	2,4
IORWF	f, d	Inclusive OR W with f	1	0001	00df	ffff	Z	2,4
MOVF	f, d	Move f	1	0010	00df	ffff	Z	2,4
MOVWF	f	Move W to f	1	0000	001f	ffff	None	1,4
NOP	-	No Operation	1	0000	0000	0000	None	
RLF	f, d	Rotate left f through Carry	1	0011	01df	ffff	С	2,4
RRF	f, d	Rotate right f through Carry	1	0011	00df	ffff	С	2,4
SUBWF	f, d	Subtract W from f	1	0000	10df	ffff	C,DC,Z	1,2,4
SWAPF	f, d	Swap f	1	0011	10df	ffff	None	2,4
XORWF	f, d	Exclusive OR W with f	1	0001	10df	ffff	Z	2,4
BIT-ORIEN	TED FIL	E REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	0100	bbbf	ffff	None	2,4
BSF	f, b	Bit Set f	1	0101	bbbf	ffff	None	2,4
BTFSC	f, b	Bit Test f, Skip if Clear	1 <sup>(2)</sup>	0110	bbbf	ffff	None	
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	0111	bbbf	ffff	None	
LITERAL A	ND CON	ITROL OPERATIONS		r				
ANDLW	k	AND literal with W	1	1110	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	1001	kkkk	kkkk	None	1
CLRWDT	k	Clear Watchdog Timer	1	0000	0000	0100	TO, PD	
GOTO	k	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW	k	Inclusive OR Literal with W	1	1101	kkkk	kkkk	Z	
MOVLW	k	Move Literal to W	1	1100	kkkk	kkkk	None	
OPTION	k	Load OPTION register	1	0000	0000	0010	None	
RETLW	k	Return, place Literal in W	2	1000	kkkk	kkkk	None	
SLEEP	-	Go into standby mode	1	0000	0000	0011	TO, PD	
TRIS	f	Load TRIS register	1	0000	0000	Offf	None	3
XORLW	k	Exclusive OR Literal to W	1	1111	kkkk	kkkk	Z	

#### TABLE 10-2: INSTRUCTION SET SUMMARY

**Note 1:** The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO (see Section 6.5 for more on program counter).

2: When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

**3:** The instruction TRIS f, where f = 5, 6 or 7 causes the contents of the W register to be written to the tristate latches of PORTA, B or C respectively. A '1' forces the pin to a hi-impedance state and disables the output buffers.

**4:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

## 12.2 DC Characteristics: PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)				Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial					
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions		
D001	Vdd	Supply Voltage PIC16C5X-RCI PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-HSI	3.0 3.0 4.5 4.5		6.25 6.25 5.5 5.5 6.25	V V V V			
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	2.5	1.5*		V	Device in SLEEP mode		
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset		
D010	IDD	Supply Current <sup>(2)</sup> PIC16C5X-RCI <sup>(3)</sup> PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-HSI PIC16C5X-LPI		1.8 1.8 4.8 9.0 15	3.3 3.3 10 10 20 40	mA mA mA mA μA	Fosc = 4 MHz, VDD = $5.5V$ Fosc = 4 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 20 MHz, VDD = $5.5V$ Fosc = $32$ kHz, VDD = $3.0V$ , WDT disabled		
D020	IPD	Power-down Current <sup>(2)</sup>	_	4.0 0.6	14 12	μΑ μΑ	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled		

\* These parameters are characterized but not tested.

- † Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
  - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
    - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
    - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
  - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.



#### FIGURE 12-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING -PIC16C54/55/56/57

#### TABLE 12-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57

AC Chara	cteristics	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic Min			Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	100*	—	_	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low		_	100*	ns	

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## 13.2 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

PIC16CR54A-04E, 10E, 20E (Extended)				ard Oper ing Temp	ating C	condition -40°C	is (unless otherwise specified) $C \le TA \le +125^{\circ}C$ for extended
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
D001	Vdd	Supply Voltage RC, XT and LP modes HS mode	3.25 4.5		6.0 5.5	V V	
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power- on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current <sup>(2)</sup> RC <sup>(3)</sup> and XT modes HS mode HS mode		1.8 4.8 9.0	3.3 10 20	mA mA mA	Fosc = 4.0 MHz, VDD = 5.5V Fosc = 10 MHz, VDD = 5.5V Fosc = 16 MHz, VDD = 5.5V
D020	IPD	Power-down Current <sup>(2)</sup>		5.0 0.8	22 18	μΑ μΑ	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

- 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
  - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
  - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

# 13.5 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS

2. Tp	pS	
Т		
F	Frequency	T Time
Lowe	ercase letters (pp) and their meanings:	
рр		
2	to	mc MCLR
ck	CLKOUT	osc oscillator
су	cycle time	os OSC1
drt	device reset timer	t0 T0CKI
io	I/O port	wdt watchdog timer
Uppe	ercase letters and their meanings:	
S		
F	Fall	P Period
Н	High	R Rise
Ι	Invalid (Hi-impedance)	V Valid
L	Low	Z Hi-impedance

# FIGURE 13-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16CR54A



# 14.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean +  $3\sigma$ ) or (mean -  $3\sigma$ ) respectively, where  $\sigma$  is a standard deviation, over the whole temperature range.





## TABLE 14-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Ave Fosc @	rage 5 V, 25°C
20 pF	3.3K	5 MHz	± 27%
	5K	3.8 MHz	± 21%
	10K	2.2 MHz	± 21%
	100K	262 kHz	± 31%
100 pF	3.3K	1.6 MHz	± 13%
	5K	1.2 MHz	± 13%
	10K	684 kHz	± 18%
	100K	71 kHz	± 25%
300 pF	3.3K	660 kHz	± 10%
	5.0K	484 kHz	± 14%
	10K	267 kHz	± 15%
	100K	29 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is  $\pm 3$  standard deviations from the average value for VDD = 5V.

#### FIGURE 14-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD







# 15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04 PIC16LC54A-04I (Commercial, Industrial)				ard Ope ting Terr	perating	<b>j Cond</b> i ure 	itions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $40^{\circ}C \le TA \le +85^{\circ}C$ for industrial
PIC16C54A-04, 10, 20 PIC16C54A-04I, 10I, 20I (Commercial, Industrial)			<b>Stand</b> Opera	ard Ope ting Terr	erating operatu	<b>j Cond</b> i ure 	itions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $40^{\circ}C \le TA \le +85^{\circ}C$ for industrial
Param No. Symbol Characteristic/Device				Тур†	Max	Units	Conditions
	Vdd	Supply Voltage					
D001		PIC16LC54A	3.0 2.5	_	6.25 6.25	V V	XT and RC modes LP mode
D001A		PIC16C54A	3.0 4.5	_	6.25 5.5	V V	RC, XT and LP modes HS mode
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	-	V/ms	See Section 5.1 for details on Power-on Reset
	IDD	Supply Current <sup>(2)</sup>					
D005		PIC16LC5X	_	0.5	2.5	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC <sup>(3)</sup> and XT modes
				11	27	μΑ	Fosc = 32 kHz, VDD = 2.5V, WDT disabled, LP mode, Commercial
			_	11	35	μΑ	Fosc = 32 kHz, VDD = 2.5V, WDT disabled, LP mode, Industrial
D005A		PIC16C5X	—	1.8	2.4	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC <sup>(3)</sup> and XT modes
			—	2.4	8.0	mA	FOSC = 10 MHz, VDD = 5.5V, HS mode
			—	4.5	16	mA	FOSC = 20  MHz,  VDD = 5.5V, HS mode
				14	29	μA	HOSC = 32 kHz, VDD = 3.0V,
			-	17	37	μΑ	Fosc = 32 kHz, VDD = 3.0V, WDT disabled, LP mode, Industrial

Legend: Rows with standard voltage device data only are shaded for improved readability.

These parameters are characterized but not tested.

- † Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- **Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
  - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
    - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
    - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
  - 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k $\Omega$ .

# 15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04 PIC16LC54A-04I (Commercial, Industrial)				$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$				
PIC16C54A-04, 10, 20 PIC16C54A-04I, 10I, 20I (Commercial, Industrial)				$\begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$				
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions	
	IPD	Power-down Current <sup>(2)</sup>						
D006		PIC16LC5X	—	2.5	12	μΑ	VDD = 2.5V, WDT enabled, Commercial	
			—	0.25	4.0	μΑ	VDD = 2.5V, WDT disabled, Commercial	
			_	0.25	5.0	μΑ μΑ	VDD = 2.5V, WDT enabled, industrial $VDD = 2.5V$ , WDT disabled, Industrial	
D006A		PIC16C5X	_	4.0	12	μΑ	VDD = 3.0V, WDT enabled, Commercial	
			—	0.25	4.0	μA	VDD = 3.0V, WDT disabled, Commercial	
			—	5.0	14	μΑ	VDD = 3.0V, WDT enabled, Industrial	
				0.3	5.0	μA	$v \Box U = 3.0v, v U T uisabled, industrial$	

Legend: Rows with standard voltage device data only are shaded for improved readability.

\* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k $\Omega$ .







# PIC16C5X

# FIGURE 16-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)









#### FIGURE 16-12: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 PF, 25°C)

FIGURE 16-13: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 PF, -40°C to +85°C)











# PIC16C5X



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