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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57c-20i-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTES:

# 5.2 Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides an 18 ms nominal time-out on RESET regardless of Oscillator mode used. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows VDD to rise above VDD min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after the voltage on the MCLR/VPP pin has reached a logic high (VIH) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The Device Reset time delay will vary from chip to chip due to VDD, temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the PIC16C5X from SLEEP mode automatically.

# 5.3 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be RESET in the event of a brown-out.

To RESET PIC16C5X devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 5-6, Figure 5-7 and Figure 5-8.





# FIGURE 5-7:

# EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

# FIGURE 5-8:

# EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX families of supervisors provide push-pull and open collector outputs with both "active high and active low" RESET pins. There are 7 different trip point selections to accommodate 5V and 3V systems.

# 6.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers and General Purpose Registers.

The Special Function Registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Purpose Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

For the PIC16C54, PIC16CR54, PIC16C56 and PIC16CR56, the register file is composed of 7 Special Function Registers and 25 General Purpose Registers (Figure 6-4).

For the PIC16C55, the register file is composed of 8 Special Function Registers and 24 General Purpose Registers.

For the PIC16C57 and PIC16CR57, the register file is composed of 8 Special Function Registers, 24 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-5).

For the PIC16C58 and PIC16CR58, the register file is composed of 7 Special Function Registers, 25 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-6).

# 6.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the File Select Register (FSR). The FSR Register is described in Section 6.7.

# FIGURE 6-4:

## PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56 REGISTER FILE MAP



# 6.4 **OPTION Register**

The OPTION Register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W Register will be transferred to the OPTION Register. A RESET sets the OPTION<5:0> bits.

# **REGISTER 6-2: OPTION REGISTER**

U-0	U-0	W-1	W-1	W-1	W-1	W-1	W-1
_	—	T0CS	TOSE	PSA	PS2	PS1	PS0
bit 7							bit 0

- bit 7-6: Unimplemented: Read as '0'
- bit 5: **TOCS**: Timer0 clock source select bit
  - 1 = Transition on T0CKI pin
  - 0 = Internal instruction cycle clock (CLKOUT)
- bit 4: **TOSE**: Timer0 source edge select bit
  - 1 = Increment on high-to-low transition on T0CKI pin
  - 0 = Increment on low-to-high transition on T0CKI pin
- bit 3: **PSA**: Prescaler assignment bit
  - 1 = Prescaler assigned to the WDT
  - 0 = Prescaler assigned to Timer0

### bit 2-0: **PS<2:0>:** Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1:64	1:32
110	1 : 128	1:64
111	1 : 256	1 : 128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

# 6.5.1 PAGING CONSIDERATIONS – PIC16C56/CR56, PIC16C57/CR57 AND PIC16C58/CR58

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS Register will not be updated. Therefore, the next GOTO, CALL or modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA<1:0>).

For example, a NOP at location 1FFh (page 0) increments the PC to 200h (page 1). A GOTO xxx at 200h will return the program to address xxh on page 0 (assuming that PA<1:0> are clear).

To prevent this, the page preselect bits must be updated under program control.

# 6.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the RESET vector).

The STATUS Register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a GOTO instruction at the RESET vector location will automatically cause the program to jump to page 0.

# 6.6 Stack

PIC16C5X devices have a 10-bit or 11-bit wide, two-level hardware push/pop stack.

A CALL instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W Register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the RETLW instruction, the PC is loaded with the Top of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC, therefore, paging is not an issue when returning from a subroutine.

# 10.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 10-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers in that bank is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 10-1:	OPCODE FIELD
	DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x1F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1)
	The assembler will generate code with $x = 0$ .
	It is the recommended form of use for com-
	patibility with all Microchip software tools.
d	Destination select;
	d = 0 (store result in W)
	d = 1 (store result in file register 'f')
	Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
TO	Time-out bit
PD	Power-down bit
dest	Destination, either the W register or the
	specified register file location
[ ]	Options
( )	Contents
$\rightarrow$	Assigned to
< >	Register bit field
E	In the set of
italics	User defined term (font is courier)

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time would be 1  $\mu$ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time would be 2  $\mu$ s.

Figure 10-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

# FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations							
<u>11 6</u>	5	4 0					
OPCODE	d	f (FILE #)					
d = 0 for destination W d = 1 for destination f f = 5-bit file register address							
Bit-oriented file register	r ope	erations					
11 8	7	5 4 0					
OPCODE	b (Bl	IT #) f (FILE #)					
Literal and control ope	ratio	ns (except GOTO)					
<u>11</u>	8	7 0					
OPCODE		k (literal)					
k = 8-bit immediat	k = 8-bit immediate value						
Literal and control operations - GOTO instruction							
11	9	8 0					
OPCODE k (literal)							
k = 9-bit immediate value							

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SUBWF	Subtr	act V	V from	f	
Syntax:	[label]	S	UBWF	f,d	
Operands:	$0 \le f \le d \in [0]$	≦ 31 (,1]			
Operation:	(f) – ( <sup>v</sup>	$W) \rightarrow$	(dest)		
Status Affected:	C, DC	;, Z			
Encoding:	0000	) 1	LOdf	ffff	
Description:	Subtra the W is 0 th registe stored	act (2 regis le res er. If l bac	's comp ster fron sult is st 'd' is 1 t k in reg	blement n n register ored in th he result ister 'f'.	nethod) 'f'. If 'd' ne W is
Words:	1				
Cycles:	1				
Example 1:	SUBW	F	REG1,	1	
Before Instruct REG1 W C After Instructi REG1 W C Example 2: Before Instructi REG1 W C After Instructi	ction = = on = = ction = = on	3 2 ? 1 2 1 2 ?	; resu	ılt is posi	tive
REG1	=	0			
W	=	2			
С	=	1	; resu	ult is zero	
Example 3: Before Inst REG1 W C After Instructi	ructior = = = on	ו 1 2 ?			
REG1	=	0xFl	F		
W	=	2			
С	=	0	; resu	ult is nega	ative

SWAPF	Swap Nibbles in f
Syntax:	[label] SWAPF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$
Operation:	$(f<3:0>) \rightarrow (dest<7:4>);$ $(f<7:4>) \rightarrow (dest<3:0>)$
Status Affected:	None
Encoding:	0011 10df ffff
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.
Words:	1
Cycles:	1
Example	SWAPF REG1, 0
REG1 After Instructi REG1 W	= 0xA5 ion = 0xA5 = 0x5A
TRIS	Load TRIS Register
Syntax:	[ <i>label</i> ] TRIS f
Operands:	f = 5, 6 or 7
Operation:	$(W) \rightarrow TRIS$ register f
Status Affected:	None
Encoding:	0000 0000 0fff
Description:	TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register.
Words:	1
Cycles:	1
Example	TRIS PORTB
Before Instruc W After Instructi TRISB	ction = 0xA5 on = 0xA5



## FIGURE 12-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING -PIC16C54/55/56/57

# TABLE 12-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57

AC Chara	cteristics	$\label{eq:standard operating Conditions (unless otherwise specified)} \begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic Min Typ† Max Units Conditions					
30	TmcL	MCLR Pulse Width (low)	100*	—	_	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low		_	100*	ns	

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

# 13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 PIC16LCR54A-04I (Commercial, Industrial)				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
PIC16CR54A-04, 10, 20 PIC16CR54A-04I, 10I, 20I (Commercial, Industrial)			Standa Operat	ard Oper ting Tem	<b>ating C</b> perature	ondition 0° –40°	s (unless otherwise specified) C $\leq$ TA $\leq$ +70°C for commercial C $\leq$ TA $\leq$ +85°C for industrial		
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions		
	Vdd	Supply Voltage							
D001		PIC16LCR54A	2.0		6.25	V			
D001 D001A		PIC16CR54A	2.5 4.5		6.25 5.5	V V	RC and XT modes HS mode		
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>		1.5*	_	V	Device in SLEEP mode		
D003	Vpor	VDD Start Voltage to ensure Power-on Reset	_	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	Svdd	VDD Rise Rate to ensure Power-on Reset	0.05*		—	V/ms	See Section 5.1 for details on Power-on Reset		
	IDD	Supply Current <sup>(2)</sup>							
D005		PICLCR54A	—	10	20 70	μA μA	Fosc = 32 kHz, VDD = 2.0V Fosc = 32 kHz, VDD = 6.0V		
D005A		PIC16CR54A		2.0 0.8 90 4.8	3.6 1.8 350 10	mA mA μA	RC <sup>(3)</sup> and XT modes: Fosc = 4.0 MHz, VDD = 6.0V Fosc = 4.0 MHz, VDD = 3.0V Fosc = 200 kHz, VDD = 2.5V HS mode: Fosc = 10 MHz, VDD = 5.5V		
			—	9.0	20	mA	FOSC = 20  MHz,  VDD = 5.5  V		

Legend: Rows with standard voltage device data only are shaded for improved readability.

- \* These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

- 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
  - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
  - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k $\Omega$ .





# 15.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended) PIC16LC54A-04E (Extended)

PIC16I	PIC16L C54A-04E Standard Operating Conditions (unloss otherwise specified)								
(Exten	ded)	-	Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended						
PIC16C54A-04E, 10E, 20E (Extended)				Standard Operating Conditions (unless otherwise speciesOperating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions		
	Vdd	Supply Voltage							
D001		PIC16LC54A	3.0 2.5		6.25 6.25	V V	XT and RC modes LP mode		
D001A		PIC16C54A	3.5 4.5		5.5 5.5	V V	RC and XT modes HS mode		
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>		1.5*	—	V	Device in SLEEP mode		
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	-	Vss	_	V	See Section 5.1 for details on Power-on Reset		
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset		
	IDD	Supply Current <sup>(2)</sup>							
D010		PIC16LC54A	-	0.5	25	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC <sup>(3)</sup> and XT modes		
			-	11	27	μA	Fosc = 32 kHz, VDD = 2.5V, LP mode, Commercial		
				11	35	μA	Fosc = 32 kHz, VDD = 2.5V, LP mode, Industrial		
			—	11	37	μA	Fosc = 32 kHz, VDD = 2.5V, LP mode, Extended		
D010A		PIC16C54A	—	1.8	3.3	mA	Fosc = 4.0 MHz, VDD = 5.5V, RC <sup>(3)</sup> and XT modes		
			-	4.8	10	mA	Fosc = 10 MHz, VDD = 5.5V, HS mode		
			-	9.0	20	mA	Fosc = 20 MHz, VDD = 5.5V, HS mode		

Legend: Rows with standard voltage device data only are shaded for improved readability.

- \* These parameters are characterized but not tested.
- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
  - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
    - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
    - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
  - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

# 16.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean +  $3\sigma$ ) or (mean -  $3\sigma$ ) respectively, where  $\sigma$  is a standard deviation, over the whole temperature range.



FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

TABLE 16-1: RC OSCILLATOR FREQUENCIES
---------------------------------------

Сехт	Rext	Average Fosc @ 5 V, 25°C			
20 pF	3.3K	5 MHz	± 27%		
	5K	3.8 MHz	± 21%		
	10K	2.2 MHz	± 21%		
	100K	262 kHz	± 31%		
100 pF	3.3K	1.6 MHz	± 13%		
	5K	1.2 MHz	± 13%		
	10K	684 kHz	± 18%		
	100K	71 kHz	± 25%		
300 pF	3.3K	660 kHz	± 10%		
	5.0K	484 kHz	± 14%		
	10K	267 kHz	± 15%		
	100K	29 kHz	± 19%		

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is  $\pm 3$  standard deviation from average value for VDD = 5V.

Typical: statistical mean @ 25°C. Maximum: mean - 3 s (-40°C to 125°C) Minimum: mean

FIGURE 16-14: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 PF, 25°C)

FIGURE 16-15: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 PF, -40°C to +85°C)



# 18.0 DEVICE CHARACTERIZATION - PIC16LC54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean +  $3\sigma$ ) or (mean -  $3\sigma$ ) respectively, where  $\sigma$  is a standard deviation, over the whole temperature range.



FIGURE 18-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

# TABLE 18-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Average Fosc @ 5V, 25°C				
20 pF	3.3K	5 MHz	± 27%			
	5K	3.8 MHz	± 21%			
	10K	2.2 MHz	± 21%			
	100K	262 kHz	± 31%			
100 pF	3.3K	1.63 MHz	± 13%			
	5K	1.2 MHz	± 13%			
	10K	684 kHz	± 18%			
	100K	71 kHz	± 25%			
300 pF	3.3K	660 kHz	± 10%			
	5.0K	484 kHz	± 14%			
	10K	267 kHz	± 15%			
	100K	29 kHz	± 19%			

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is  $\pm 3$  standard deviation from average value for VDD = 5V.

#### 19.4 **Timing Diagrams and Specifications**



#### **FIGURE 19-3: EXTERNAL CLOCK TIMING - PIC16C5X-40**

#### **EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X-40 TABLE 19-1:**

AC Chara	$\label{eq:aracteristics} \begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \end{array}$				1)		
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
	Fosc	External CLKIN Frequency <sup>(1)</sup>	20		40	MHz	HS osc mode
1	Tosc	External CLKIN Period <sup>(1)</sup>	25			ns	HS osc mode
2	Тсу	Instruction Cycle Time <sup>(2)</sup>	_	4/Fosc		_	
3	TosL, TosH	Clock in (OSC1) Low or High Time	6.0*			ns	HS oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time			6.5*	ns	HS oscillator

- \* These parameters are characterized but not tested.
- † Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

  - 2: Instruction cycle period (TCY) equals four times the input oscillator time base period.



# FIGURE 19-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X-40

# TABLE 19-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X-40

AC CharacteristicsStandard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial)Operating Voltage VDD range is described in Section 19.1.							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1000*		_	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns	

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested. NOTES:

# PIC16C5X



# FIGURE 20-9: IOL vs. VOL, VDD = 5 V



NOTES: