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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57c-40-sp

PIC16C5X

NOTES:

5.2 Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides an 18 ms nominal time-out on RESET regardless of Oscillator mode used. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows VDD to rise above VDD min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after the voltage on the MCLR/VPP pin has reached a logic high (VIH) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The Device Reset time delay will vary from chip to chip due to VDD, temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the PIC16C5X from SLEEP mode automatically.

5.3 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be RESET in the event of a brown-out.

To RESET PIC16C5X devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 5-6, Figure 5-7 and Figure 5-8.

FIGURE 5-6: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1

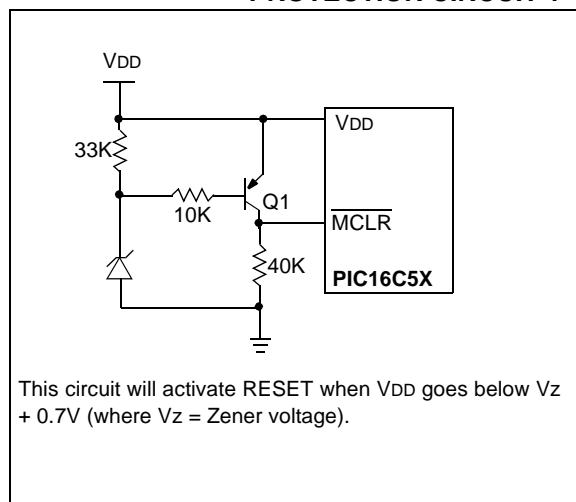


FIGURE 5-7: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2

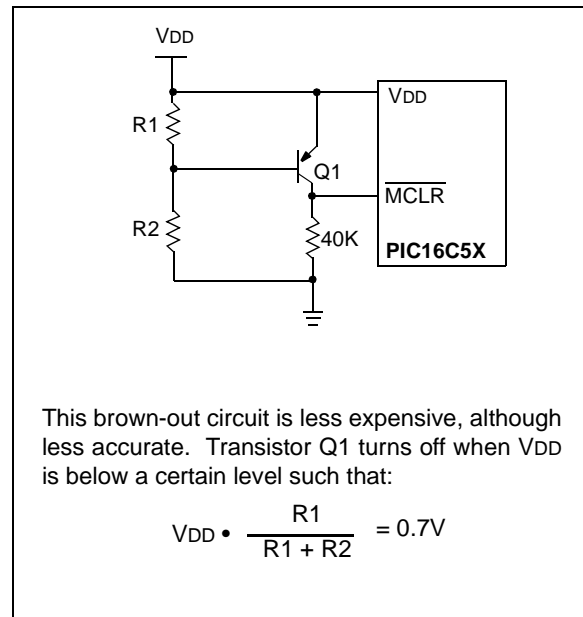
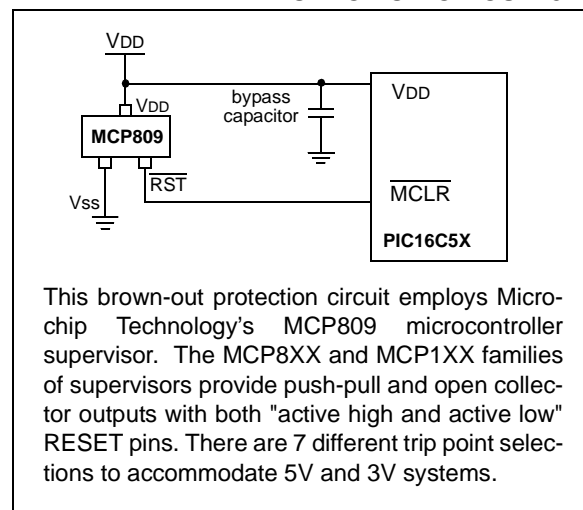


FIGURE 5-8: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



7.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., `MOVF PORTB, W`) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

7.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used ($RA<3:0>$). Bits 7-4 are unimplemented and read as '0's.

7.2 PORTB

PORTB is an 8-bit I/O Register ($PORTB<7:0>$).

7.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58 and PIC16CR58.

7.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the `TRIS f` instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

Note: A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

7.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 7-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF PORTB, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared ($= 0$). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

FIGURE 7-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN

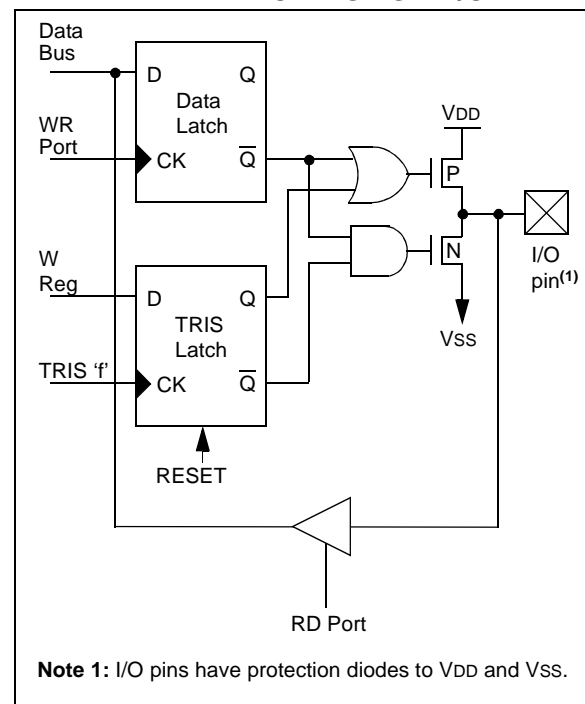


TABLE 7-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	TRIS	I/O Control Registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'

7.6 I/O Programming Considerations

7.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 7-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

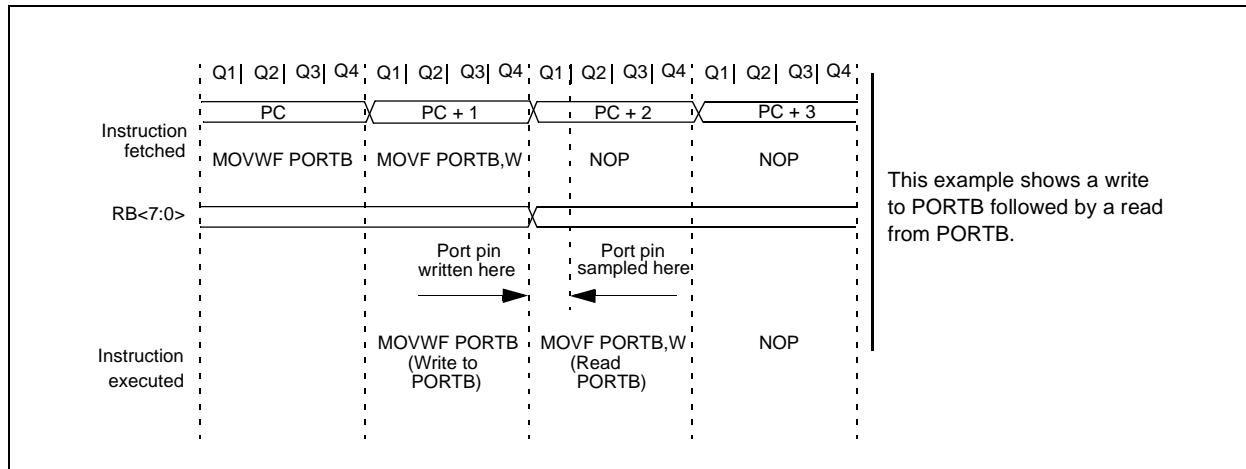
EXAMPLE 7-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;
;          PORT latch  PORT pins
;          -----
BCF  PORTB, 7  ;01pp pppp  11pp pppp
BCF  PORTB, 6  ;10pp pppp  11pp pppp
MOVLW H'3F'    ;
TRIS  PORTB    ;10pp pppp  10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

7.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 7-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 7-2: SUCCESSIVE I/O OPERATION



9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC16C5X family of microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator Selection (Section 4.0)
- RESET (Section 5.0)
- Power-On Reset (Section 5.1)
- Device Reset Timer (Section 5.2)
- Watchdog Timer (WDT) (Section 9.2)
- SLEEP (Section 9.3)
- Code protection (Section 9.4)
- ID locations (Section 9.5)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in RESET until the crystal oscillator is stable. With this timer on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake up from SLEEP through external RESET or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

REGISTER 9-2: CONFIGURATION WORD FOR PIC16C54/C55/C56/C57

—	—	—	—	—	—	—	—	CP	WDTE	FOSC1	FOSC0
bit 11											bit 0

bit 11-4: **Unimplemented:** Read as '0'

bit 3: **CP:** Code protection bit.

1 = Code protection off

0 = Code protection on

bit 2: **WDTE:** Watchdog timer enable bit

1 = WDT enabled

0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator selection bits⁽²⁾

00 = LP oscillator

01 = XT oscillator

10 = HS oscillator

11 = RC oscillator

Note 1: Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

2: PIC16LV54A supports XT, RC and LP oscillator only.

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

1 = bit is set

0 = bit is cleared

x = bit is unknown

9.3 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

9.3.1 SLEEP

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the \overline{TO} bit (STATUS<4>) is set, the \overline{PD} bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the \overline{MCLR}/VPP pin low.

For lowest current consumption while powered down, the $T0CKI$ input should be at VDD or VSS and the \overline{MCLR}/VPP pin must be at a logic high level ($\overline{MCLR} = V_{IH}$).

9.3.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. An external RESET input on \overline{MCLR}/VPP pin.
2. A Watchdog Timer Time-out Reset (if WDT was enabled).

Both of these events cause a device RESET. The \overline{TO} and \overline{PD} bits can be used to determine the cause of device RESET. The \overline{TO} bit is cleared if a WDT time-out occurred (and caused wake-up). The \overline{PD} bit, which is set on power-up, is cleared when SLEEP is invoked.

The WDT is cleared when the device wakes from SLEEP, regardless of the wake-up source.

9.4 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

9.5 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

Note: Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

PIC16C5X

NOTES:

GOTO Unconditional Branch

Syntax: [*label*] GOTO *k*

Operands: $0 \leq k \leq 511$

Operation: $k \rightarrow PC<8:0>;$
 $STATUS<6:5> \rightarrow PC<10:9>$

Status Affected: None

Encoding:

101k	kkkk	kkkk
------	------	------

Description: GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two-cycle instruction.

Words: 1

Cycles: 2

Example: GOTO THERE

After Instruction
 PC = address (THERE)

INCF Increment f

Syntax: [*label*] INCF *f*,*d*

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

0010	10df	ffff
------	------	------

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example: INCF CNT, 1

Before Instruction
 CNT = 0xFF
 Z = 0

After Instruction
 CNT = 0x00
 Z = 1

INCFSZ Increment f, Skip if 0

Syntax: [*label*] INCFSZ *f*,*d*

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{dest})$, skip if result = 0

Status Affected: None

Encoding:

0011	11df	ffff
------	------	------

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example: HERE INCFSZ CNT, 1
 GOTO LOOP
 CONTINUE •
 •
 •

Before Instruction
 PC = address (HERE)

After Instruction
 CNT = CNT + 1;
 if CNT = 0,
 PC = address (CONTINUE);
 if CNT \neq 0,
 PC = address (HERE + 1)

PIC16C5X

13.4 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	V _{IL}	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	V _{SS} V _{SS} V _{SS} V _{SS} V _{SS}	— — — — —	0.15 V _{DD} 0.15 V _{DD} 0.15 V _{DD} 0.15 V _{DD} 0.3 V _{DD}	V V V V V	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes
D040	V _{IH}	Input High Voltage I/O ports I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	0.45 V _{DD} 2.0 0.36 V _{DD} 0.85 V _{DD} 0.85 V _{DD} 0.85 V _{DD} 0.7 V _{DD}	— — — — — — —	V _{DD} V _{DD} V _{DD} V _{DD} V _{DD} V _{DD} V _{DD}	V V V V V V V	For all V _{DD} ⁽⁴⁾ 4.0V < V _{DD} ≤ 5.5V ⁽⁴⁾ V _{DD} > 5.5V RC mode only ⁽³⁾ XT, HS and LP modes
D050	V _{HYS}	Hysteresis of Schmitt Trigger inputs	0.15 V _{DD} *	—	—	V	
D060	I _{IL}	Input Leakage Current^(1,2) I/O ports MCLR MCLR T0CKI OSC1	−1.0 −5.0 — −3.0 −3.0	0.5 — 0.5 0.5 0.5	+1.0 — +5.0 +3.0 +3.0	μA μA μA μA μA	For V_{DD} ≤ 5.5V: V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance V _{PIN} = V _{SS} + 0.25V V _{PIN} = V _{DD} V _{SS} ≤ V _{PIN} ≤ V _{DD} V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT, HS and LP modes
D080	V _{OL}	Output Low Voltage I/O ports OSC2/CLKOUT	— —	— —	0.6 0.6	V V	I _{OL} = 8.7 mA, V _{DD} = 4.5V I _{OL} = 1.6 mA, V _{DD} = 4.5V, RC mode only
D090	V _{OH}	Output High Voltage⁽²⁾ I/O ports OSC2/CLKOUT	V _{DD} − 0.7 V _{DD} − 0.7	— —	— —	V V	I _{OH} = −5.4 mA, V _{DD} = 4.5V I _{OH} = −1.0 mA, V _{DD} = 4.5V, RC mode only

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

14.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum” or “minimum” represents (mean + 3 σ) or (mean – 3 σ) respectively, where σ is a standard deviation, over the whole temperature range.

FIGURE 14-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

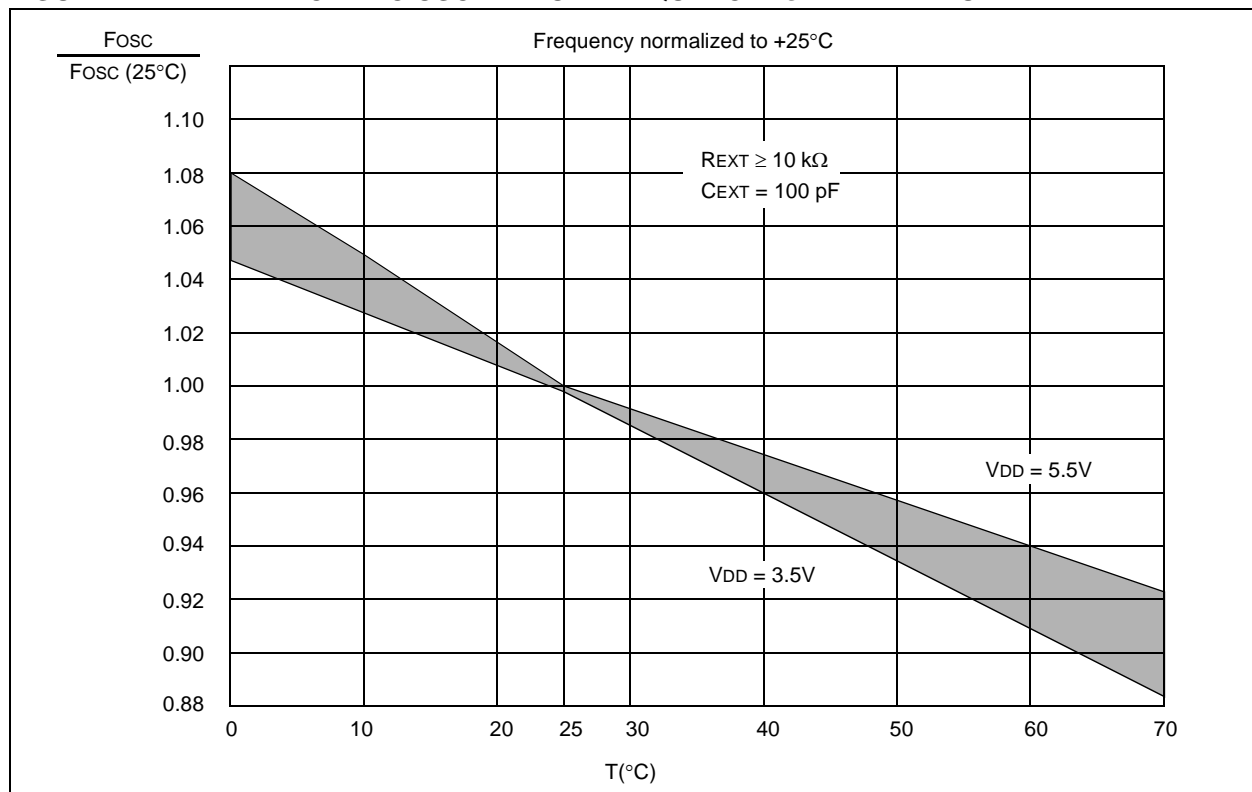


TABLE 14-1: RC OSCILLATOR FREQUENCIES

C_{EXT}	R_{EXT}	Average $F_{osc} @ 5 \text{ V}, 25^\circ\text{C}$	
20 pF	3.3K	5 MHz	$\pm 27\%$
	5K	3.8 MHz	$\pm 21\%$
	10K	2.2 MHz	$\pm 21\%$
	100K	262 kHz	$\pm 31\%$
100 pF	3.3K	1.6 MHz	$\pm 13\%$
	5K	1.2 MHz	$\pm 13\%$
	10K	684 kHz	$\pm 18\%$
	100K	71 kHz	$\pm 25\%$
300 pF	3.3K	660 kHz	$\pm 10\%$
	5.0K	484 kHz	$\pm 14\%$
	10K	267 kHz	$\pm 15\%$
	100K	29 kHz	$\pm 19\%$

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviations from the average value for $V_{DD} = 5\text{V}$.

FIGURE 14-13: MAXIMUM IDD VS. FREQUENCY (EXTERNAL CLOCK, -40°C TO +85°C)

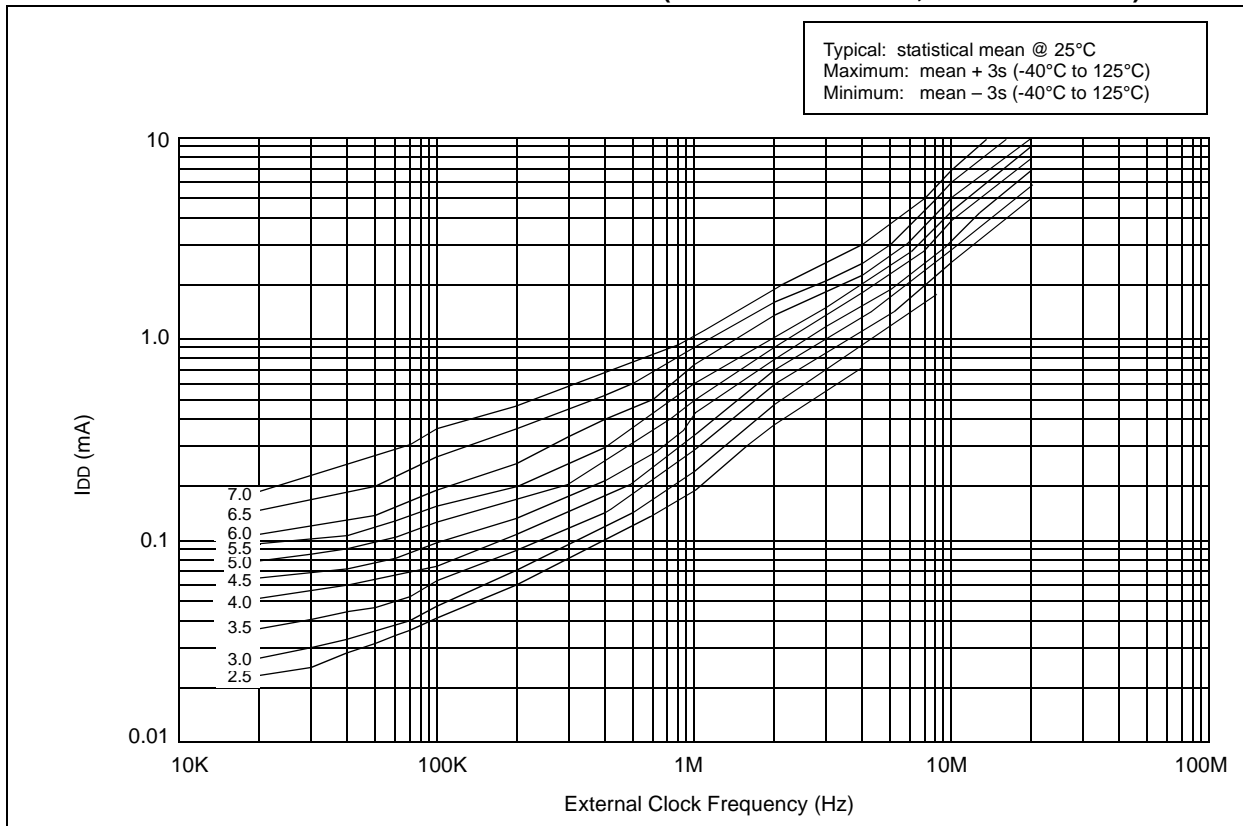
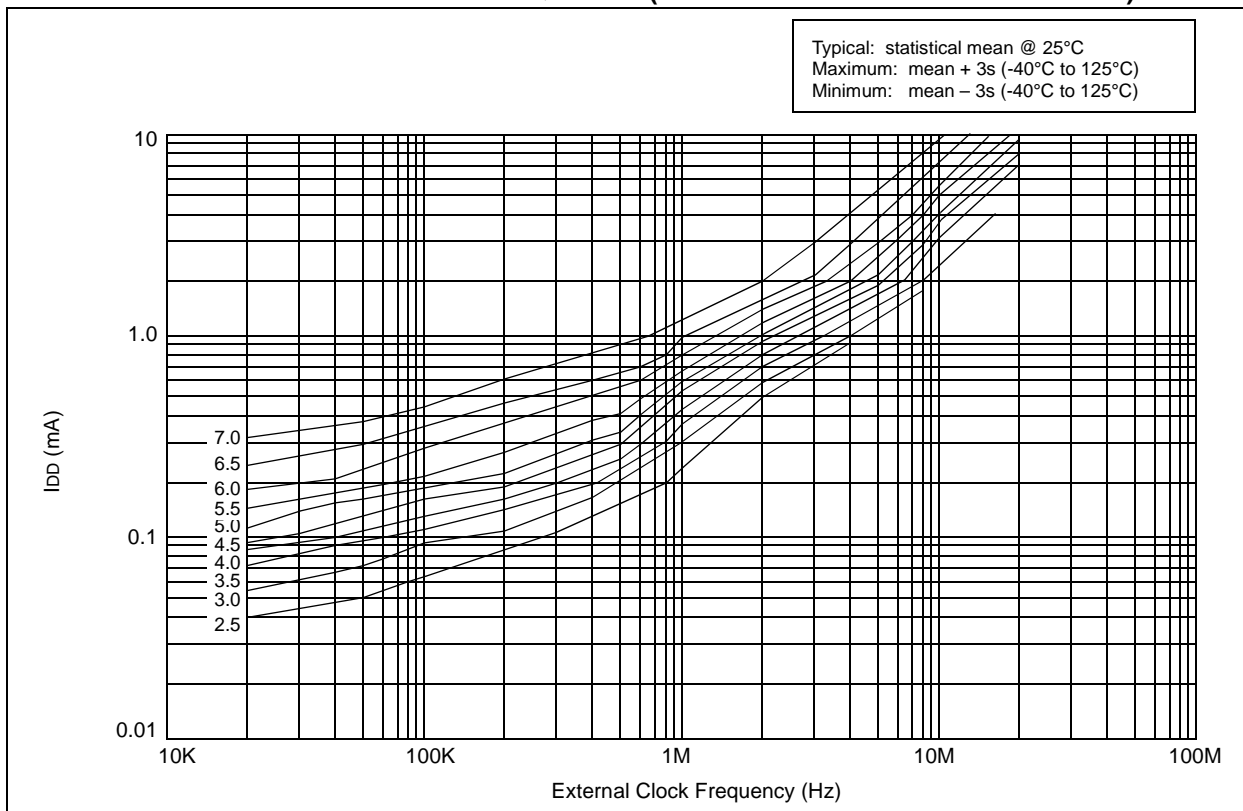


FIGURE 14-14: MAXIMUM I_{DD} vs. FREQUENCY (EXTERNAL CLOCK -55°C TO +125°C)



PIC16C5X

TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I -40°C ≤ TA ≤ +125°C for extended							
AC Characteristics							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
1	Tosc	External CLKIN Period ⁽¹⁾	250	—	—	ns	XT osc mode
			500	—	—	ns	XT osc mode (PIC16LV54A)
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	μs	LP osc mode
		Oscillator Period ⁽¹⁾	250	—	—	ns	RC osc mode
			500	—	—	ns	RC osc mode (PIC16LV54A)
			250	—	10,000	ns	XT osc mode
			500	—	—	ns	XT osc mode (PIC16LV54A)
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	μs	LP osc mode
2	Tcy	Instruction Cycle Time ⁽²⁾	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

PIC16C5X

17.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial)		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial					
PIC16C5X PIC16CR5X (Commercial, Industrial)		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage					
		PIC16LC5X	2.5	—	5.5	V	-40°C ≤ TA ≤ +85°C, 16LCR5X
			2.7	—	5.5	V	-40°C ≤ TA ≤ 0°C, 16LC5X
D001A		PIC16C5X	2.5	—	5.5	V	0°C ≤ TA ≤ +85°C 16LC5X
			3.0	—	5.5	V	RC, XT, LP and HS mode from 0 - 10 MHz
			4.5	—	5.5	V	from 10 - 20 MHz
D002	VDR	RAM Data Retention Voltage⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. V_{DD} , $C_{EXT} = 300$ pF, 25°C

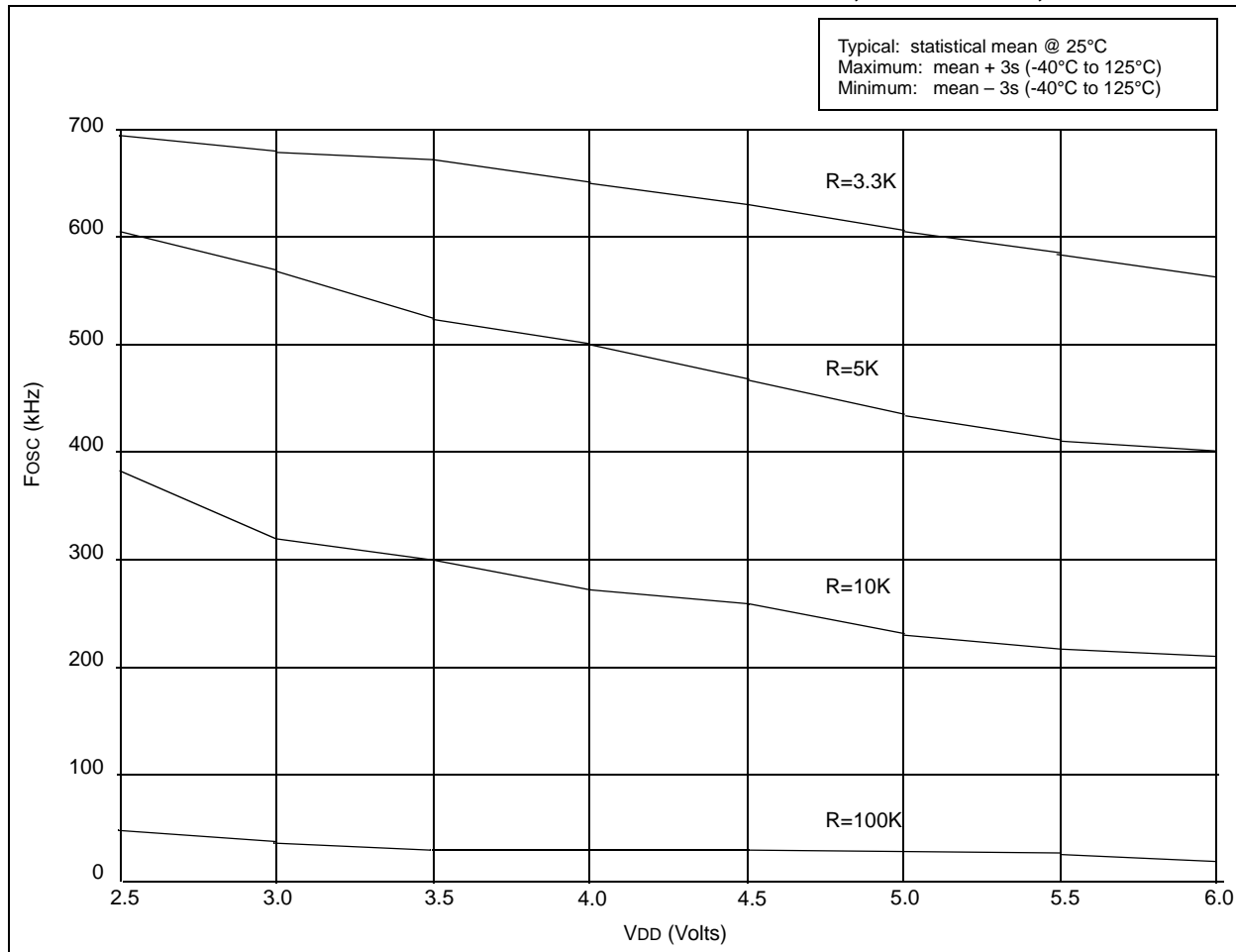


FIGURE 18-5: TYPICAL I_{PD} vs. V_{DD} , WATCHDOG DISABLED (25°C)

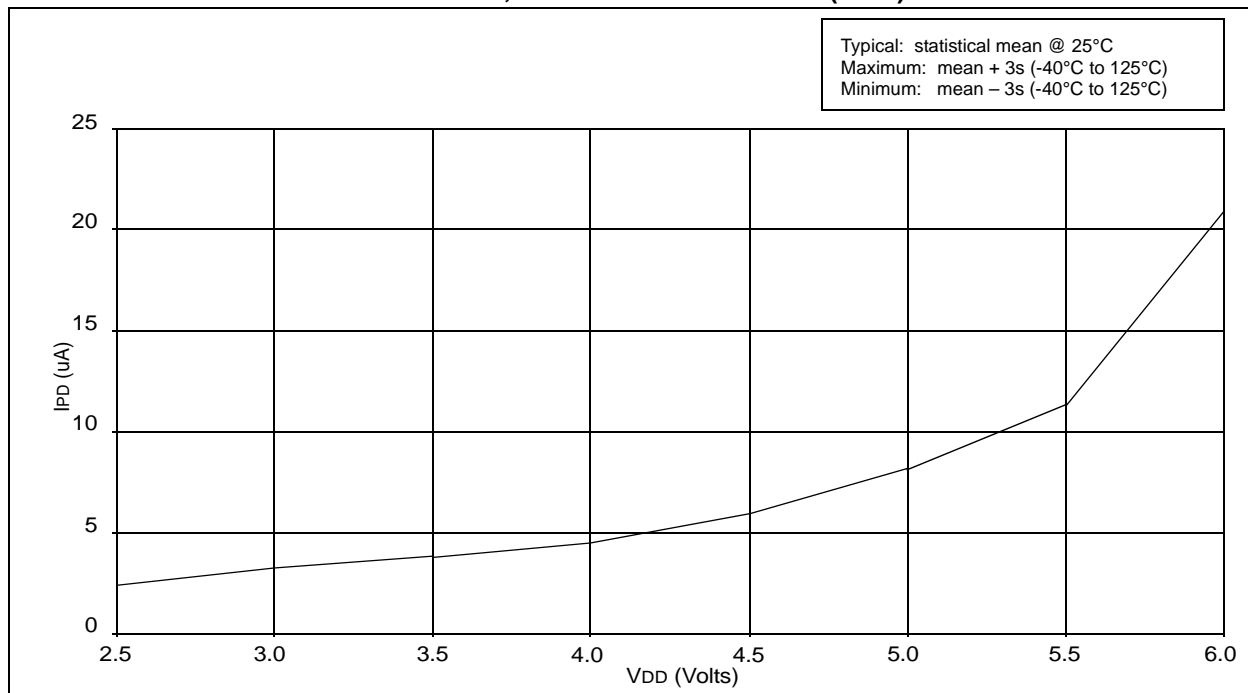


FIGURE 18-6: TYPICAL I_{PD} vs. V_{DD} , WATCHDOG ENABLED (25°C)

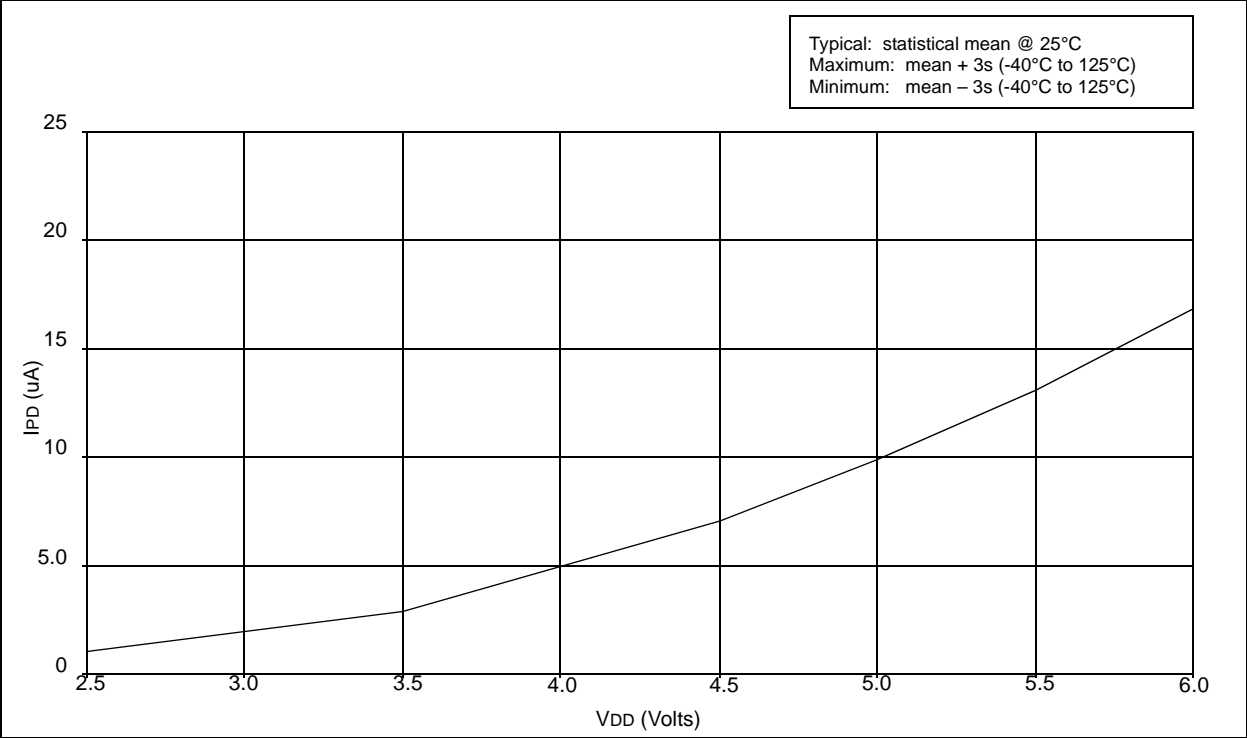


FIGURE 18-7: TYPICAL I_{PD} vs. V_{DD} , WATCHDOG ENABLED (-40°C, 85°C)

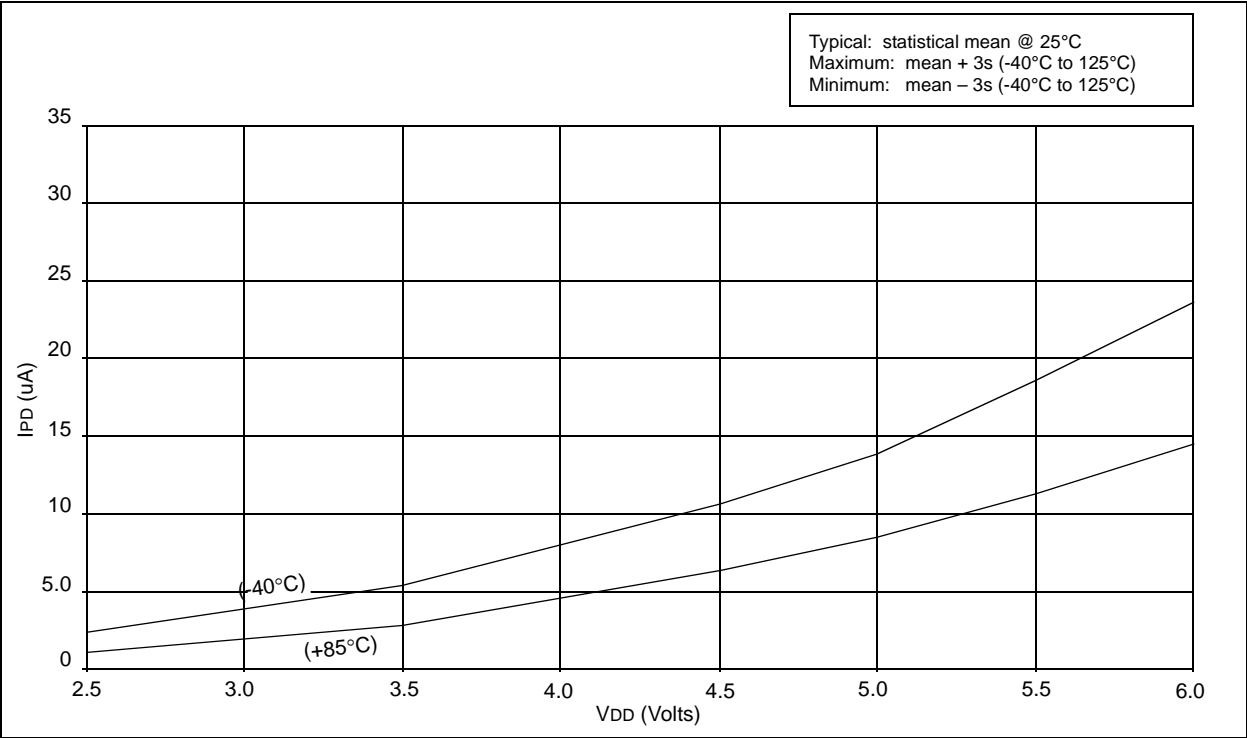


FIGURE 18-8: V_{TH} (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. V_{DD}

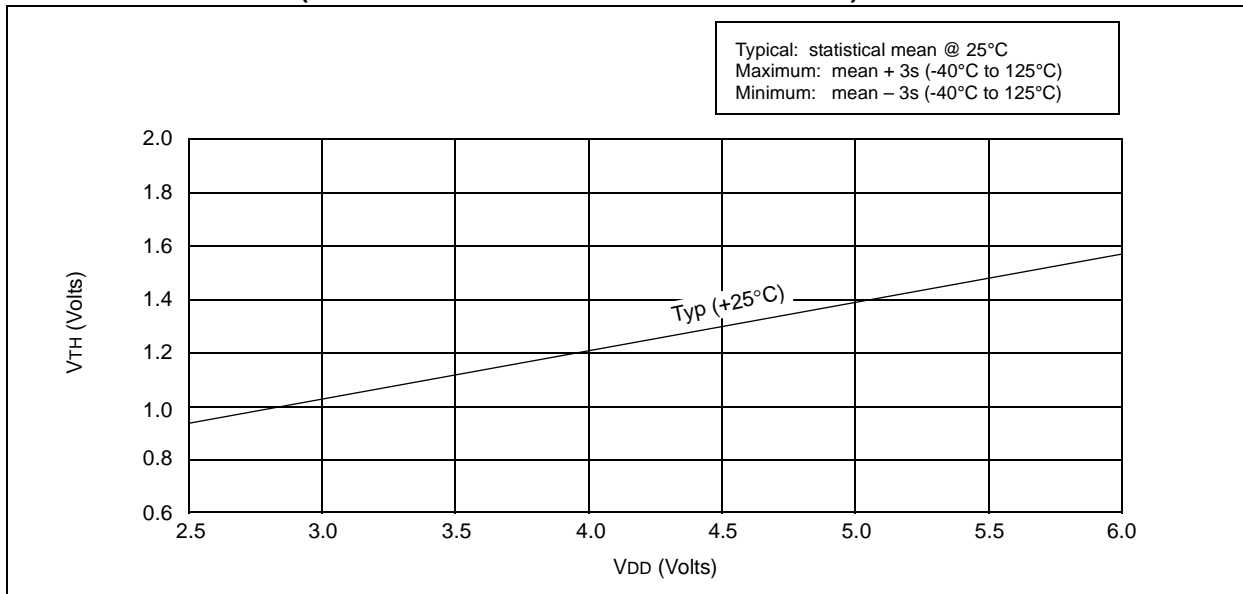


FIGURE 18-9: V_{IH} , V_{IL} OF \overline{MCLR} , $T0CKI$ AND $OSC1$ (IN RC MODE) vs. V_{DD}

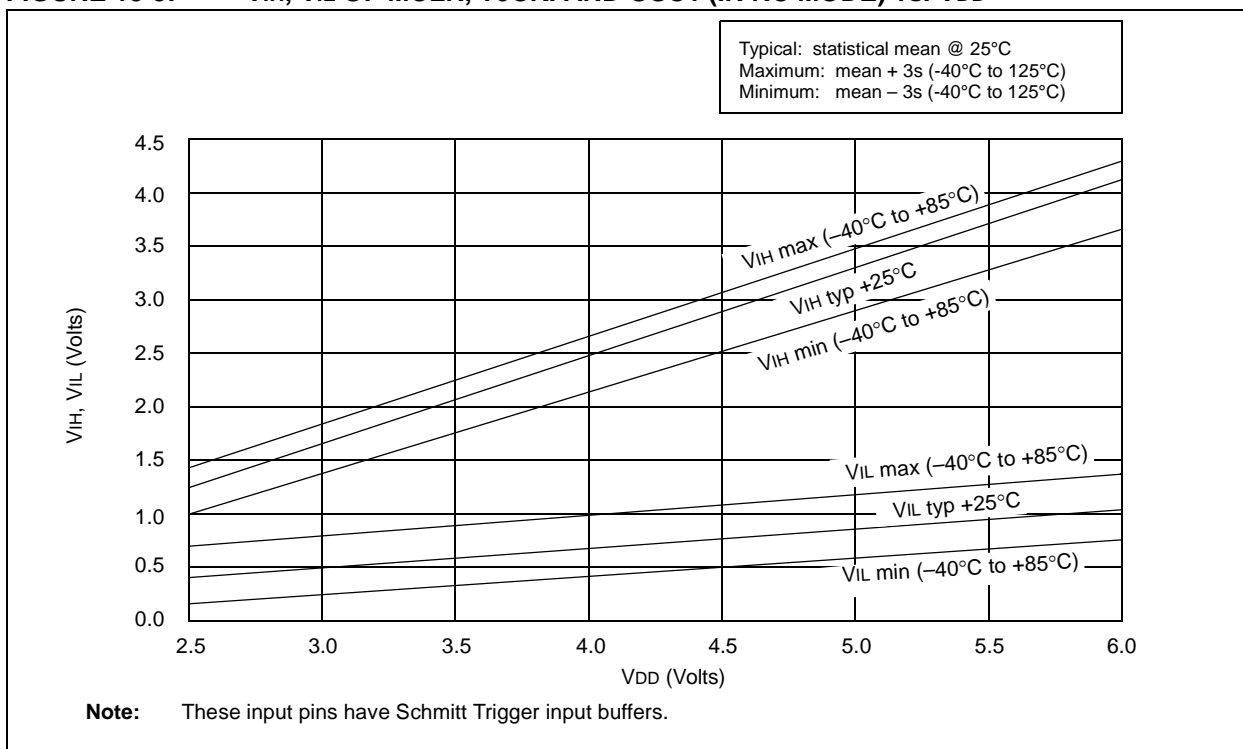


FIGURE 18-12: TYPICAL I_{DD} vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, 25°C)

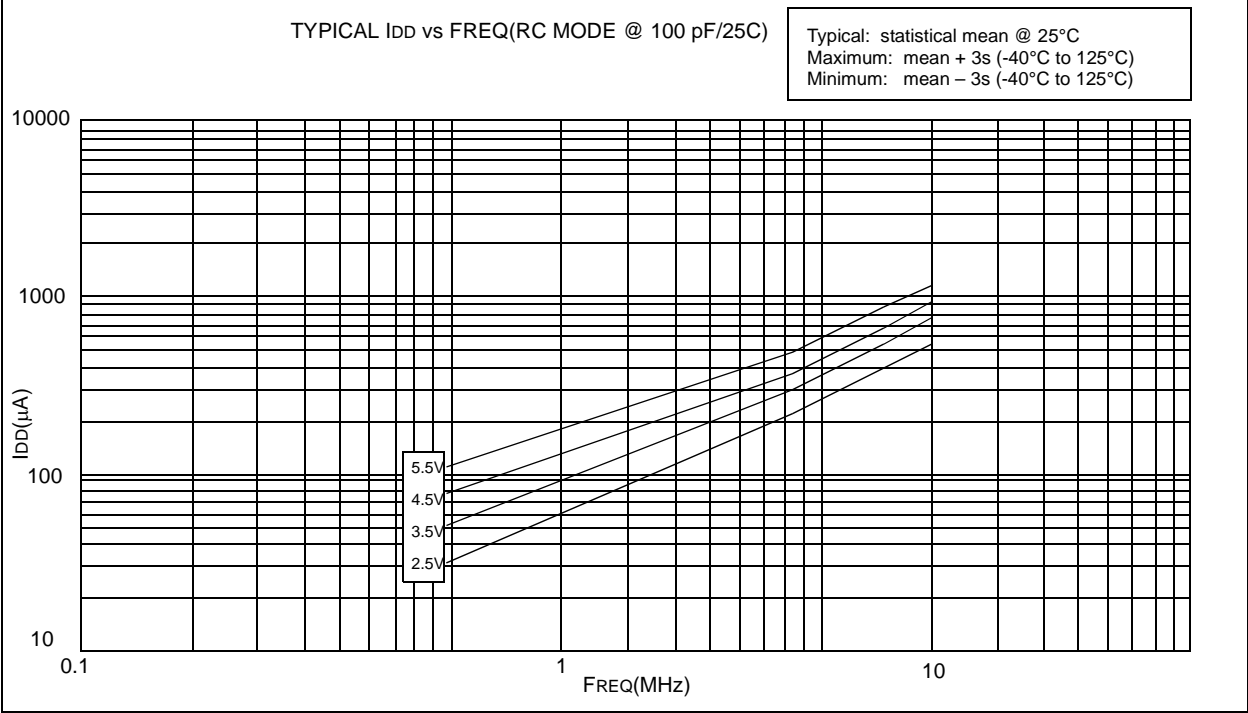


FIGURE 18-13: TYPICAL I_{DD} vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, 25°C)

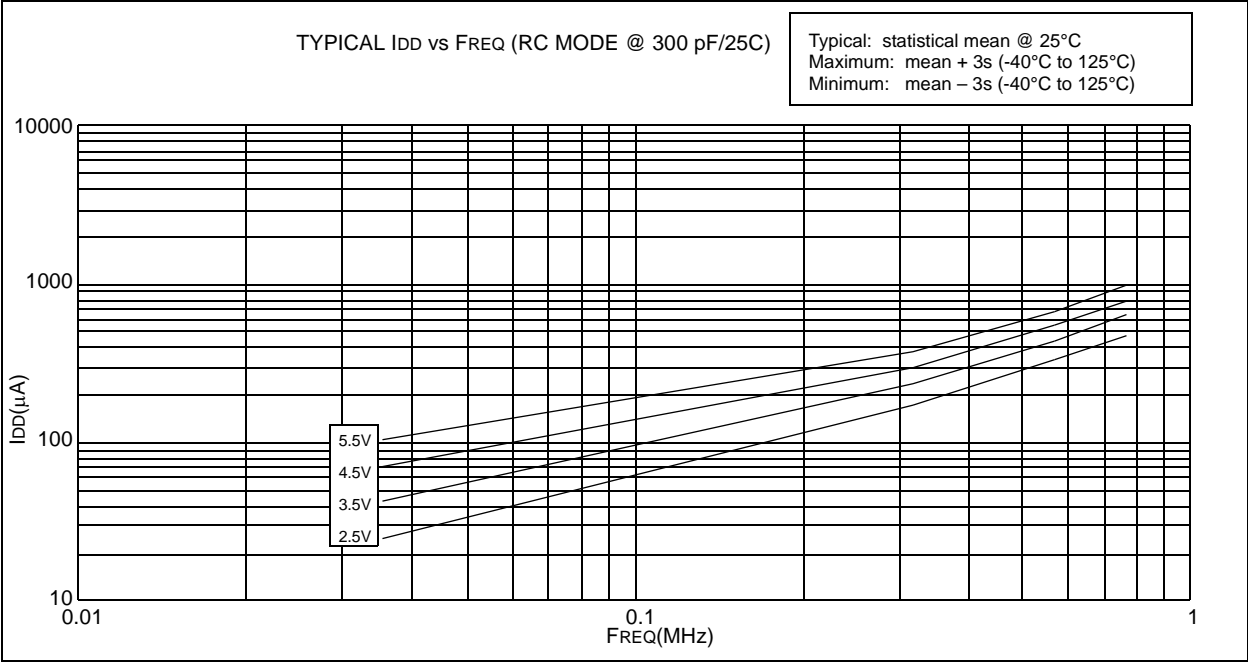


FIGURE 19-4: CLKOUT AND I/O TIMING - PIC16C5X-40

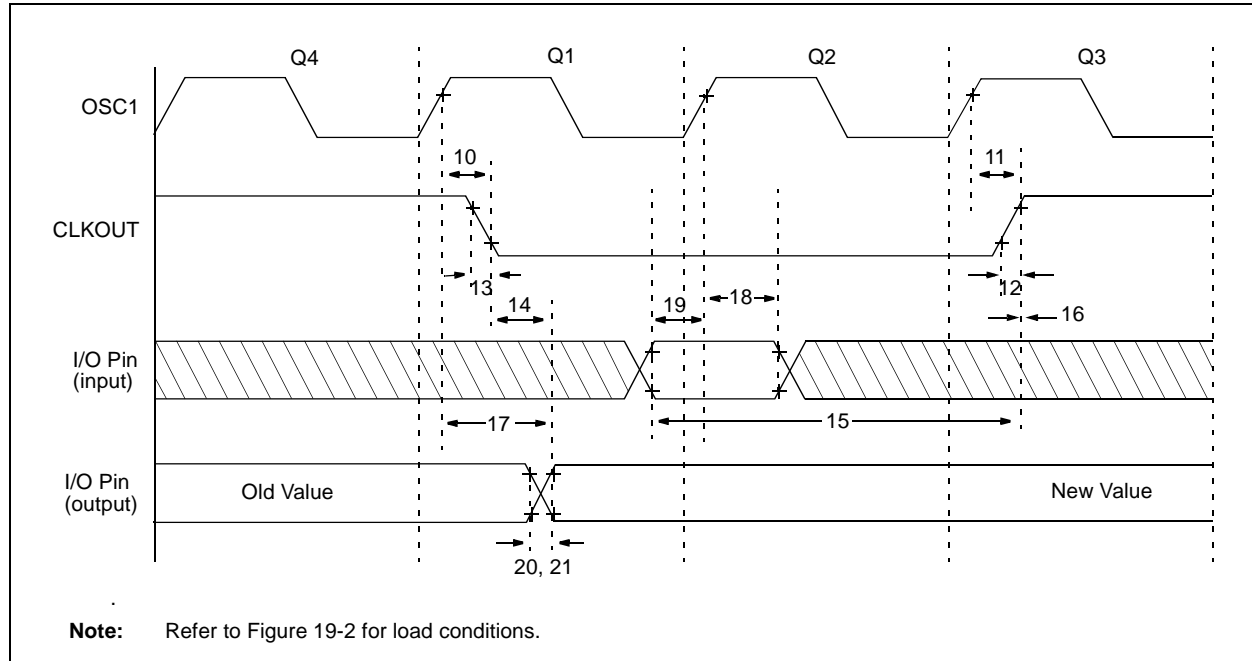


TABLE 19-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X-40

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ^(1,2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ^(1,2)	—	15	30**	ns
12	TckR	CLKOUT rise time ^(1,2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time ^(1,2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ^(1,2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ^(1,2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ ^(1,2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽²⁾	—	—	100	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽²⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

2: Refer to Figure 19-2 for load conditions.

FIGURE 20-4: V_{TH} (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. V_{DD}

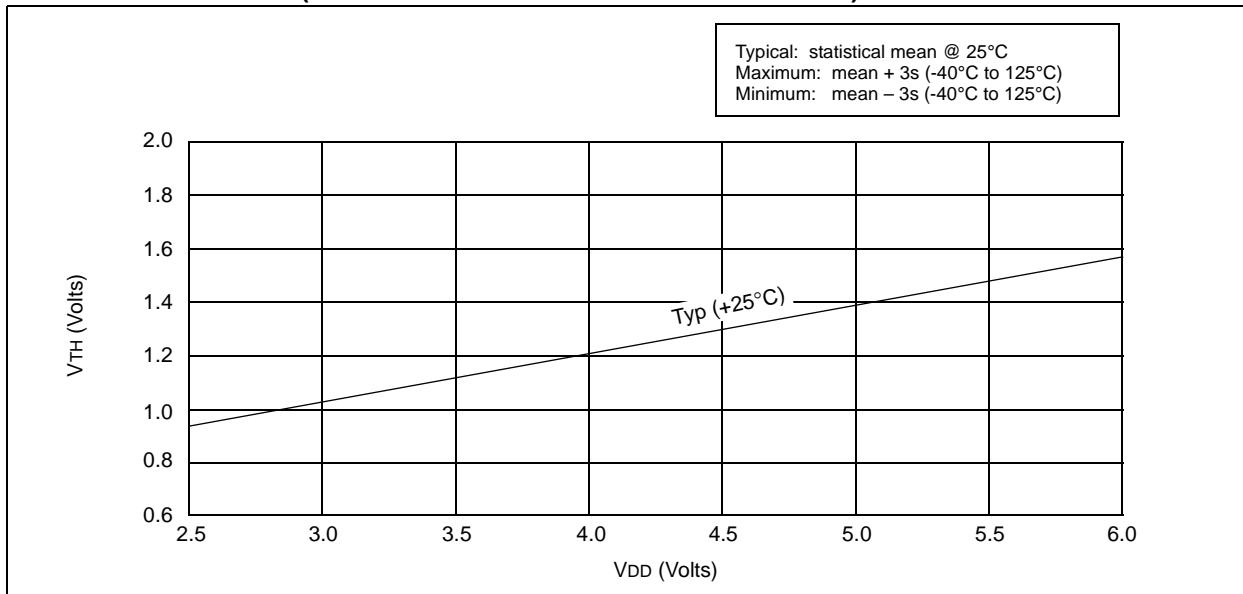


FIGURE 20-5: V_{TH} (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (HS MODE) vs. V_{DD}

