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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57ct-04i-ss

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TABLE 1-1: PIC16C5X FAMILY OF DEVICES

Features	PIC16C54	PIC16CR54	PIC16C55	PIC16C56	PIC16CR56				
Maximum Operation Frequency	40 MHz	20 MHz	40 MHz	40 MHz	20 MHz				
EPROM Program Memory (x12 words)	512	—	512	1K	—				
ROM Program Memory (x12 words)	—	512	—	—	1K				
RAM Data Memory (bytes)	25	25	24	25	25				
Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0				
I/O Pins	12	12	20	12	12				
Number of Instructions	33	33	33	33	33				
Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP				
All PIC [®] Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.									

PIC16C58 Features **PIC16C57** PIC16CR57 PIC16CR58 Maximum Operation Frequency 20 MHz 40 MHz 40 MHz 20 MHz EPROM Program Memory (x12 words) 2K 2K ____ _ ROM Program Memory (x12 words) 2K 2K _ _ RAM Data Memory (bytes) 72 72 73 73 Timer Module(s) TMR0 TMR0 TMR0 TMR0 I/O Pins 20 20 12 12 Number of Instructions 33 33 33 33 28-pin DIP, SOIC; 28-pin DIP, SOIC; 18-pin DIP, SOIC; 18-pin DIP, SOIC; Packages 28-pin SSOP 28-pin SSOP 20-pin SSOP 20-pin SSOP All PIC® Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.

	Pi	n Numb	er	Pin	Buffer	
Pin Name	DIP	SOIC	SSOP	Туре	Туре	Description
RA0	17	17	19	I/O	TTL	Bi-directional I/O port
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RB0	6	6	7	I/O	TTL	Bi-directional I/O port
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	
RB5	11	11	12	I/O	TTL	
RB6	12	12	13	I/O	TTL	
RB7	13	13	14	I/O	TTL	
TOCKI	3	3	3	I	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in use, to reduce current consumption.
MCLR/Vpp	4	4	4	I	ST	Master clear (RESET) input/programming voltage input. This pin is an active low RESET to the device. Voltage on the MCLR/VPP pin must not exceed VDD to avoid unin- tended entering of Programming mode.
OSC1/CLKIN	16	16	18	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	17	0		Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
Vdd	14	14	15,16	Р	_	Positive supply for logic and I/O pins.
Vss	5	5	5,6	Р	_	Ground reference for logic and I/O pins.

TABLE 3-1:PINOUT DESCRIPTION - PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16CR58,
PIC16CR58

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

4.0 OSCILLATOR CONFIGURATIONS

4.1 Oscillator Types

PIC16C5Xs can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- 1. LP: Low Power Crystal
- 2. XT: Crystal/Resonator
- 3. HS: High Speed Crystal/Resonator
- 4. RC: Resistor/Capacitor

Note: Not all oscillator selections available for all parts. See Section 9.1.

4.2 Crystal Oscillator/Ceramic Resonators

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 4-1). The PIC16C5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 4-2).

FIGURE 4-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



FIGURE 4-2:

EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)



TABLE 4-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS -PIC16C5X, PIC16CR5X

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	68-100 pF	68-100 pF
	2.0 MHz	15-33 pF	15-33 pF
	4.0 MHz	10-22 pF	10-22 pF
HS	8.0 MHz	10-22 pF	10-22 pF
	16.0 MHz	10 pF	10 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 4-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR -PIC16C5X. PIC16CR5X

Osc Type	Crystal Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz ⁽¹⁾	15 pF	15 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Note 1: For VDD > 4.5V, C1 = C2 \approx 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

Note: If you change from this device to another device, please verify oscillator characteristics in your application.

NOTES:





9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of realtime applications. The PIC16C5X family of microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator Selection (Section 4.0)
- RESET (Section 5.0)
- Power-On Reset (Section 5.1)
- Device Reset Timer (Section 5.2)
- Watchdog Timer (WDT) (Section 9.2)
- SLEEP (Section 9.3)
- Code protection (Section 9.4)
- ID locations (Section 9.5)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in RESET until the crystal oscillator is stable. With this timer on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake up from SLEEP through external RESET or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

9.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT Reset or Wake-up Reset generates a device RESET.

The $\overline{\text{TO}}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset (Section 6.3).

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 9.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

9.2.1 WDT PERIOD

An 8-bit counter is available as a prescaler for the Timer0 module (Section 8.2), or as a postscaler for the Watchdog Timer (WDT), respectively. For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not

both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio (Section 6.4).

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see Device Characterization).

Under worst case conditions (VDD = Min., Temperature = Max., WDT prescaler = 1:128), it may take several seconds before a WDT time-out occurs.

9.2.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction RESETS the WDT and the prescaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.



TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	<u>Value</u> on MCLR and WDT Reset
N/A	OPTION	—	—	Tosc	Tose	PSA	PS2	PS1	PS0	11 1111	11 1111

Legend: u = unchanged, - = unimplemented, read as '0'. Shaded cells not used by Watchdog Timer.

BSF	Bit Set f						
Syntax:	ax: [label] BSF f,b						
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ 0 \leq b \leq 7 \end{array}$	$\begin{array}{l} 0 \leq f \leq 31 \\ 0 \leq b \leq 7 \end{array}$					
Operation:	$1 \rightarrow (f < b)$	>)					
Status Affected:	None						
Encoding:	0101	bbbf	ffff				
Description:	Bit 'b' in register 'f' is set.						
Words:	1						
Cycles:	1						
Example:	BSF	FLAG_RE	G, 7				
Before Instruction FLAG_REG = 0x0A After Instruction							
FLAG_F	REG = C)x8A					

BTFSC	Bit Test f, Skip if Clear							
Syntax:	[label] BTFSC f,b							
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ 0 \leq b \leq 7 \end{array}$							
Operation:	skip if (f) = 0						
Status Affected:	None							
Encoding:	0110	bbbf	ffff					
Description:	If bit 'b' in register 'f' is 0 then the next instruction is skipped. If bit 'b' is 0 then the next instruc- tion fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a 2-cycle instruction							
Words:	1							
Cycles:	1(2)							
Example:	HERE FALSE TRUE	BTFSC GOTO • •	FLAG,1 PROCESS	S_CODE				
Before Instru	ction							
PC After Instructi if FLAG< PC if FLAG< PC	= (1> = (1> = (1> = =	address 0, address (1, address (1	(HERE) TRUE); FALSE)					

BTFSS	Bit Test f, Skip if Set								
Syntax:	[label] BTFSS f,b								
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ 0 \leq b < 7 \end{array}$								
Operation:	skip if (f) = 1								
Status Affected:	None								
Encoding:	0111 bbbf ffff								
Description:	If bit 'b' in register 'f' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruc- tion fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a 2-cycle instruction.								
Words:	1								
Cycles:	1(2)								
Example:	HERE BTFSS FLAG,1 FALSE GOTO PROCESS_CODI TRUE • •	Ξ							
Before Instr	ruction								
PC	= address (HERE)								
After Instruc	ction								
	< i > = 0, = address (FALSE)								
if FLAG<	<1> = 1.								
PC	= address (TRUE)								

11.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB[®] IDE Software
- Assemblers/Compilers/Linkers
 - MPASM[™] Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK™ Object Linker/
 - MPLIB[™] Object Librarian
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - ICEPIC[™] In-Circuit Emulator
- In-Circuit Debugger
- MPLAB ICD
- Device Programmers
 - PRO MATE[®] II Universal Device Programmer
- PICSTART[®] Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
 - PICDEM[™]1 Demonstration Board
 - PICDEM 2 Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 17 Demonstration Board
 - KEELOQ[®] Demonstration Board

11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows[®]-based application that contains:

- An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file
 - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

11.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

12.7 Timing Diagrams and Specifications



FIGURE 12-2: EXTERNAL CLOCK TIMING - PIC16C54/55/56/57

TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57

		Standard Operating Conditions (unless otherwise specified)										
AC Characteristics		Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial										
		-40	$-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial									
		-40	$-40^{\circ}C \le TA \le +125^{\circ}C$ for extended									
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions					
1A	Fosc	External CLKIN Frequency ⁽¹⁾	DC		4.0	MHz	XT OSC mode					
			DC	—	10	MHz	10 MHz mode					
			DC	—	20	MHz	HS OSC mode (Comm/Ind)					
			DC	—	16	MHz	HS OSC mode (Ext)					
			DC	—	40	kHz	LP OSC mode					
		Oscillator Frequency ⁽¹⁾	DC	—	4.0	MHz	RC OSC mode					
			0.1	—	4.0	MHz	XT OSC mode					
			4.0	—	10	MHz	10 MHz mode					
			4.0	—	20	MHz	HS OSC mode (Comm/Ind)					
			4.0	—	16	MHz	HS OSC mode (Ext)					
			DC	_	40	kHz	LP osc mode					

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

13.2 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

PIC16CR54A-04E, 10E, 20E (Extended)			Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
D001	Vdd	Supply Voltage RC, XT and LP modes HS mode	3.25 4.5		6.0 5.5	V V		
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode	
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset	
D004	SVDD	VDD Rise Rate to ensure Power- on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset	
D010	IDD	Supply Current ⁽²⁾ RC ⁽³⁾ and XT modes HS mode HS mode		1.8 4.8 9.0	3.3 10 20	mA mA mA	Fosc = 4.0 MHz, VDD = 5.5V Fosc = 10 MHz, VDD = 5.5V Fosc = 16 MHz, VDD = 5.5V	
D020	IPD	Power-down Current ⁽²⁾		5.0 0.8	22 18	μΑ μΑ	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled	

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

- 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.



FIGURE 14-22: PORTA, B AND C IOL vs. VoL, VDD = 5 V





TABLE 15-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54A

AC Chara	cteristics	$\begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \ \ for \ commercial \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \ \ for \ industrial \\ -20^{\circ}C \leq TA \leq +85^{\circ}C \ \ for \ industrial - PIC16LV54A-02I \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \ \ for \ extended \end{array}$							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units			
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾		15	30**	ns			
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾		15	30**	ns			
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns			
13	TckF	CLKOUT fall time ⁽¹⁾		5.0	15**	ns			
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾		—	40**	ns			
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽¹⁾	0.25 TCY+30*	_	_	ns			
16	TckH2iol	Port in hold after CLKOUT ⁽¹⁾	0*	—	_	ns			
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽²⁾	—	_	100*	ns			
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD		_	ns			
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	_	ns			
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns			
21	TioF	Port output fall time ⁽²⁾		10	25**	ns			

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Please refer to Figure 15-1 for load conditions.



FIGURE 16-12: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 PF, 25°C)

FIGURE 16-13: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 PF, -40°C to +85°C)



Typical: statistical mean @ 25°C. Maximum: mean - 3 s (-40°C to 125°C) Minimum: mean

FIGURE 16-14: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 PF, 25°C)

FIGURE 16-15: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 PF, -40°C to +85°C)



TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics		$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for extended} \end{array} $						
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions	
2	Тсу	Instruction Cycle Time ⁽²⁾	—	4/Fosc				
3	TosL, TosH	Clock in (OSC1) Low or High	50*		_	ns	XT oscillator	
		Time	20*	—	_	ns	HS oscillator	
			2.0*	—	_	μS	LP oscillator	
4	TosR, TosF	Clock in (OSC1) Rise or Fall	-		25*	ns	XT oscillator	
		Time	—	—	25*	ns	HS oscillator	
			—	_	50*	ns	LP oscillator	

- * These parameters are characterized but not tested.
- † Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- **Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

18.0 DEVICE CHARACTERIZATION - PIC16LC54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.



FIGURE 18-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

TABLE 18-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Average Fosc @ 5V, 25°C			
20 pF	3.3K	5 MHz	± 27%		
	5K	3.8 MHz	± 21%		
	10K	2.2 MHz	± 21%		
	100K	262 kHz	± 31%		
100 pF	3.3K	1.63 MHz	± 13%		
	5K	1.2 MHz	± 13%		
	10K	684 kHz	± 18%		
	100K	71 kHz	± 25%		
300 pF	3.3K	660 kHz	± 10%		
	5.0K	484 kHz	± 14%		
	10K	267 kHz	± 15%		
	100K	29 kHz	± 19%		

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for VDD = 5V.

21.0 PACKAGING INFORMATION

21.1 Package Marketing Information

18-Lead PDIP



28-Lead Skinny PDIP (.300")



28-Lead PDIP (.600")



18-Lead SOIC



28-Lead SOIC



20-Lead SSOP



28-Lead SSOP





Example



Example



Example



Example



Example



Example



28-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









	Units	INCHES			MILLIMETERS*			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28		
Pitch	р		.026			0.65		
Overall Height	Α	.068	.073	.078	1.73	1.85	1.98	
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83	
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25	
Overall Width	E	.299	.309	.319	7.59	7.85	8.10	
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38	
Overall Length	D	.396	.402	.407	10.06	10.20	10.34	
Foot Length	L	.022	.030	.037	0.56	0.75	0.94	
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25	
Foot Angle	¢	0	4	8	0.00	101.60	203.20	
Lead Width	В	.010	.013	.015	0.25	0.32	0.38	
Mold Draft Angle Top	α	0	5	10	0	5	10	
Mold Draft Angle Bottom	β	0	5	10	0	5	10	

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-150 Drawing No. C04-073

28-Lead Ceramic Dual In-line with Window (JW) - 600 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES*		Ν	1ILLIMETERS	3
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.100			2.54	
Top to Seating Plane	А	.195	.210	.225	4.95	5.33	5.72
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.038	.060	0.38	0.95	1.52
Shoulder to Shoulder Width	Е	.595	.600	.625	15.11	15.24	15.88
Ceramic Pkg. Width	E1	.514	.520	.526	13.06	13.21	13.36
Overall Length	D	1.430	1.460	1.490	36.32	37.08	37.85
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.058	.065	1.27	1.46	1.65
Lower Lead Width	В	.016	.020	.023	0.41	0.51	0.58
Overall Row Spacing §	eB	.610	.660	.710	15.49	16.76	18.03
Window Diameter	W	.270	.280	.290	6.86	7.11	7.37

Sontolling Parameter
 Significant Characteristic
 JEDEC Equivalent: MO-103
 Drawing No. C04-013