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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57t-hsi-so

5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the $\overline{\text{MCLR}}/\text{VPP}$ pin to VDD . A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is RESET. The DRT timer begins counting once it detects $\overline{\text{MCLR}}$ to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where $\overline{\text{MCLR}}$ is not tied to VDD is shown in Figure 5-3. VDD is allowed to rise and stabilize before bringing $\overline{\text{MCLR}}$ high. The chip will actually come out of reset T_{DRT} msec after $\overline{\text{MCLR}}$ goes high.

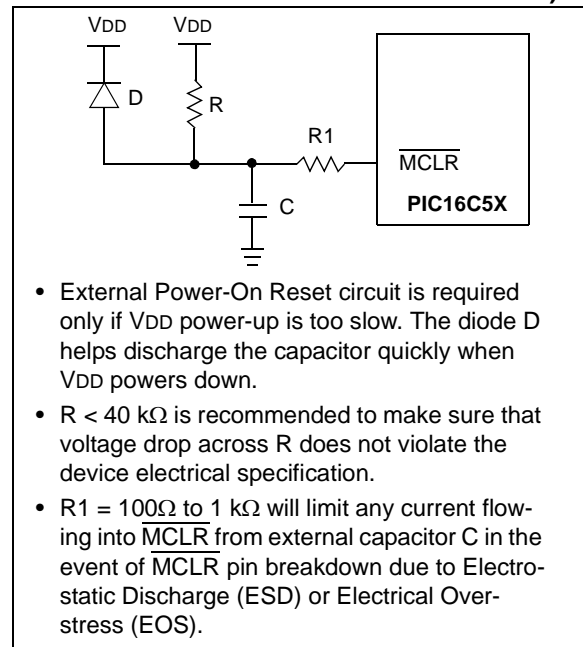
In Figure 5-4, the on-chip Power-On Reset feature is being used ($\overline{\text{MCLR}}$ and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the $\overline{\text{MCLR}}/\text{VPP}$ pin, and when the $\overline{\text{MCLR}}/\text{VPP}$ pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the $\text{V}_{\text{DD}}(\text{min})$ value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

Note: When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the [Embedded Control Handbook](#).

The POR circuit does not produce an internal RESET when VDD declines.

FIGURE 5-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



8.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

8.1.1 EXTERNAL CLOCK SYNCHRONIZATION

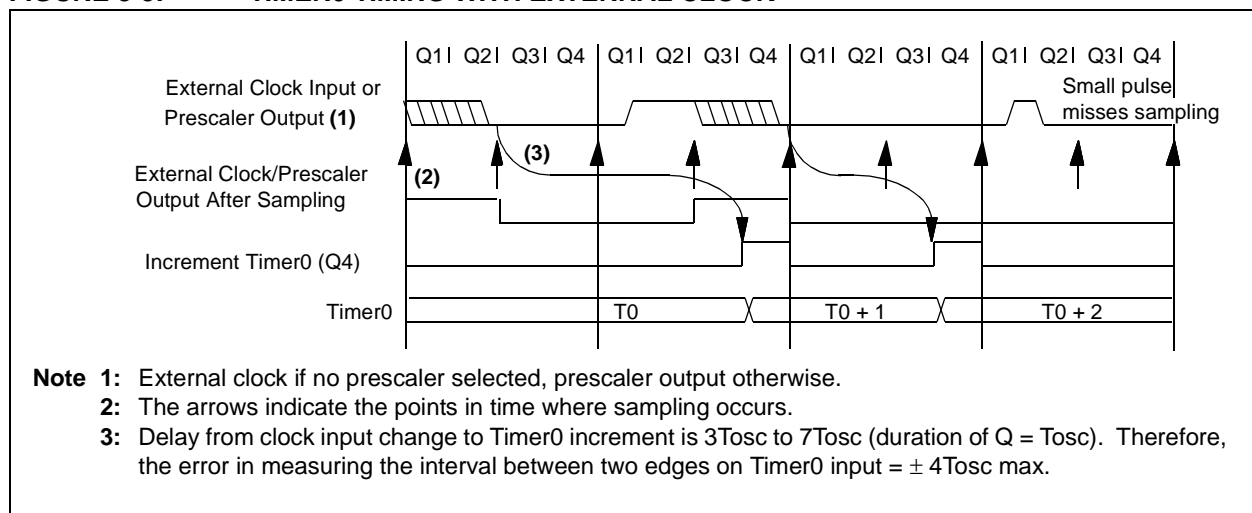
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 8-5). Therefore, it is necessary for T0CKI to be high for at least $2T_{osc}$ (and a small RC delay of 20 ns) and low for at least $2T_{osc}$ (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least $4T_{osc}$ (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

8.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 8-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 8-5: TIMER0 TIMING WITH EXTERNAL CLOCK



PIC16C5X

COMF Complement f

Syntax: [*label*] COMF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) \rightarrow (dest)$

Status Affected: Z

Encoding:

0010	01df	ffff
------	------	------

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: COMF REG1, 0

Before Instruction

REG1 = 0x13

After Instruction

REG1 = 0x13

W = 0xEC

DECFSZ Decrement f

Syntax: [*label*] DECFSZ f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) - 1 \rightarrow (dest)$

Status Affected: Z

Encoding:

0000	11df	ffff
------	------	------

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: DECFSZ CNT, 1

Before Instruction

CNT = 0x01

Z = 0

After Instruction

CNT = 0x00

Z = 1

DECFSZ Decrement f, Skip if 0

Syntax: [*label*] DECFSZ f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) - 1 \rightarrow d$; skip if result = 0

Status Affected: None

Encoding:

0010	11df	ffff
------	------	------

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
 If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example:

HERE	DECFSZ	CNT, 1
	GOTO	LOOP
CONTINUE	•	
	•	
	•	

Before Instruction

PC = address (HERE)

After Instruction

CNT = CNT - 1;

if CNT = 0,

PC = address (CONTINUE);

if CNT \neq 0,

PC = address (HERE+1)

PIC16C5X

IORLW Inclusive OR literal with W

Syntax: [*label*] IORLW *k*
Operands: $0 \leq k \leq 255$
Operation: (W) .OR. (*k*) \rightarrow (W)
Status Affected: Z
Encoding:

1101	kkkk	kkkk
------	------	------

Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.
Words: 1
Cycles: 1
Example: IORLW 0x35

Before Instruction
W = 0x9A
After Instruction
W = 0xBF
Z = 0

IORWF Inclusive OR W with f

Syntax: [*label*] IORWF *f*,*d*
Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
Operation: (W).OR. (*f*) \rightarrow (*dest*)
Status Affected: Z
Encoding:

0001	00df	ffff
------	------	------

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
Words: 1
Cycles: 1
Example: IORWF RESULT, 0

Before Instruction
RESULT = 0x13
W = 0x91
After Instruction
RESULT = 0x13
W = 0x93
Z = 0

MOVF Move f

Syntax: [*label*] MOVF *f*,*d*
Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
Operation: (*f*) \rightarrow (*dest*)
Status Affected: Z
Encoding:

0010	00df	ffff
------	------	------

Description: The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.
Words: 1
Cycles: 1
Example: MOVF FSR, 0

After Instruction
W = value in FSR register

MOVLW Move Literal to W

Syntax: [*label*] MOVLW *k*
Operands: $0 \leq k \leq 255$
Operation: *k* \rightarrow (W)
Status Affected: None
Encoding:

1100	kkkk	kkkk
------	------	------

Description: The eight bit literal 'k' is loaded into the W register.
Words: 1
Cycles: 1
Example: MOVLW 0x5A

After Instruction
W = 0x5A

13.3 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	V _{IL}	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	V _{SS} V _{SS} V _{SS} V _{SS} V _{SS}	— — — — —	0.2 V _{DD} 0.15 V _{DD} 0.15 V _{DD} 0.15 V _{DD} 0.15 V _{DD}	V V V V V	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes
D040	V _{IH}	Input High Voltage I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	2.0 0.6 V _{DD} 0.85 V _{DD} 0.85 V _{DD} 0.85 V _{DD} 0.85 V _{DD}	— — — — — —	V _{DD} V _{DD} V _{DD} V _{DD} V _{DD} V _{DD}	V V V V V V	V _{DD} = 3.0V to 5.5V ⁽⁴⁾ Full V _{DD} range ⁽⁴⁾ RC mode only ⁽³⁾ XT, HS and LP modes
D050	V _{HYS}	Hysteresis of Schmitt Trigger inputs	0.15 V _{DD} *	—	—	V	
D060	I _{IL}	Input Leakage Current^(1,2) I/O ports MCLR MCLR T0CKI OSC1	–1.0 –5.0 — –3.0 –3.0	— — 0.5 0.5 0.5	+1.0 — +5.0 +3.0 +3.0	μA μA μA μA μA	For V_{DD} ≤ 5.5V: V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance V _{PIN} = V _{SS} + 0.25V V _{PIN} = V _{DD} V _{SS} ≤ V _{PIN} ≤ V _{DD} V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT, HS and LP modes
D080	V _{OL}	Output Low Voltage I/O ports OSC2/CLKOUT	— —	— —	0.5 0.5	V V	I _{OL} = 10 mA, V _{DD} = 6.0V I _{OL} = 1.9 mA, V _{DD} = 6.0V, RC mode only
D090	V _{OH}	Output High Voltage⁽²⁾ I/O ports OSC2/CLKOUT	V _{DD} – 0.5 V _{DD} – 0.5	— —	— —	V V	I _{OH} = –4.0 mA, V _{DD} = 6.0V I _{OH} = –0.8 mA, V _{DD} = 6.0V, RC mode only

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

FIGURE 13-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR54A

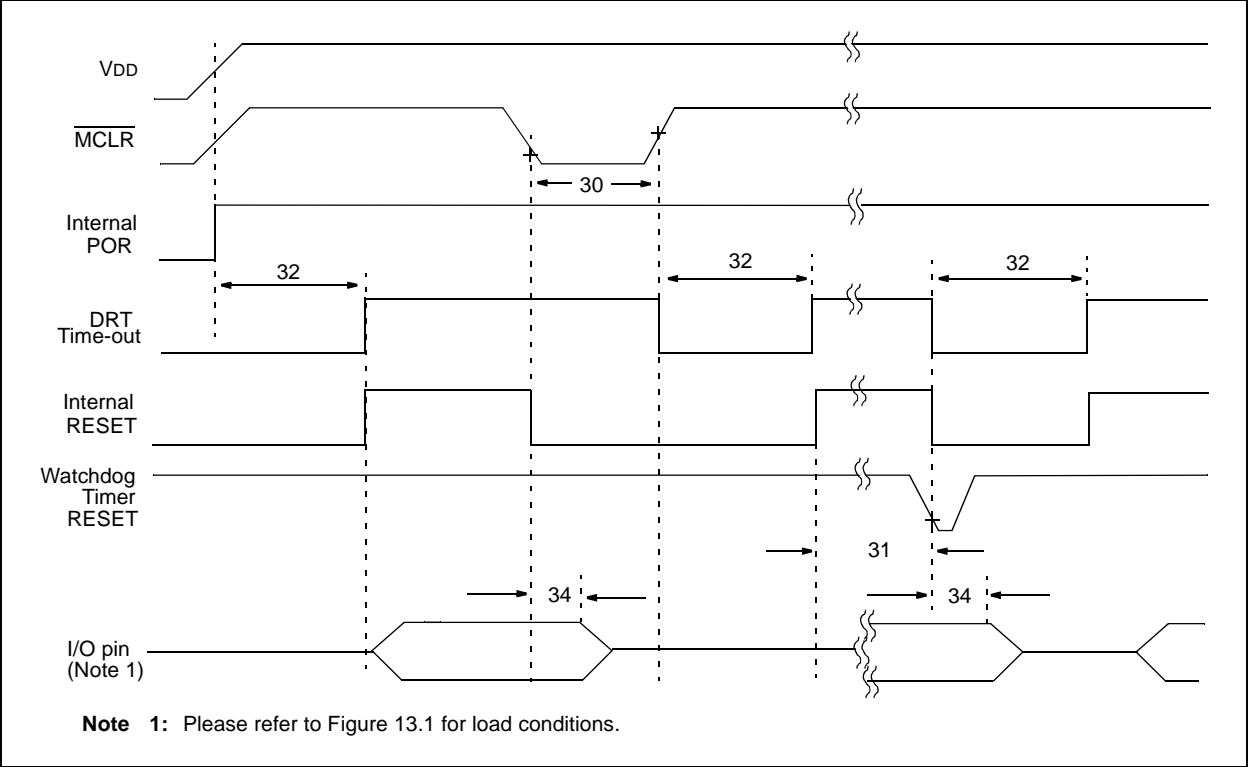


TABLE 13-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR54A

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics		Operating Temperature					
		0°C ≤ TA ≤ +70°C for commercial					
		-40°C ≤ TA ≤ +85°C for industrial					
		-40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	1.0*	—	—	μs	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7.0*	18*	40*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	7.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	TioZ	I/O Hi-impedance from MCLR Low	—	—	1.0*	μs	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 14-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

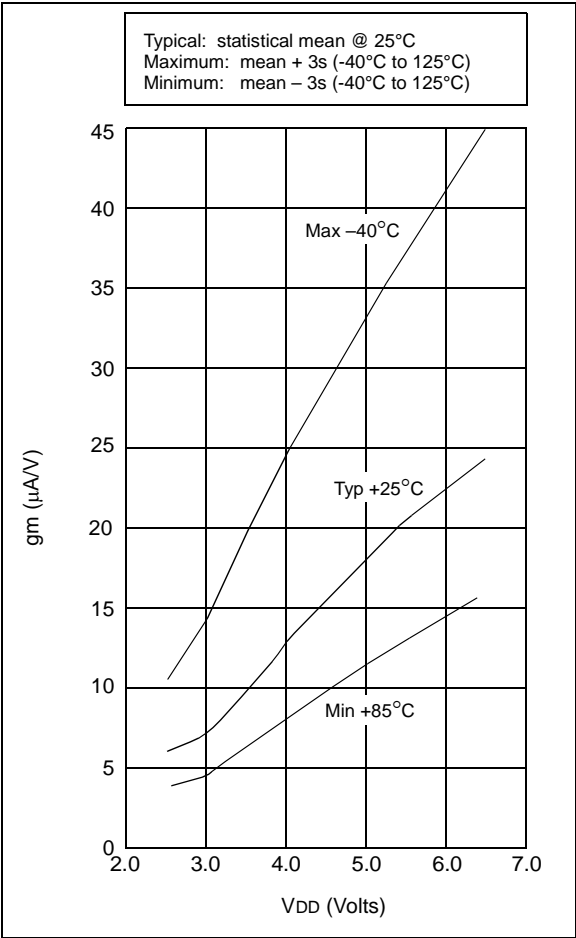


FIGURE 14-18: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

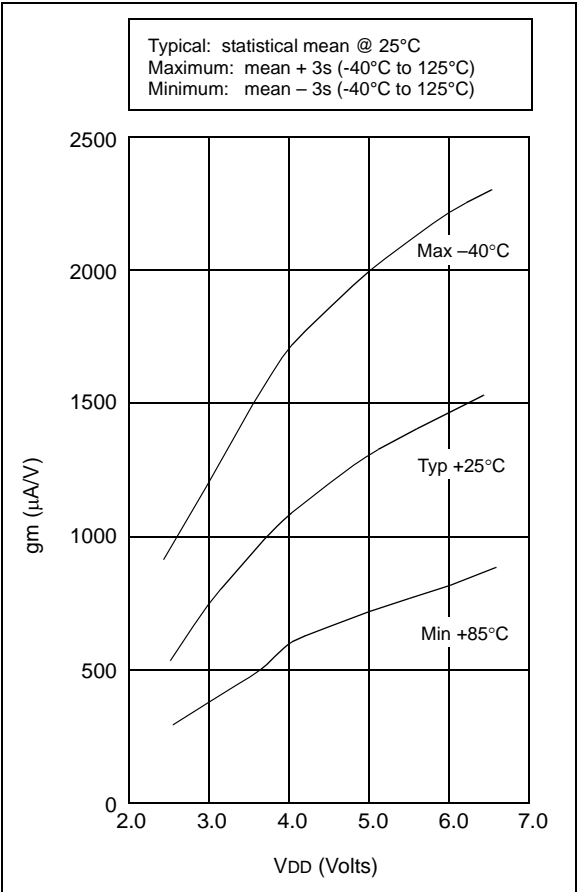


FIGURE 14-21: PORTA, B AND C IoL vs. VOL, VDD = 3 V

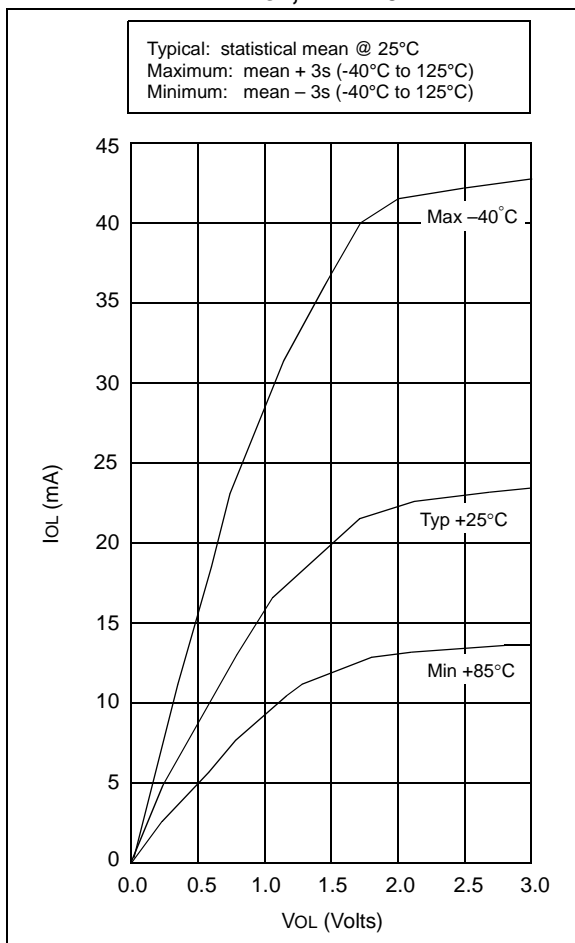
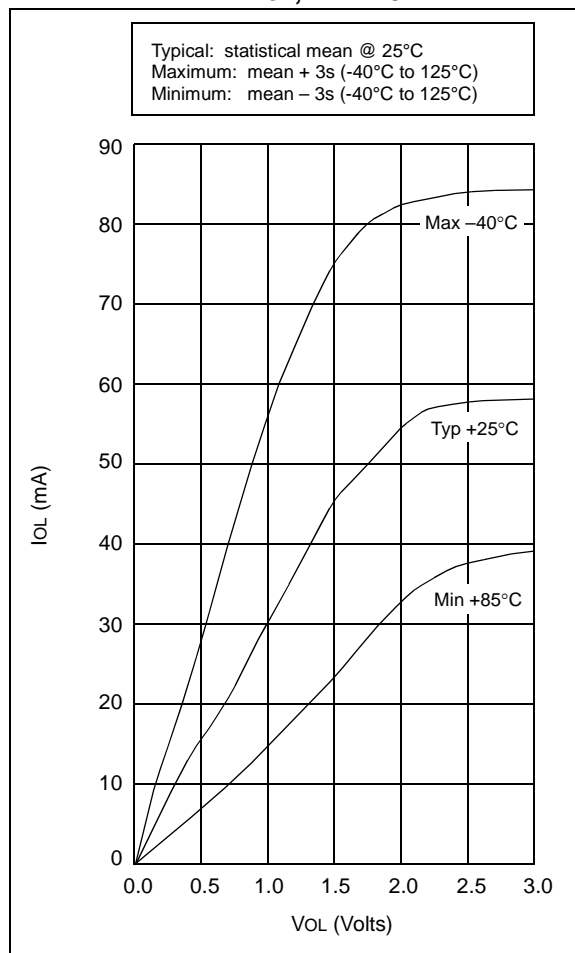


FIGURE 14-22: PORTA, B AND C IoL vs. VOL, VDD = 5 V



PIC16C5X

15.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended) PIC16LC54A-04E (Extended)

PIC16LC54A-04E (Extended)		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
PIC16C54A-04E, 10E, 20E (Extended)		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage					
		PIC16LC54A	3.0 2.5	— —	6.25 6.25	V V	XT and RC modes LP mode
D001A		PIC16C54A	3.5 4.5	— —	5.5 5.5	V V	RC and XT modes HS mode
D002	VDR	RAM Data Retention Voltage⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current⁽²⁾					
		PIC16LC54A	—	0.5	25	mA	FOSC = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes
			—	11	27	μA	FOSC = 32 kHz, VDD = 2.5V, LP mode, Commercial
			—	11	35	μA	FOSC = 32 kHz, VDD = 2.5V, LP mode, Industrial
			—	11	37	μA	FOSC = 32 kHz, VDD = 2.5V, LP mode, Extended
D010A		PIC16C54A	—	1.8	3.3	mA	FOSC = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes
			—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V, HS mode
			—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V, HS mode

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

Note 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{EXT}$ (mA) with REXT in kΩ.

PIC16C5X

FIGURE 15-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A

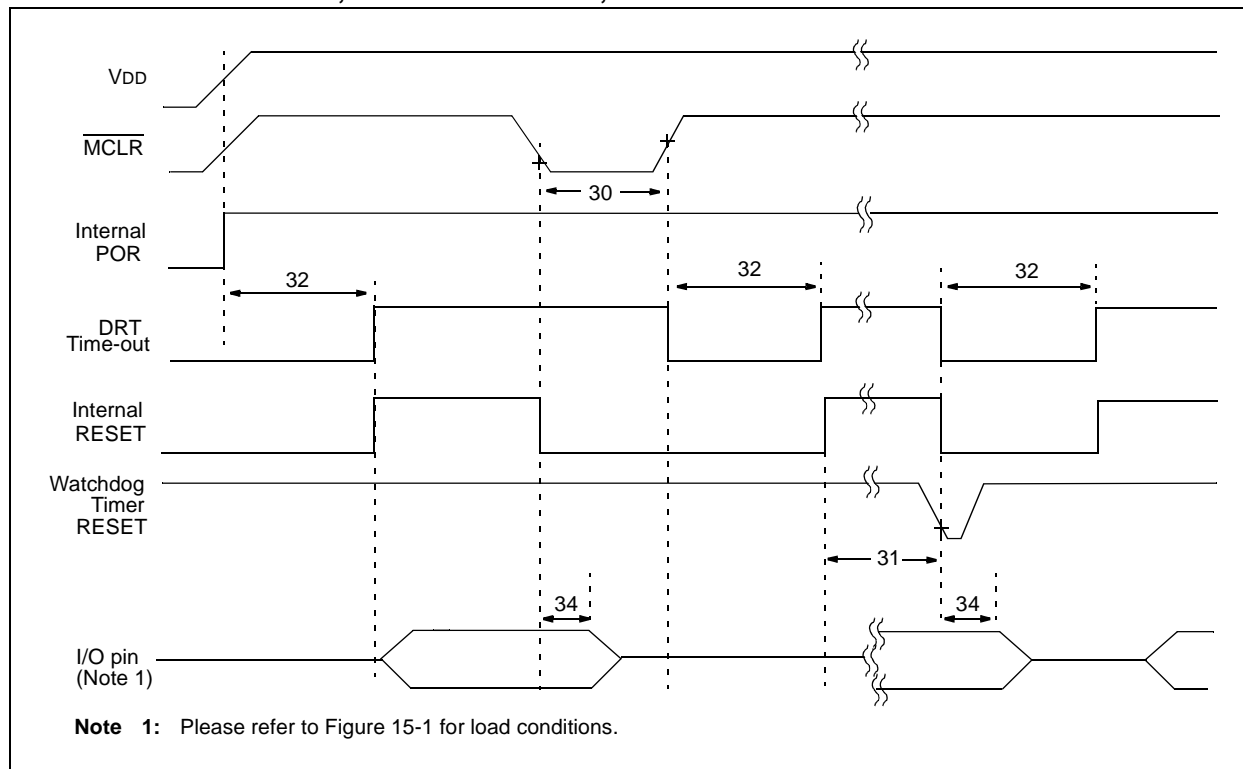


TABLE 15-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A

Standard Operating Conditions (unless otherwise specified)							
Operating Temperature							
AC Characteristics							
0°C ≤ TA ≤ +70°C for commercial							
-40°C ≤ TA ≤ +85°C for industrial							
-20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I							
-40°C ≤ TA ≤ +125°C for extended							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	100* 1	— —	— —	ns μs	VDD = 5.0V VDD = 5.0V (PIC16LV54A only)
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	TioZ	I/O Hi-impedance from MCLR Low	— —	— —	100* 1μs	ns —	(PIC16LV54A only)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

16.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum” or “minimum” represents (mean + 3 σ) or (mean – 3 σ) respectively, where σ is a standard deviation, over the whole temperature range.

FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

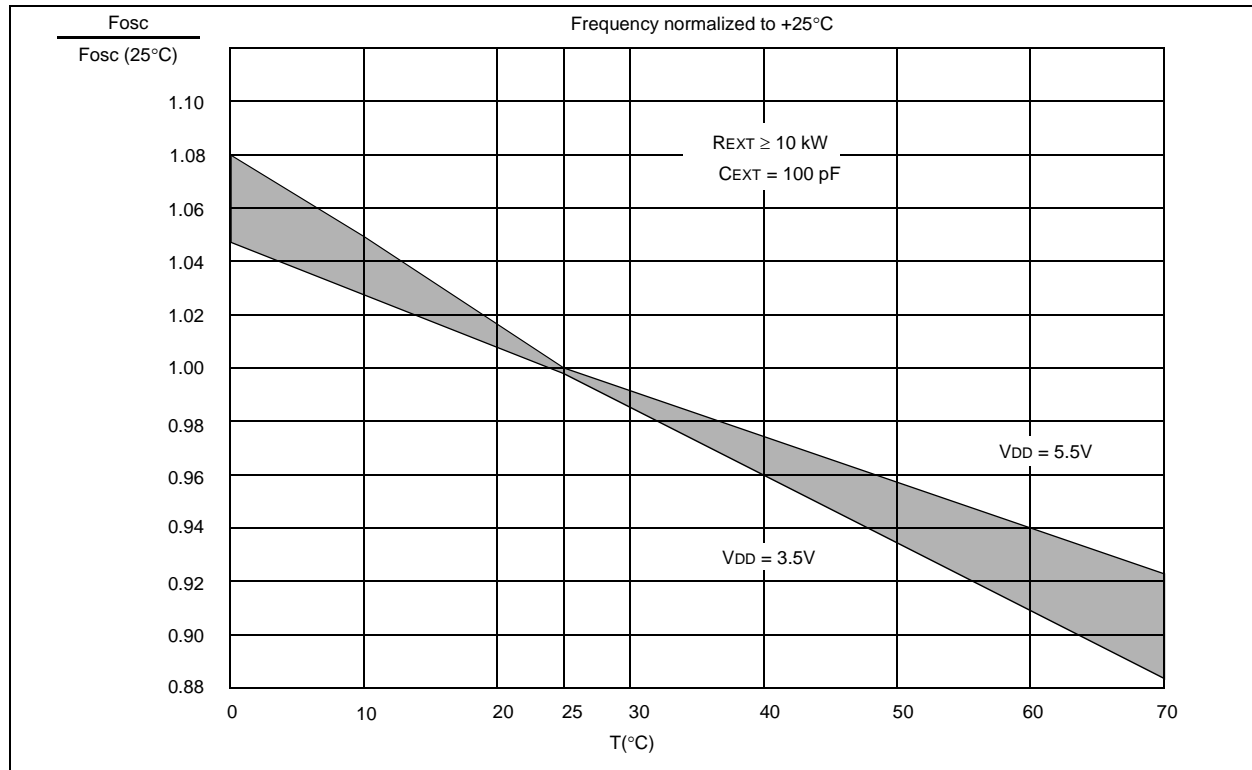


TABLE 16-1: RC OSCILLATOR FREQUENCIES

C_{EXT}	R_{EXT}	Average F_{osc} @ 5 V, 25°C	
20 pF	3.3K	5 MHz	± 27%
	5K	3.8 MHz	± 21%
	10K	2.2 MHz	± 21%
	100K	262 kHz	± 31%
100 pF	3.3K	1.6 MHz	± 13%
	5K	1.2 MHz	± 13%
	10K	684 kHz	± 18%
	100K	71 kHz	± 25%
300 pF	3.3K	660 kHz	± 10%
	5.0K	484 kHz	± 14%
	10K	267 kHz	± 15%
	100K	29 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for $V_{DD} = 5\text{V}$.

FIGURE 16-16: WDT TIMER TIME-OUT PERIOD vs. VDD⁽¹⁾

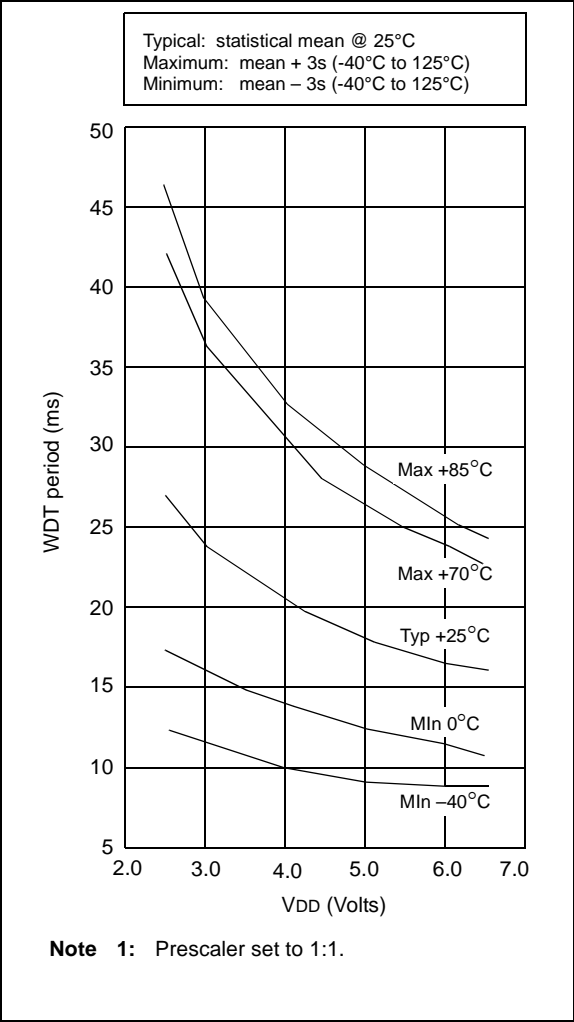


FIGURE 16-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD

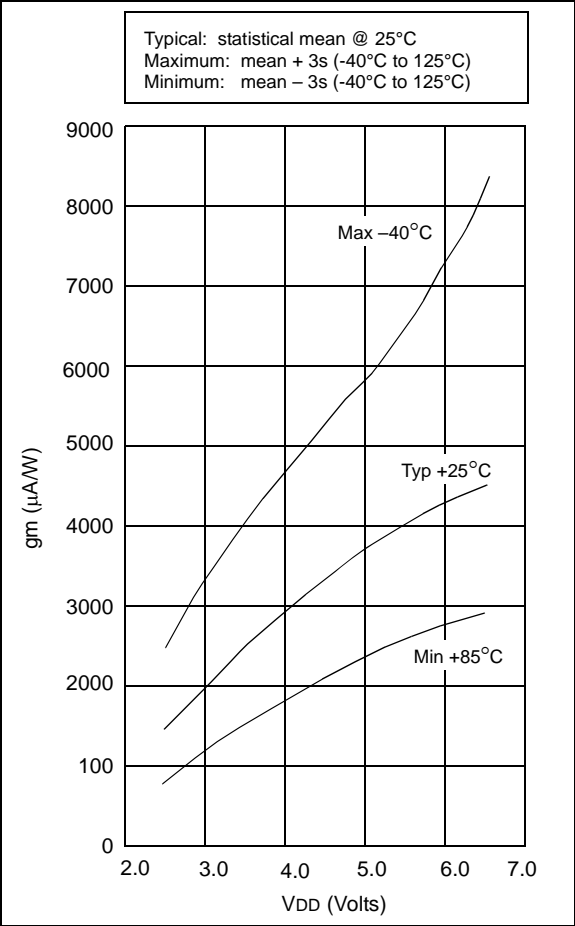


TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
2	Tcy	Instruction Cycle Time ⁽²⁾	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

PIC16C5X

FIGURE 17-7: CLKOUT AND I/O TIMING - PIC16C5X, PIC16CR5X

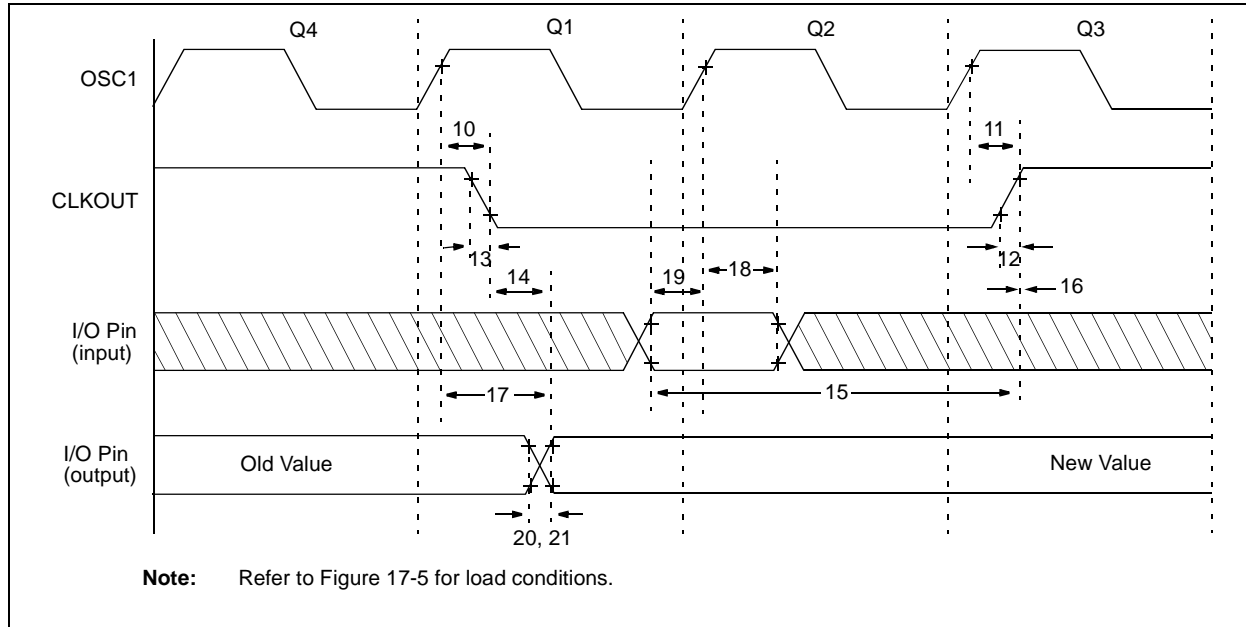


TABLE 17-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature				
		0°C ≤ TA ≤ +70°C for commercial				
		-40°C ≤ TA ≤ +85°C for industrial				
		-40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽¹⁾	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ ⁽¹⁾	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽²⁾	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽²⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

2: Refer to Figure 17-5 for load conditions.

FIGURE 18-10: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (IN XT, HS AND LP MODES) vs. VDD

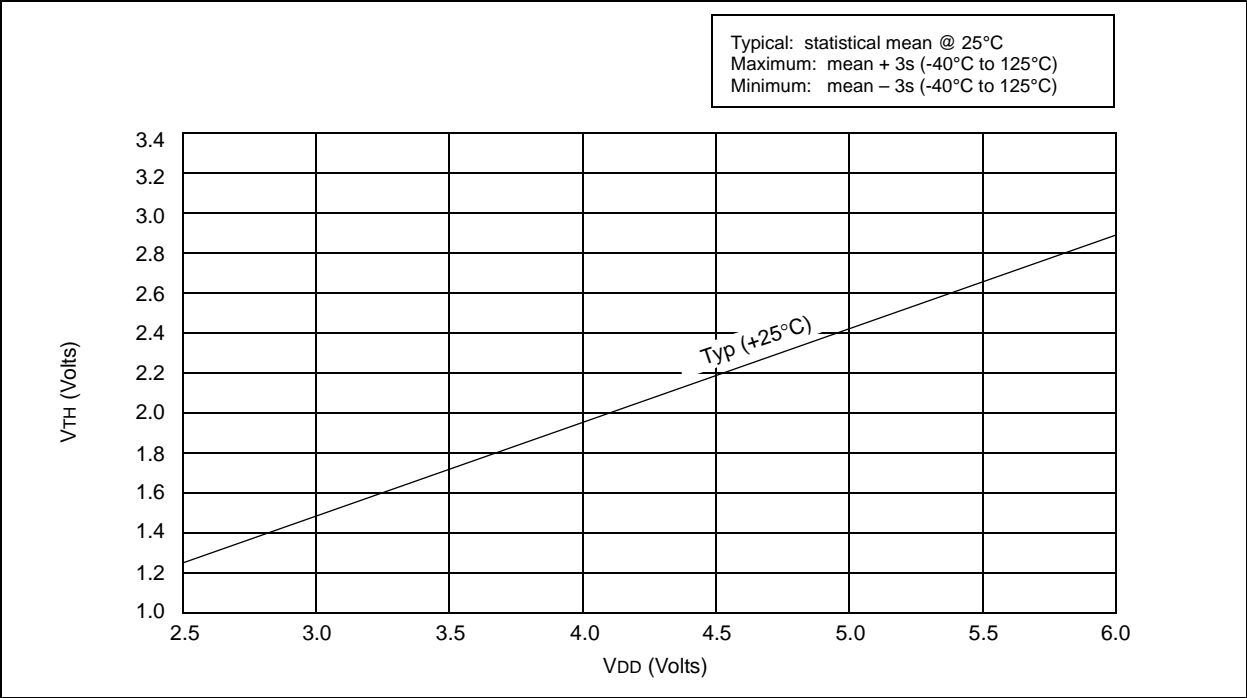


FIGURE 18-11: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, 25°C)

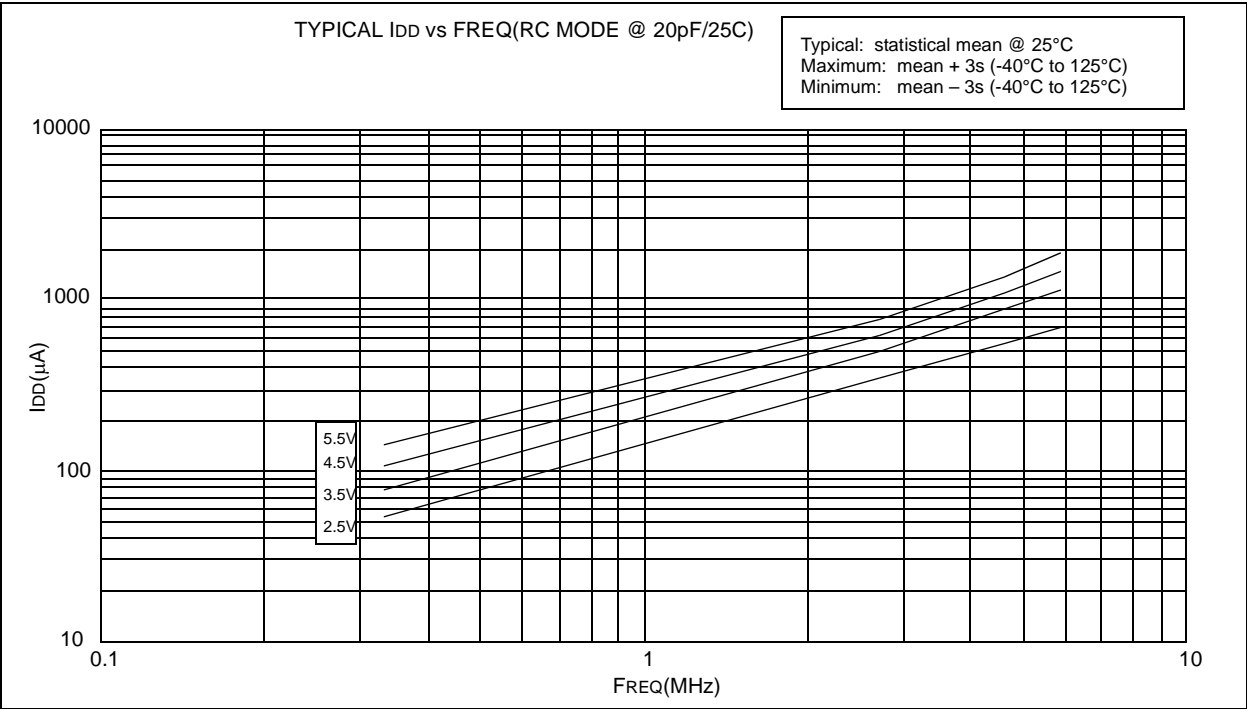


FIGURE 18-12: TYPICAL I_{DD} vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, 25°C)

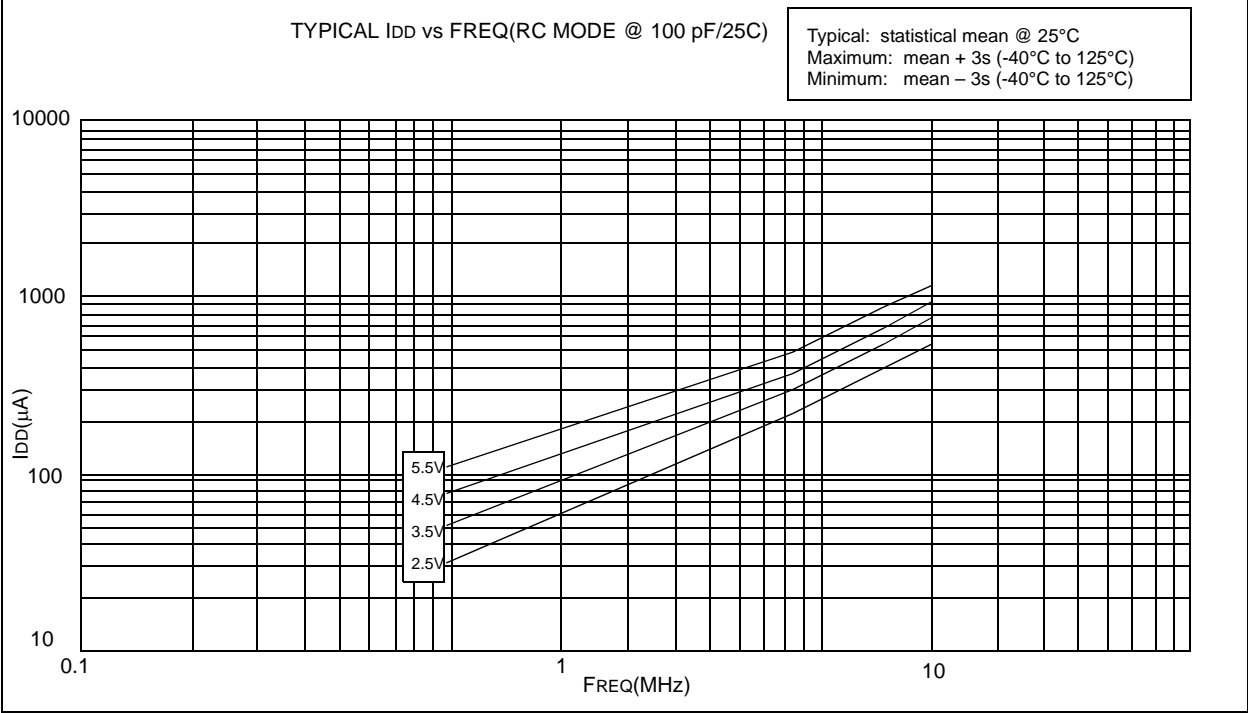
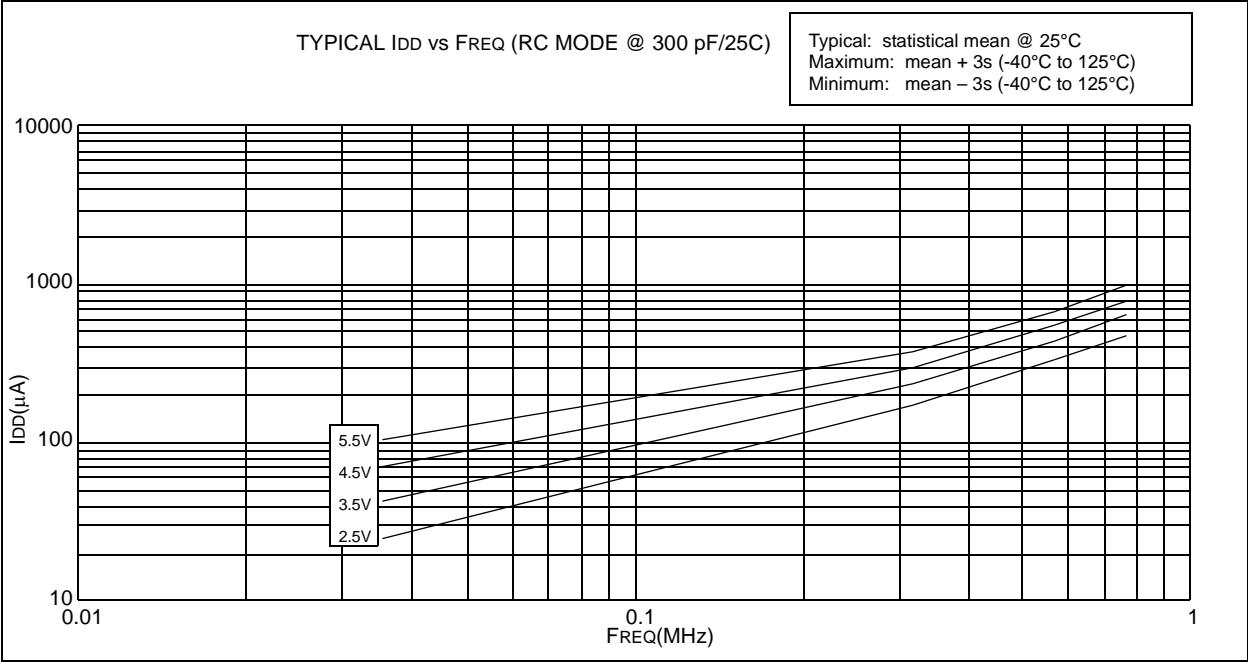


FIGURE 18-13: TYPICAL I_{DD} vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, 25°C)



PIC16C5X

**FIGURE 18-18: PORTA, B AND C IoL vs.
VOL, VDD = 5 V**

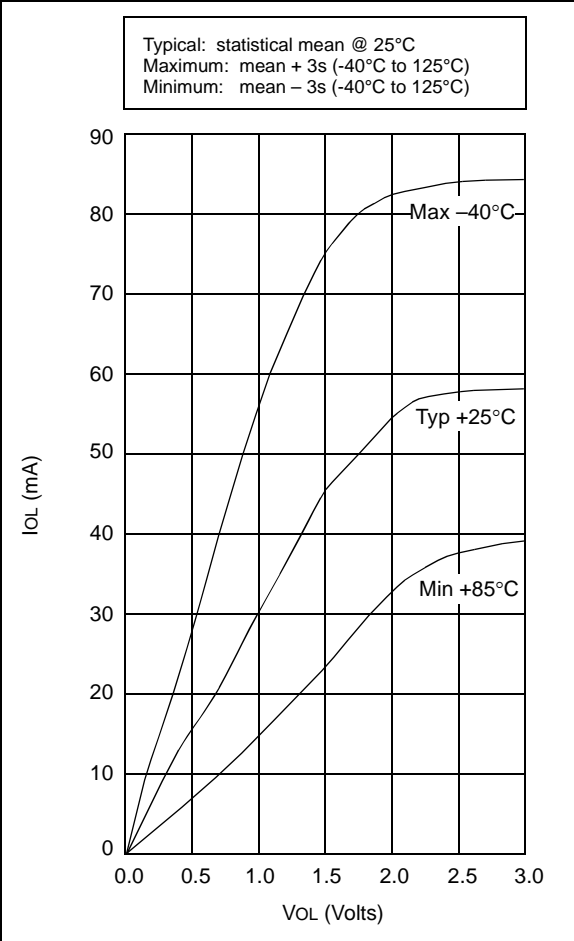


TABLE 18-2: INPUT CAPACITANCE

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
MCLR	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

PIC16C5X

FIGURE 19-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X-40

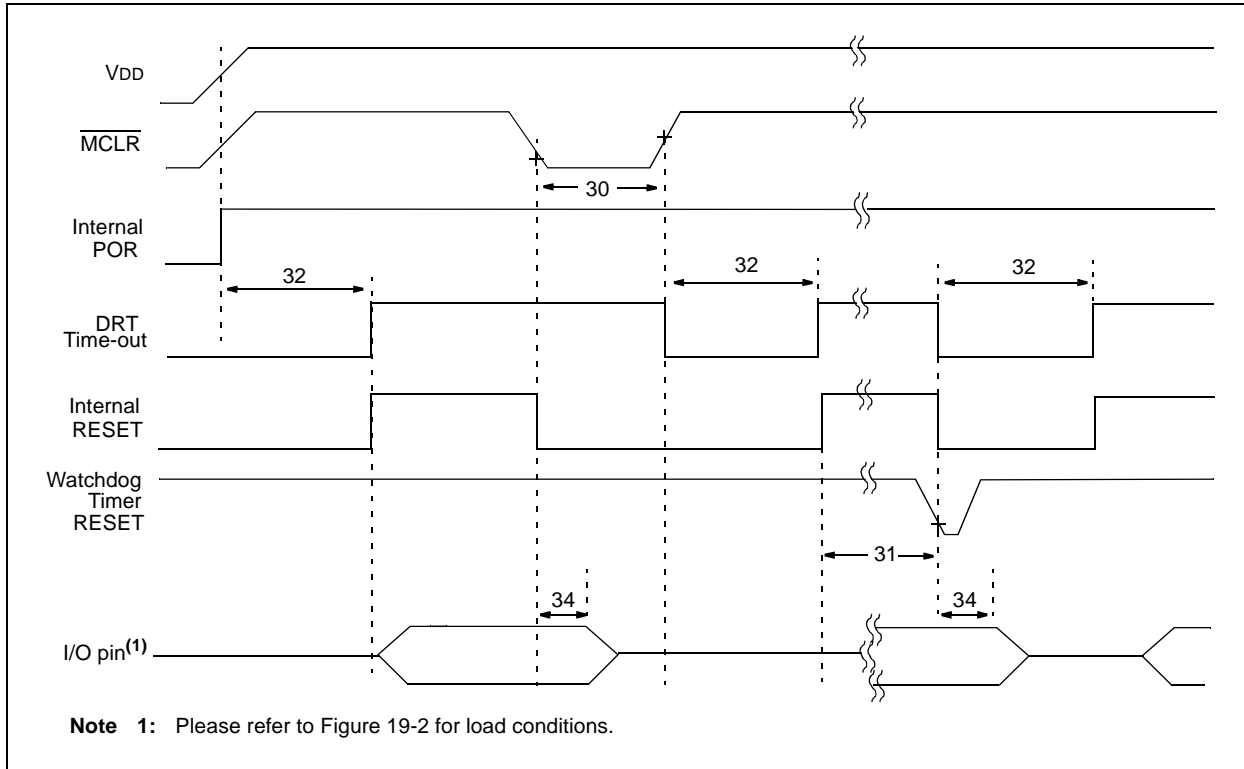


TABLE 19-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X-40

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics							
Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial)							
Operating Voltage VDD range is described in Section 19.1.							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	1000*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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