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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c57t-rc-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 1-1: PIC16C5X FAMILY OF DEVICES

Features	PIC16C54	PIC16CR54	PIC16C55	PIC16C56	PIC16CR56	
Maximum Operation Frequency	40 MHz	20 MHz	40 MHz	40 MHz	20 MHz	
EPROM Program Memory (x12 words)	512	—	512	1K	—	
ROM Program Memory (x12 words)	—	512	—	—	1K	
RAM Data Memory (bytes)	25	25	24	25	25	
Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	
I/O Pins	12	12	20	12	12	
Number of Instructions	33	33	33	33	33	
Packages18-pin DIP, SOIC;18-pin DIP, SOIC;28-pin DIP, SOIC;18-pin DIP, SOIC;18-						
All PIC [®] Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.						

PIC16C58 Features **PIC16C57** PIC16CR57 PIC16CR58 Maximum Operation Frequency 20 MHz 40 MHz 40 MHz 20 MHz EPROM Program Memory (x12 words) 2K 2K ____ _ ROM Program Memory (x12 words) 2K 2K _ _ RAM Data Memory (bytes) 72 72 73 73 Timer Module(s) TMR0 TMR0 TMR0 TMR0 I/O Pins 20 20 12 12 Number of Instructions 33 33 33 33 28-pin DIP, SOIC; 28-pin DIP, SOIC; 18-pin DIP, SOIC; 18-pin DIP, SOIC; Packages 28-pin SSOP 28-pin SSOP 20-pin SSOP 20-pin SSOP All PIC® Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.

2.0 PIC16C5X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC16C5X Product Identification System at the back of this data sheet to specify the correct part number.

For the PIC16C5X family of devices, there are four device types, as indicated in the device number:

- 1. **C**, as in PIC16**C**54C. These devices have EPROM program memory and operate over the standard voltage range.
- LC, as in PIC16LC54A. These devices have EPROM program memory and operate over an extended voltage range.
- 3. **CR**, as in PIC16**CR**54A. These devices have ROM program memory and operate over the standard voltage range.
- 4. LCR, as in PIC16LCR54A. These devices have ROM program memory and operate over an extended voltage range.

2.1 UV Erasable Devices (EPROM)

The UV erasable versions offered in CERDIP packages, are optimal for prototype development and pilot programs.

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's

PICSTART[®] Plus⁽¹⁾ and PRO MATE[®] programmers both support programming of the PIC16C5X. Third party programmers also are available. Refer to the Third Party Guide (DS00104) for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates, or small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

Note 1: PIC16LC54C and PIC16C54A devices require OSC2 not to be connected while programming with PICSTART[®] Plus programmer.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTPSM) Devices

Microchip offers the unique programming service where a few user defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, giving the customer a low cost option for high volume, mature products.

TABLE 5-3: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-On Reset	MCLR or WDT Reset
W	N/A	xxxx xxxx	uuuu uuuu
TRIS	N/A	1111 1111	1111 1111
OPTION	N/A	11 1111	11 1111
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	XXXX XXXX	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000q quuu
FSR ⁽¹⁾	04h	1xxx xxxx	luuu uuuu
PORTA	05h	xxxx	uuuu
PORTB	06h	XXXX XXXX	uuuu uuuu
PORTC ⁽²⁾	07h	XXXX XXXX	uuuu uuuu
General Purpose Register Files	07-7Fh	xxxx xxxx	սսսս սսսս

Legend: x = unknown u = unchanged - = unimplemented, read as '0'<math>q = see tables in Table 5-1 for possible values.

- Note 1: These values are valid for PIC16C57/CR57/CR58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for MCLR and WDT Reset, the value is 111u uuuu.
 - **2:** General purpose register file on PIC16C54/CR54/C56/CR56/C58/CR58.

FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



NOTES:

7.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., MOVF PORTB, W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

7.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used (RA<3:0>). Bits 7-4 are unimplemented and read as '0's.

7.2 PORTB

PORTB is an 8-bit I/O Register (PORTB<7:0>).

7.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16CR56, PIC16CR56, PIC16CS8 and PIC16CR58.

7.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the TRIS f instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

Note:	A read of the ports reads the pins, not the
	output data latches. That is, if an output
	driver on a pin is enabled and driven high,
	but the external system is holding it low, a
	read of the port will indicate that the pin is
	low.

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

TABLE 7-1:	SUMMARY O	F PORT	REGISTERS
			LOIOI LIVO

Value on Value on Bit 4 Bit 3 Bit 1 Bit 0 MCLR and Address Name Bit 7 Bit 6 Bit 5 Bit 2 Power-On Reset WDT Reset TRIS N/A I/O Control Registers (TRISA, TRISB, TRISC) 1111 1111 1111 1111 05h PORTA RA3 RA2 RA1 RA0 _ _ _ _ xxxx _ _ _ _ uuuu PORTB 06h RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0 XXXX XXXX uuuu uuuu 07h PORTC RC7 RC6 RC5 RC4 RC3 RC2 RC1 RC0 XXXX XXXX uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'

7.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 7-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

FIGURE 7-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



8.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

8.1.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 8-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

8.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 8-5 shows the delay from the external clock edge to the timer incrementing.



the error in measuring the interval between two edges on Timer0 input = ± 4 Tosc max.

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9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of realtime applications. The PIC16C5X family of microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator Selection (Section 4.0)
- RESET (Section 5.0)
- Power-On Reset (Section 5.1)
- Device Reset Timer (Section 5.2)
- Watchdog Timer (WDT) (Section 9.2)
- SLEEP (Section 9.3)
- Code protection (Section 9.4)
- ID locations (Section 9.5)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in RESET until the crystal oscillator is stable. With this timer on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake up from SLEEP through external RESET or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

BSF	Bit Set f			
Syntax:	[label]	BSF f,b		
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ 0 \leq b \leq 7 \end{array}$	$\begin{array}{l} 0 \leq f \leq 31 \\ 0 \leq b \leq 7 \end{array}$		
Operation:	$1 \rightarrow (f < b)$	>)		
Status Affected:	None			
Encoding:	0101	bbbf	ffff	
Description:	Bit 'b' in r	register 'f'	is set.	
Words:	1			
Cycles:	1			
Example:	BSF	FLAG_RE	G, 7	
Before Instruction FLAG_REG = 0x0A After Instruction				
$FLAG_REG = 0x8A$				

BTFSC	Bit Test	f, Skip if	Clear	
Syntax:	[label]	BTFSC	f,b	
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ 0 \leq b \leq 7 \end{array}$			
Operation:	skip if (f) = 0		
Status Affected:	None			
Encoding:	0110	bbbf	ffff	
Description:	If bit 'b' in register 'f' is 0 then the next instruction is skipped. If bit 'b' is 0 then the next instruc- tion fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a 2-cycle instruction			
Words:	1			
Cycles:	1(2)			
Example:	HERE FALSE TRUE	BTFSC GOTO • •	FLAG,1 PROCESS	S_CODE
Before Instru	ction			
PC After Instructi if FLAG< PC if FLAG< PC	= (1> = (1> = (1> = =	address 0, address (1, address (1	(HERE) TRUE); FALSE)	

BTFSS	Bit Test f, Skip if Set		
Syntax:	[label] BTFSS f,b		
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ 0 \leq b < 7 \end{array}$		
Operation:	skip if (f) = 1		
Status Affected:	None		
Encoding:	0111 bbbf ffff		
Description:	If bit 'b' in register 'f' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruc- tion fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a 2-cycle instruction.	-	
Words:	1		
Cycles:	1(2)		
Example:	HERE BTFSS FLAG,1 FALSE GOTO PROCESS_CODI TRUE • •	Ξ	
Before Instr	ruction		
PC	= address (HERE)		
After Instruction			
	< i > = 0, = address (FALSE)		
if FLAG<	<1> = 1.		
PC	= address (TRUE)		

11.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB[®] IDE Software
- Assemblers/Compilers/Linkers
 - MPASM[™] Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK™ Object Linker/
 - MPLIB[™] Object Librarian
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - ICEPIC[™] In-Circuit Emulator
- In-Circuit Debugger
- MPLAB ICD
- Device Programmers
 - PRO MATE[®] II Universal Device Programmer
- PICSTART[®] Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
 - PICDEM[™]1 Demonstration Board
 - PICDEM 2 Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 17 Demonstration Board
 - KEELOQ[®] Demonstration Board

11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows[®]-based application that contains:

- An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file
 - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

11.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display. NOTES:

13.0 ELECTRICAL CHARACTERISTICS - PIC16CR54A

Absolute Maximum Ratings(†)

Ambient Temperature under bias	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on MCLR with respect to Vss ⁽¹⁾	0 to +14V
Voltage on all other pins with respect to Vss	–0.6V to (VDD + 0.6V)
Total power dissipation ⁽²⁾	
Max. current out of Vss pin	150 mA
Max. current into Vod pin	50 mA
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, Iık (VI < 0 or VI > VDD)	±20 mA
Output clamp current, IOK (V0 < 0 or V0 > VDD)	±20 mA
Max. output current sunk by any I/O pin	25 mA
Max. output current sourced by any I/O pin	20 mA
Max. output current sourced by a single I/O port (PORTA or B)	40 mA
Max. output current sunk by a single I/O port (PORTA or B)	50 mA

- **Note 1:** Voltage spikes below Vss at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a low level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to Vss.
 - **2:** Power Dissipation is calculated as follows: PDIS = VDD x {IDD \sum IOH} + \sum {(VDD-VOH) x IOH} + \sum (VOL x IOL)

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 14-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED



FIGURE 14-7: T

TYPICAL IPD vs. VDD, WATCHDOG ENABLED



FIGURE 14-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED



IPD, with WDT enabled, has two components: The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At -40° C, the latter dominates explaining the apparently anomalous behavior.









TABLE 14-2: INPUT CAPACITANCE FOR PIC16C54/56

Dia	Typical Capa	acitance (pF)
FIII	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
MCLR	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
TOCKI	3.2	2.8

All capacitance values are typical at 25° C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

TABLE 14-3:	INPUT CAPACITANCE FOR
	PIC16C55/57

	Typical Capa	acitance (pF)
Pin	28L PDIP (600 mil)	28L SOIC
RA port	5.2	4.8
RB port	5.6	4.7
RC port	5.0	4.1
MCLR	17.0	17.0
OSC1	6.6	3.5
OSC2/CLKOUT	4.6	3.5
TOCKI	4.5	3.5

All capacitance values are typical at 25° C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.



FIGURE 18-17: PORTA, B AND C IOL vs. Vol, VDD = 3 V











PIC16C5X

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