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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 12 |
| Program Memory Size | 768B (512 x 12) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 25 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 6.25V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 20-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lc54a-04i-ss |

## 2.0 PIC16C5X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC16C5X Product Identification System at the back of this data sheet to specify the correct part number.

For the PIC16C5X family of devices, there are four device types, as indicated in the device number:

1. **C**, as in PIC16**C**54C. These devices have EPROM program memory and operate over the standard voltage range.
2. **LC**, as in PIC16**LC**54A. These devices have EPROM program memory and operate over an extended voltage range.
3. **CR**, as in PIC16**CR**54A. These devices have ROM program memory and operate over the standard voltage range.
4. **LCR**, as in PIC16**LCR**54A. These devices have ROM program memory and operate over an extended voltage range.

### 2.1 UV Erasable Devices (EPROM)

The UV erasable versions offered in CERDIP packages, are optimal for prototype development and pilot programs.

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's PICSTART® Plus**(1)** and PRO MATE® programmers both support programming of the PIC16C5X. Third party programmers also are available. Refer to the Third Party Guide (DS00104) for a list of sources.

### 2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates, or small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

**Note 1:** PIC16LC54C and PIC16C54A devices require OSC2 not to be connected while programming with PICSTART® Plus programmer.

### 2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

### 2.4 Serialized Quick-Turnaround-Production (SQTP℠) Devices

Microchip offers the unique programming service where a few user defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

### 2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, giving the customer a low cost option for high volume, mature products.

## 5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the $\overline{MCLR}$/VPP pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is RESET. The DRT timer begins counting once it detects $\overline{MCLR}$ to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where $\overline{MCLR}$ is not tied to VDD is shown in Figure 5-3. VDD is allowed to rise and stabilize before bringing $\overline{MCLR}$ high. The chip will actually come out of reset TDRT msec after $\overline{MCLR}$ goes high.

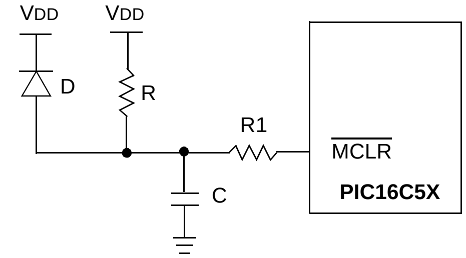
In Figure 5-4, the on-chip Power-On Reset feature is being used ($\overline{MCLR}$ and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the $\overline{MCLR}$/VPP pin, and when the $\overline{MCLR}$/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

| **Note:** | When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met. |
|---|---|

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the Embedded Control Handbook.

The POR circuit does not produce an internal RESET when VDD declines.

**FIGURE 5-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)**




- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$ pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

## 9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC16C5X family of microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator Selection (Section 4.0)
- RESET (Section 5.0)
- Power-On Reset (Section 5.1)
- Device Reset Timer (Section 5.2)
- Watchdog Timer (WDT) (Section 9.2)
- SLEEP (Section 9.3)
- Code protection (Section 9.4)
- ID locations (Section 9.5)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in RESET until the crystal oscillator is stable. With this timer on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake up from SLEEP through external RESET or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

### GOTO — Unconditional Branch

| | |
|---|---|
| Syntax: | [ *label* ] GOTO k |
| Operands: | $0 \le k \le 511$ |
| Operation: | k → PC<8:0>;<br>STATUS<6:5> → PC<10:9> |
| Status Affected: | None |
| Encoding: | `101k` `kkkk` `kkkk` |
| Description: | GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two-cycle instruction. |
| Words: | 1 |
| Cycles: | 2 |
| Example: | `GOTO THERE` |

After Instruction
PC = address (THERE)

### INCF — Increment f

| | |
|---|---|
| Syntax: | [ *label* ] INCF f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (f) + 1 → (dest) |
| Status Affected: | Z |
| Encoding: | `0010` `10df` `ffff` |
| Description: | The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. |
| Words: | 1 |
| Cycles: | 1 |
| Example: | `INCF CNT, 1` |

Before Instruction
CNT = 0xFF
Z = 0
After Instruction
CNT = 0x00
Z = 1

### INCFSZ — Increment f, Skip if 0

| | |
|---|---|
| Syntax: | [ *label* ] INCFSZ f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (f) + 1 → (dest), skip if result = 0 |
| Status Affected: | None |
| Encoding: | `0011` `11df` `ffff` |
| Description: | The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.<br>If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction. |
| Words: | 1 |
| Cycles: | 1(2) |
| Example: | see below |

```
HERE      INCFSZ    CNT, 1
          GOTO      LOOP
CONTINUE  •
          •
          •
```

Before Instruction
PC = address (HERE)
After Instruction
CNT = CNT + 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT ≠ 0,
PC = address (HERE +1)

### IORLW — Inclusive OR literal with W

| | |
|---|---|
| Syntax: | [ *label* ] IORLW k |
| Operands: | 0 ≤ k ≤ 255 |
| Operation: | (W) .OR. (k) → (W) |
| Status Affected: | Z |
| Encoding: | `1101` `kkkk` `kkkk` |
| Description: | The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register. |
| Words: | 1 |
| Cycles: | 1 |
| Example: | `IORLW` 0x35 |

Before Instruction
W = 0x9A
After Instruction
W = 0xBF
Z = 0

### IORWF — Inclusive OR W with f

| | |
|---|---|
| Syntax: | [ *label* ] IORWF f,d |
| Operands: | 0 ≤ f ≤ 31<br>d ∈ [0,1] |
| Operation: | (W).OR. (f) → (dest) |
| Status Affected: | Z |
| Encoding: | `0001` `00df` `ffff` |
| Description: | Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. |
| Words: | 1 |
| Cycles: | 1 |
| Example: | `IORWF RESULT, 0` |

Before Instruction
RESULT = 0x13
W = 0x91
After Instruction
RESULT = 0x13
W = 0x93
Z = 0

### MOVF — Move f

| | |
|---|---|
| Syntax: | [ *label* ] MOVF f,d |
| Operands: | 0 ≤ f ≤ 31<br>d ∈ [0,1] |
| Operation: | (f) → (dest) |
| Status Affected: | Z |
| Encoding: | `0010` `00df` `ffff` |
| Description: | The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected. |
| Words: | 1 |
| Cycles: | 1 |
| Example: | `MOVF FSR, 0` |

After Instruction
W = value in FSR register

### MOVLW — Move Literal to W

| | |
|---|---|
| Syntax: | [ *label* ] MOVLW k |
| Operands: | 0 ≤ k ≤ 255 |
| Operation: | k → (W) |
| Status Affected: | None |
| Encoding: | `1100` `kkkk` `kkkk` |
| Description: | The eight bit literal 'k' is loaded into the W register. |
| Words: | 1 |
| Cycles: | 1 |
| Example: | `MOVLW` 0x5A |

After Instruction
W = 0x5A

## 11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for pre-compiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

## 11.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

## 11.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows environment were chosen to best make these features available to you, the end user.

## 11.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

## 13.4 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D030 | VIL | **Input Low Voltage** | | | | | |
| | | I/O ports | Vss | — | 0.15 VDD | V | Pin at hi-impedance |
| | | MCLR (Schmitt Trigger) | Vss | — | 0.15 VDD | V | |
| | | T0CKI (Schmitt Trigger) | Vss | — | 0.15 VDD | V | |
| | | OSC1 (Schmitt Trigger) | Vss | — | 0.15 VDD | V | RC mode only(3) |
| | | OSC1 | Vss | — | 0.3 VDD | V | XT, HS and LP modes |
| D040 | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | 0.45 VDD | — | VDD | V | For all VDD(4) |
| | | I/O ports | 2.0 | — | VDD | V | 4.0V < VDD ≤ 5.5V(4) |
| | | I/O ports | 0.36 VDD | — | VDD | V | VDD > 5.5V |
| | | MCLR (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | T0CKI (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | OSC1 (Schmitt Trigger) | 0.85 VDD | — | VDD | V | RC mode only(3) |
| | | OSC1 | 0.7 VDD | — | VDD | V | XT, HS and LP modes |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current(1,2)** | | | | | **For VDD ≤ 5.5V:** |
| | | I/O ports | –1.0 | 0.5 | +1.0 | μA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| | | MCLR | –5.0 | — | — | μA | VPIN = VSS + 0.25V |
| | | MCLR | — | 0.5 | +5.0 | μA | VPIN = VDD |
| | | T0CKI | –3.0 | 0.5 | +3.0 | μA | VSS ≤ VPIN ≤ VDD |
| | | OSC1 | –3.0 | 0.5 | +3.0 | μA | VSS ≤ VPIN ≤ VDD, XT, HS and LP modes |
| D080 | VOL | **Output Low Voltage** | | | | | |
| | | I/O ports | — | — | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | — | — | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V, RC mode only |
| D090 | VOH | **Output High Voltage(2)** | | | | | |
| | | I/O ports | VDD – 0.7 | — | — | V | IOH = –5.4 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | VDD – 0.7 | — | — | V | IOH = –1.0 mA, VDD = 4.5V, RC mode only |

* These parameters are characterized but not tested.

† Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

**4:** The user may use the better of the two specifications.

## 15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

| **PIC16LC54A-04**<br>**PIC16LC54A-04I**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
|---|---|---|---|---|---|---|---|
| **PIC16C54A-04, 10, 20**<br>**PIC16C54A-04I, 10I, 20I**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D006 | IPD | **Power-down Current(2)** | | | | | |
| | | PIC16LC5X | —<br>—<br>—<br>— | 2.5<br>0.25<br>2.5<br>0.25 | 12<br>4.0<br>14<br>5.0 | μA<br>μA<br>μA<br>μA | VDD = 2.5V, WDT enabled, Commercial<br>VDD = 2.5V, WDT disabled, Commercial<br>VDD = 2.5V, WDT enabled, Industrial<br>VDD = 2.5V, WDT disabled, Industrial |
| D006A | | PIC16C5X | —<br>—<br>—<br>— | 4.0<br>0.25<br>5.0<br>0.3 | 12<br>4.0<br>14<br>5.0 | μA<br>μA<br>μA<br>μA | VDD = 3.0V, WDT enabled, Commercial<br>VDD = 3.0V, WDT disabled, Commercial<br>VDD = 3.0V, WDT enabled, Industrial<br>VDD = 3.0V, WDT disabled, Industrial |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in “Typ” column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

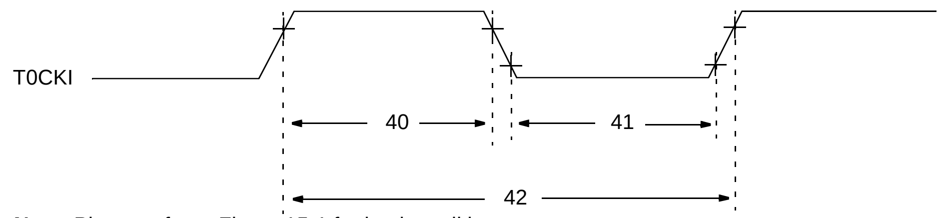
**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

**FIGURE 15-5: TIMER0 CLOCK TIMINGS - PIC16C54A**




**Note:** Please refer to Figure 15-1 for load conditions.

**TABLE 15-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54A**

| AC Characteristics | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I<br>–40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 40 | Tt0H | T0CKI High Pulse Width | | | | | |
| | | - No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width | | | | | |
| | | - No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | 20 or $\frac{T_{CY} + 40}{N}$* | — | — | ns | Whichever is greater.<br>N = Prescale Value (1, 2, 4,..., 256) |

* These parameters are characterized but not tested.

† Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 16-10: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, 25°C)**

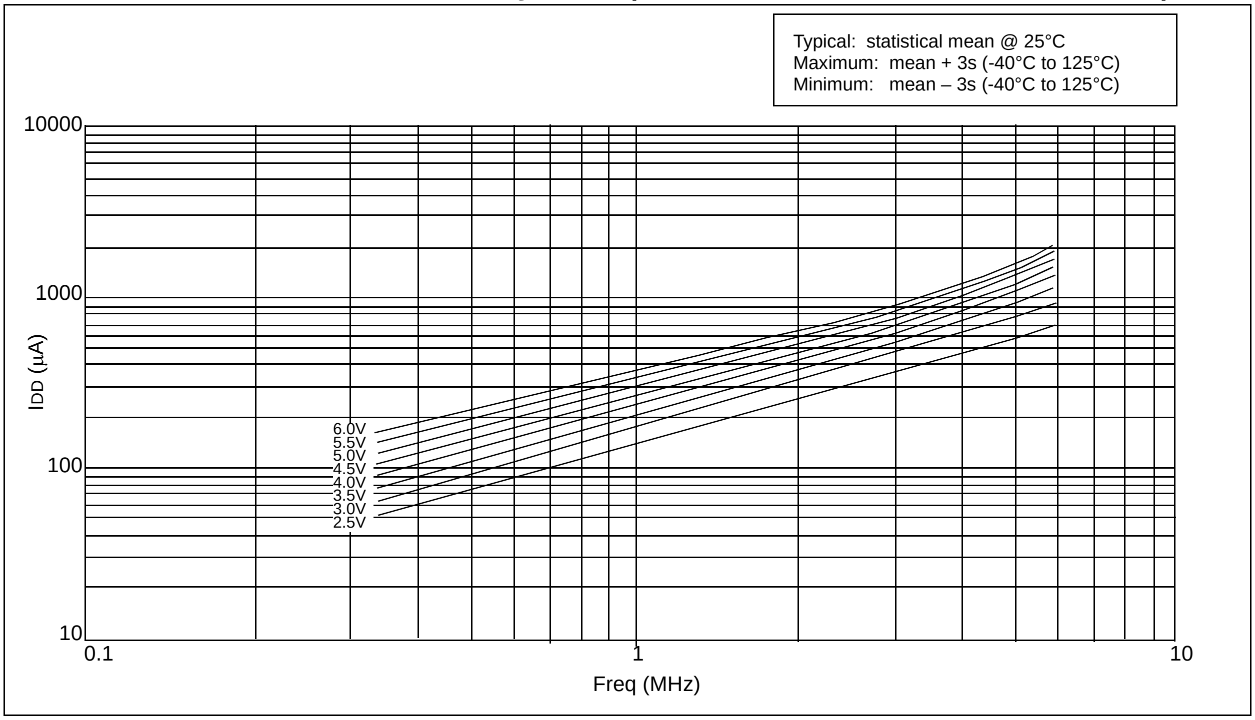



**FIGURE 16-11: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, –40°C to +85°C)**

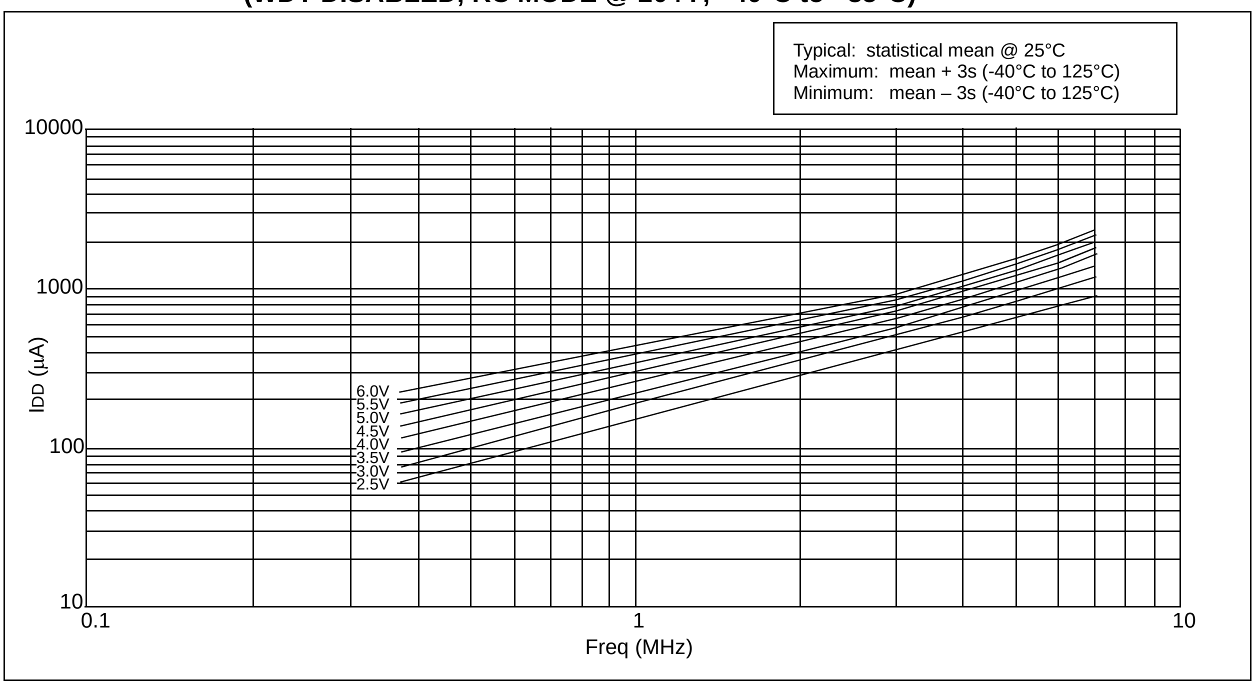


**FIGURE 16-12: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, 25°C)**

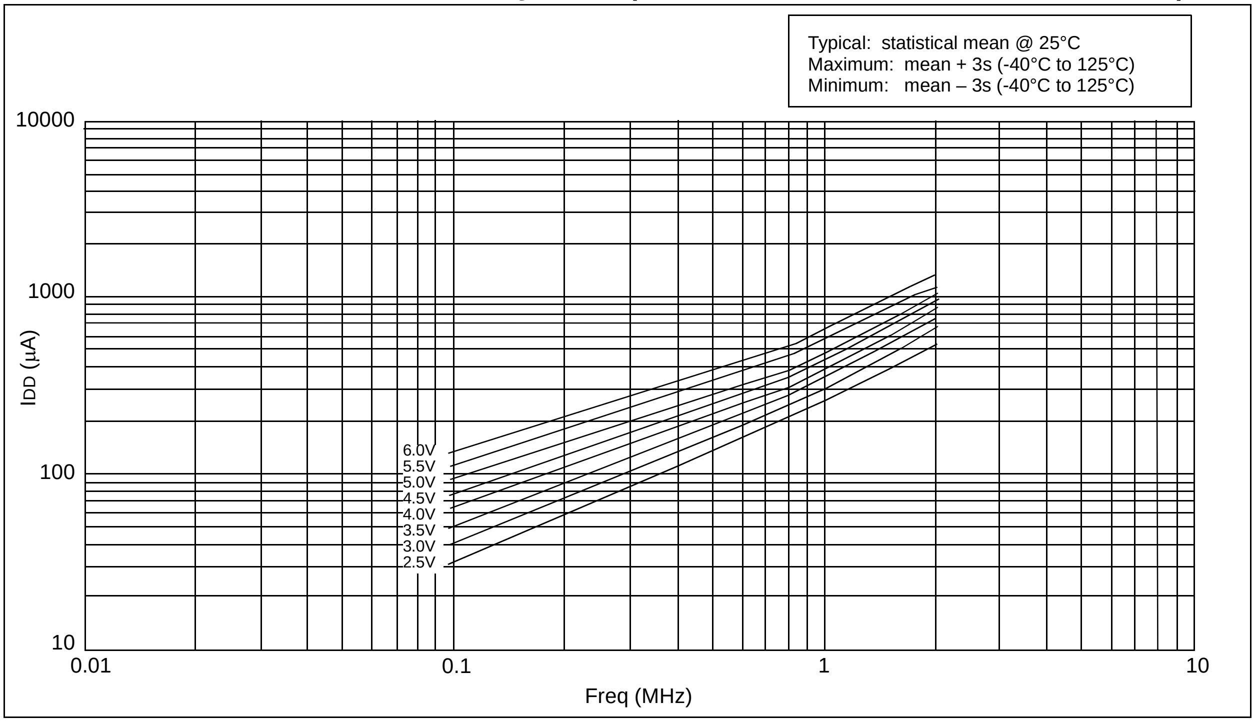
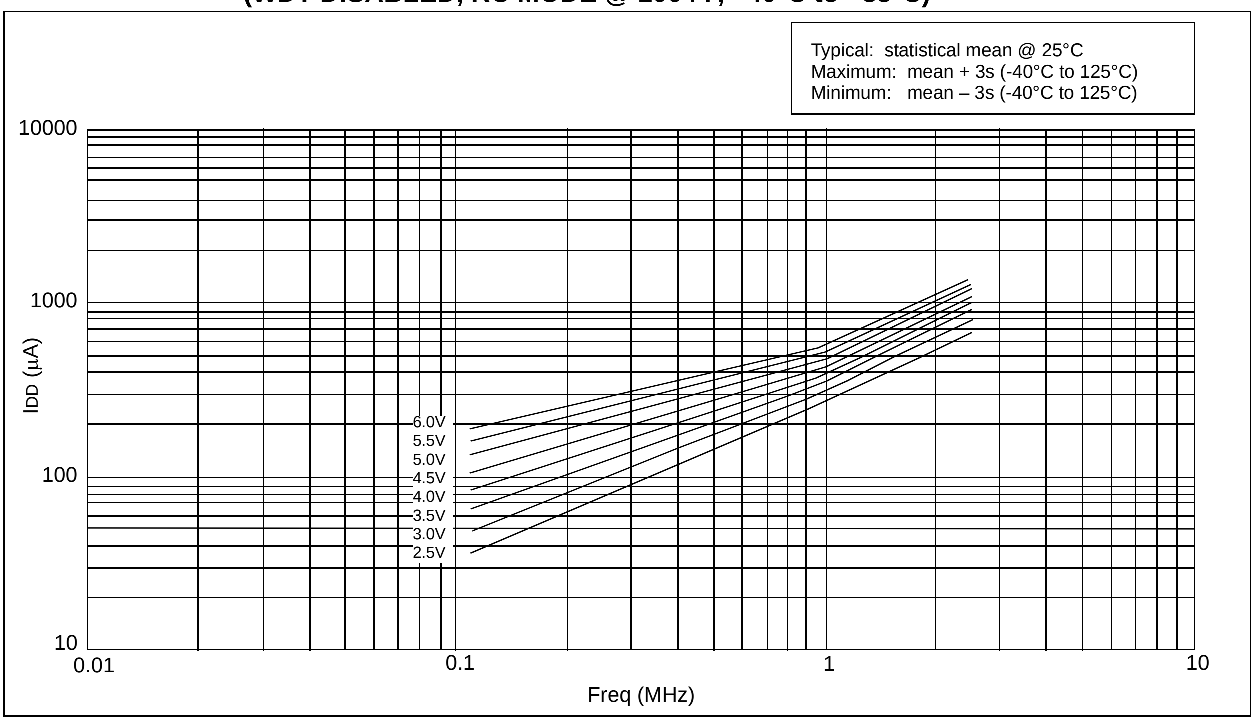



**FIGURE 16-13: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, –40°C to +85°C)**




 Preliminary 

**FIGURE 16-14: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, 25°C)**

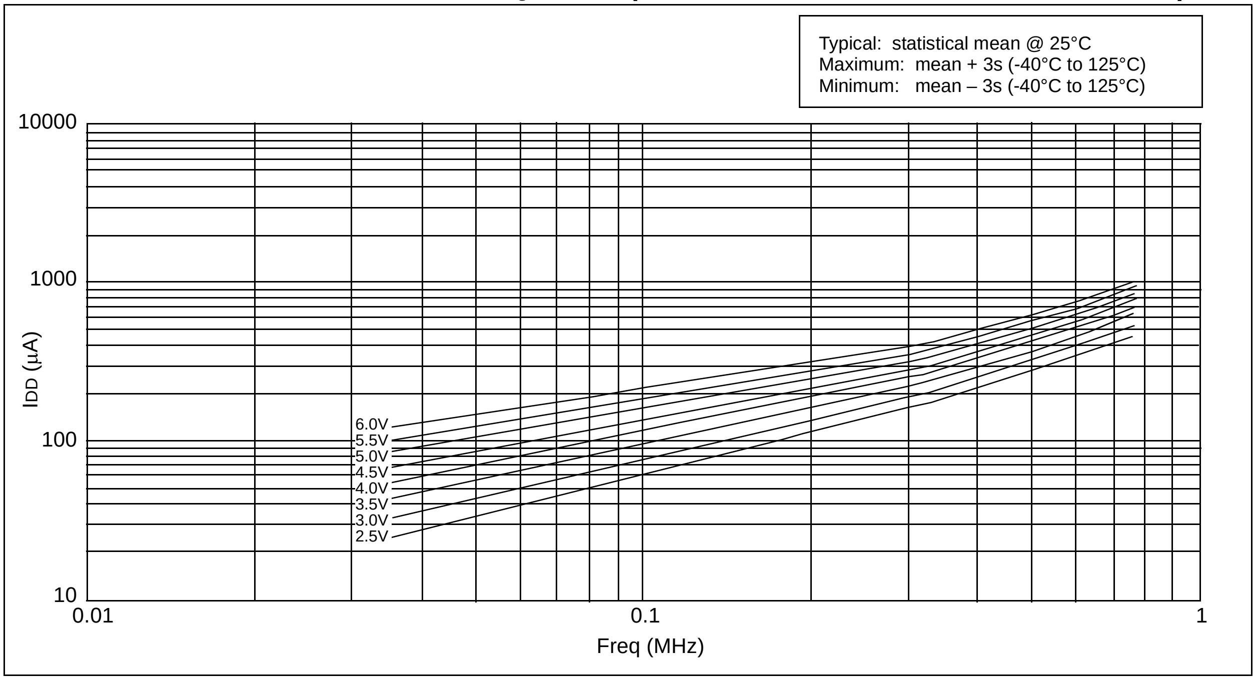



**FIGURE 16-15: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, –40°C to +85°C)**

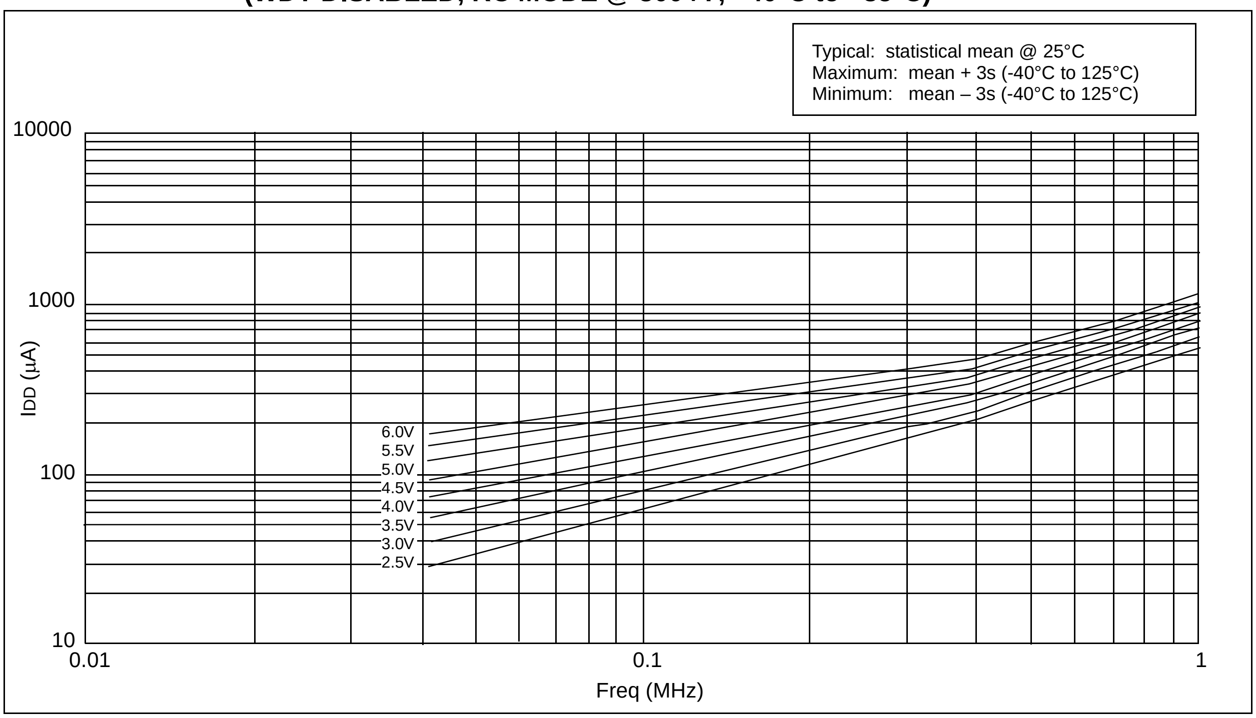


**TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 2 | Tcy | Instruction Cycle Time(2) | — | 4/FOSC | — | — | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 50* | — | — | ns | XT oscillator |
| | | | 20* | — | — | ns | HS oscillator |
| | | | 2.0* | — | — | μs | LP oscillator |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 25* | ns | XT oscillator |
| | | | — | — | 25* | ns | HS oscillator |
| | | | — | — | 50* | ns | LP oscillator |

* These parameters are characterized but not tested.

† Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

**FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF, 25°C**

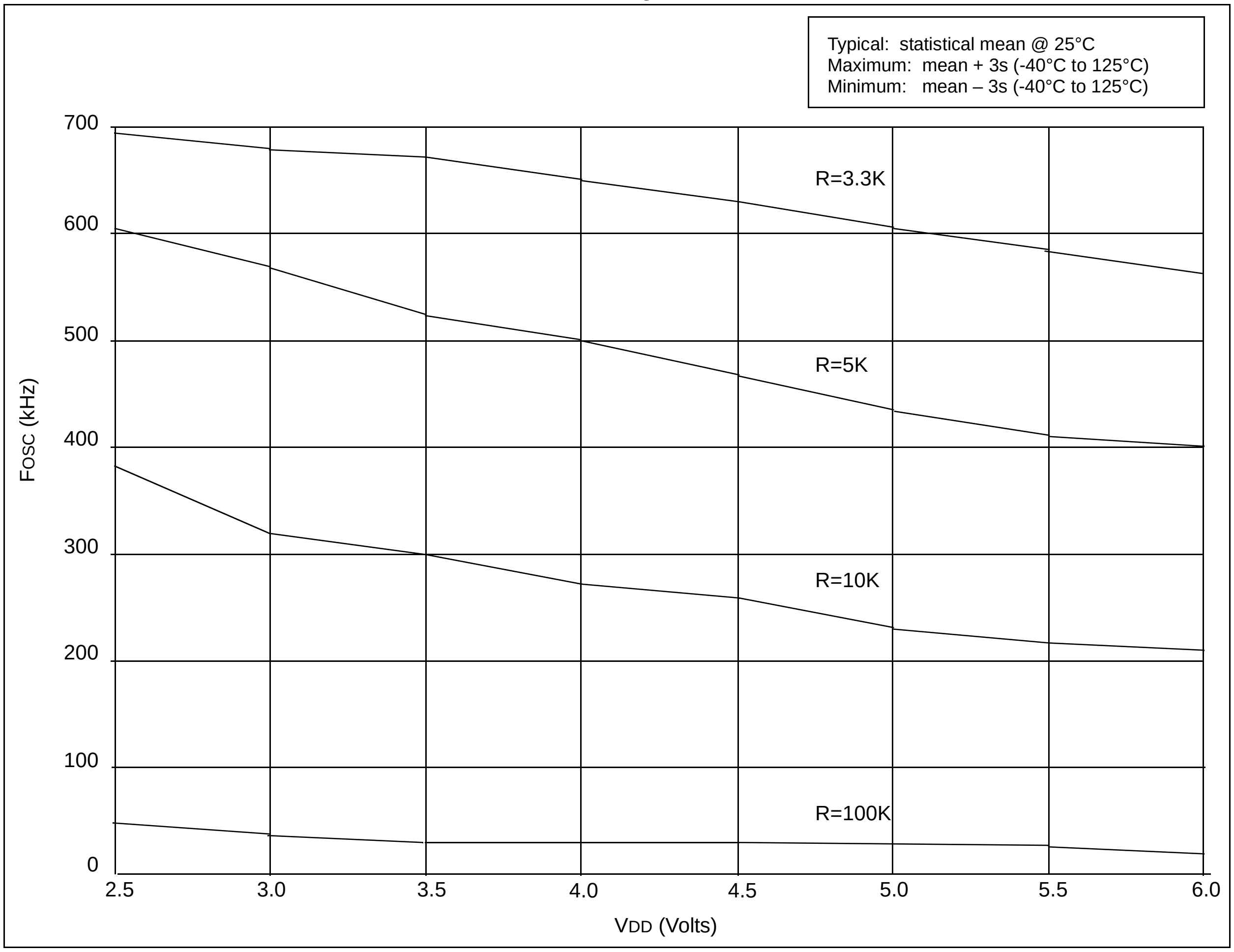



**FIGURE 18-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)**

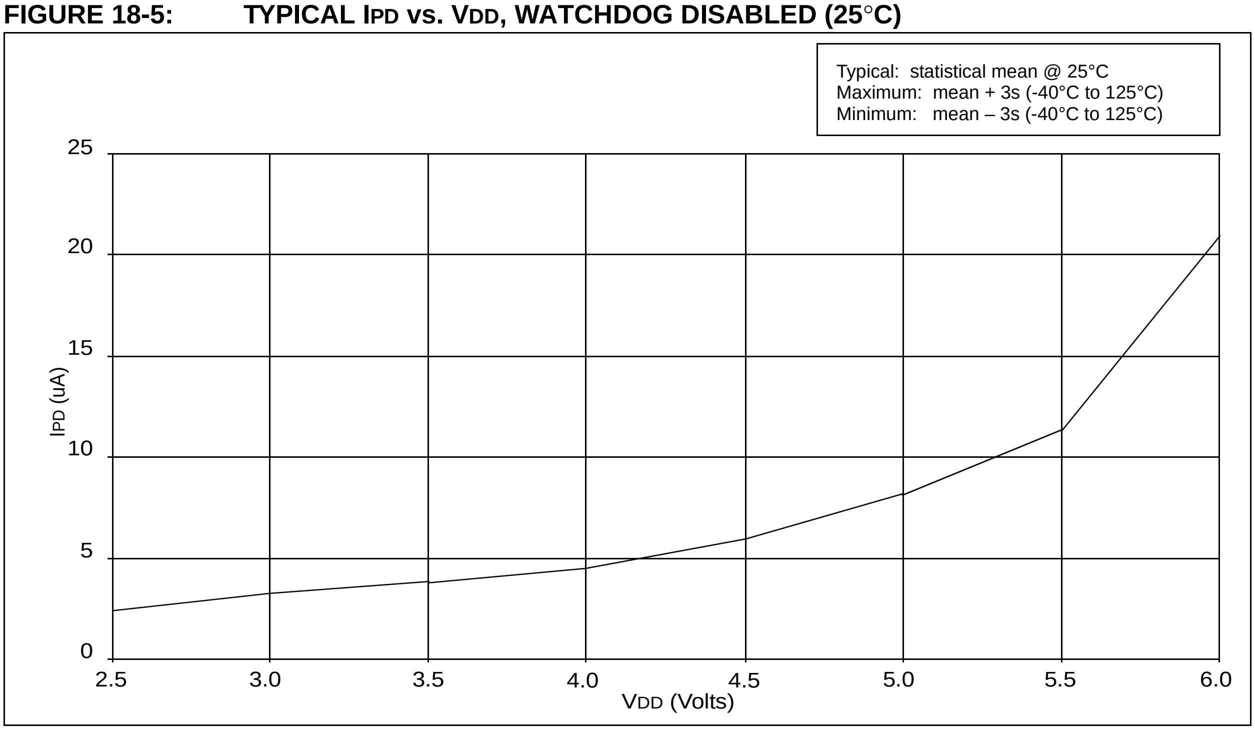


**FIGURE 18-12: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, 25°C)**

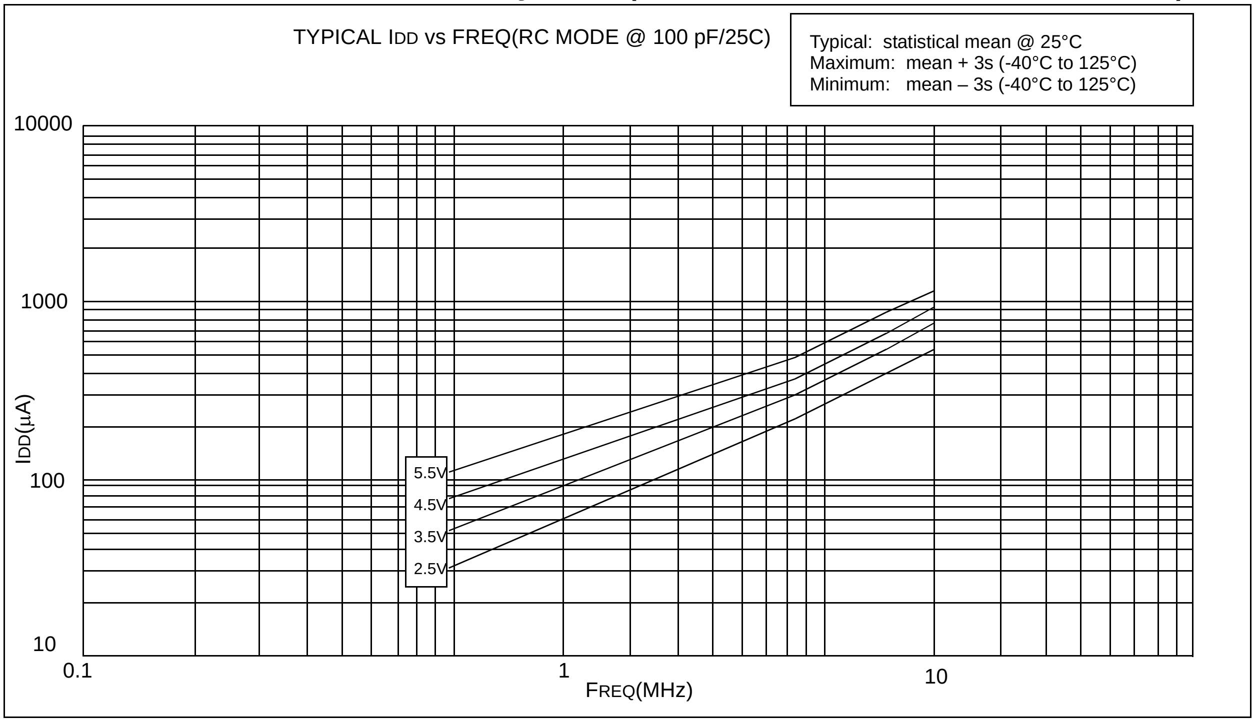
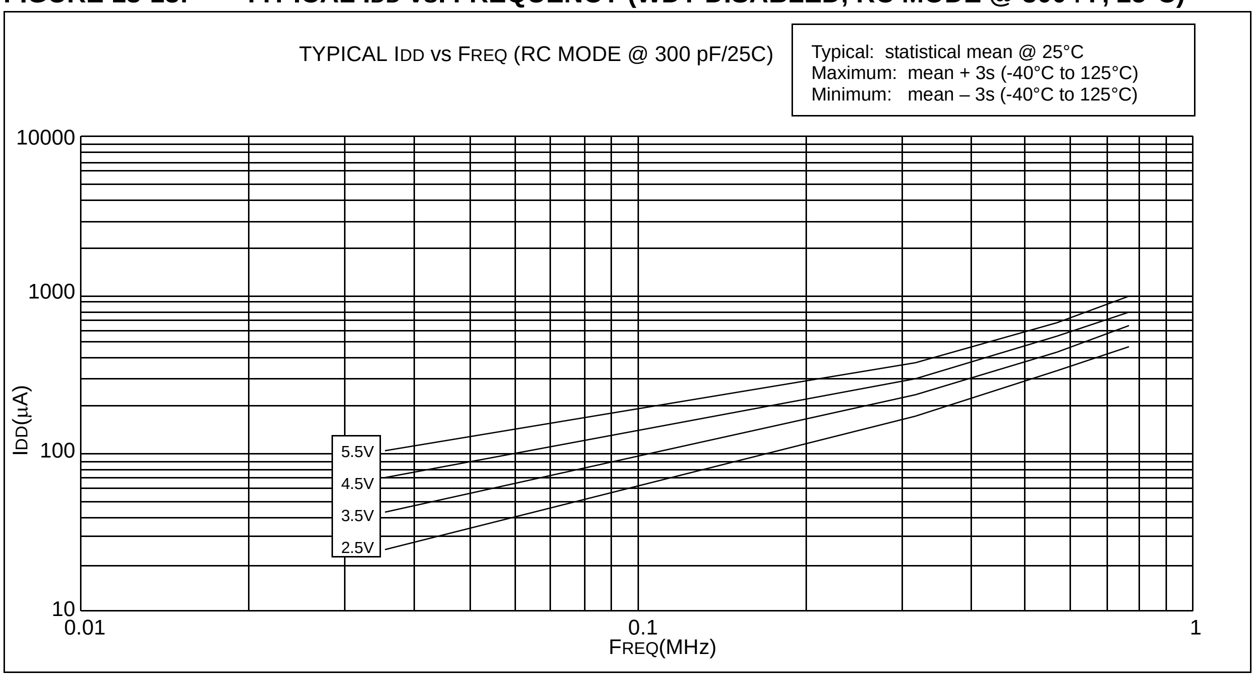


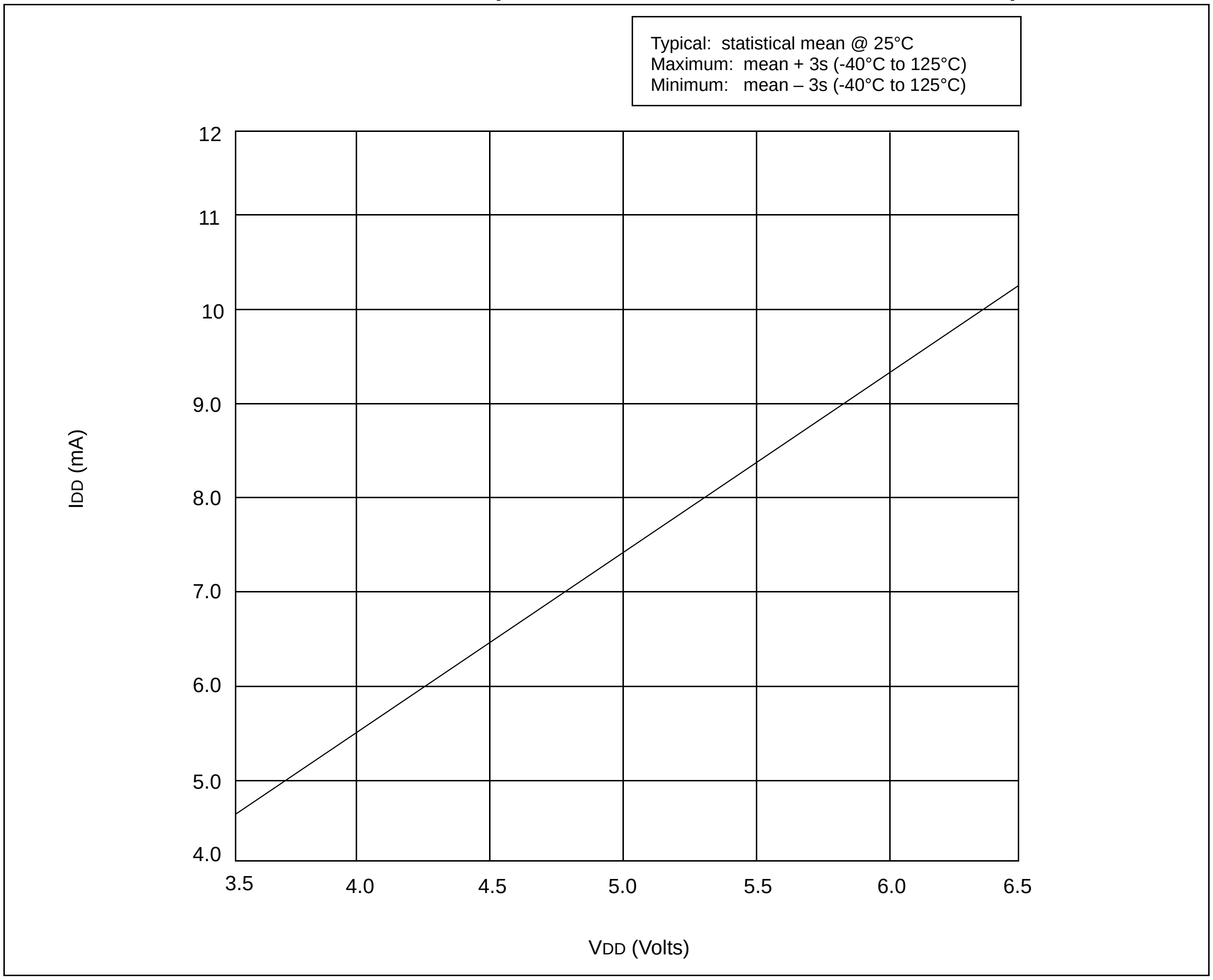

**FIGURE 18-13: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, 25°C)**



**NOTES:**

**FIGURE 20-6: TYPICAL IDD vs. VDD (40 MHZ, WDT DISABLED, HS MODE, 70°C)**

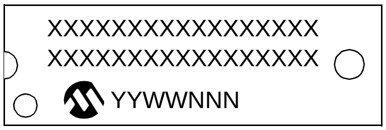


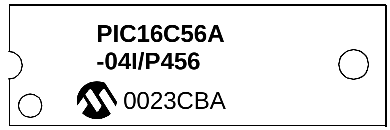
# 21.0 PACKAGING INFORMATION

## 21.1 Package Marketing Information

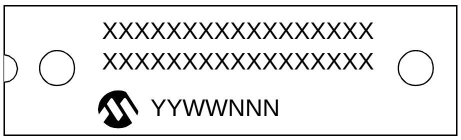
18-Lead PDIP



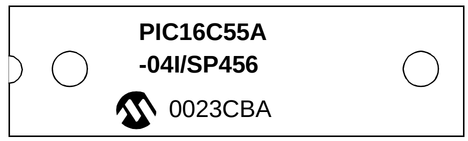

Example



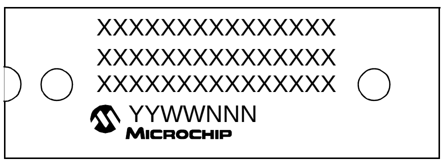

28-Lead Skinny PDIP (.300")



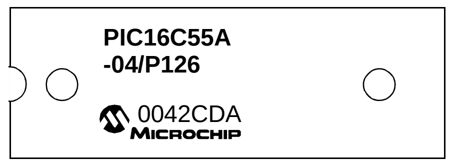

Example



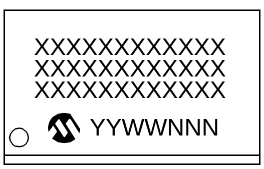

28-Lead PDIP (.600")




Example

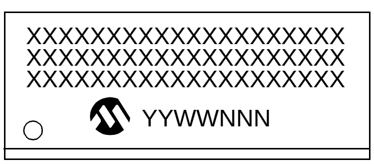



18-Lead SOIC



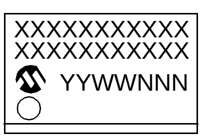

Example


28-Lead SOIC




Example


20-Lead SSOP



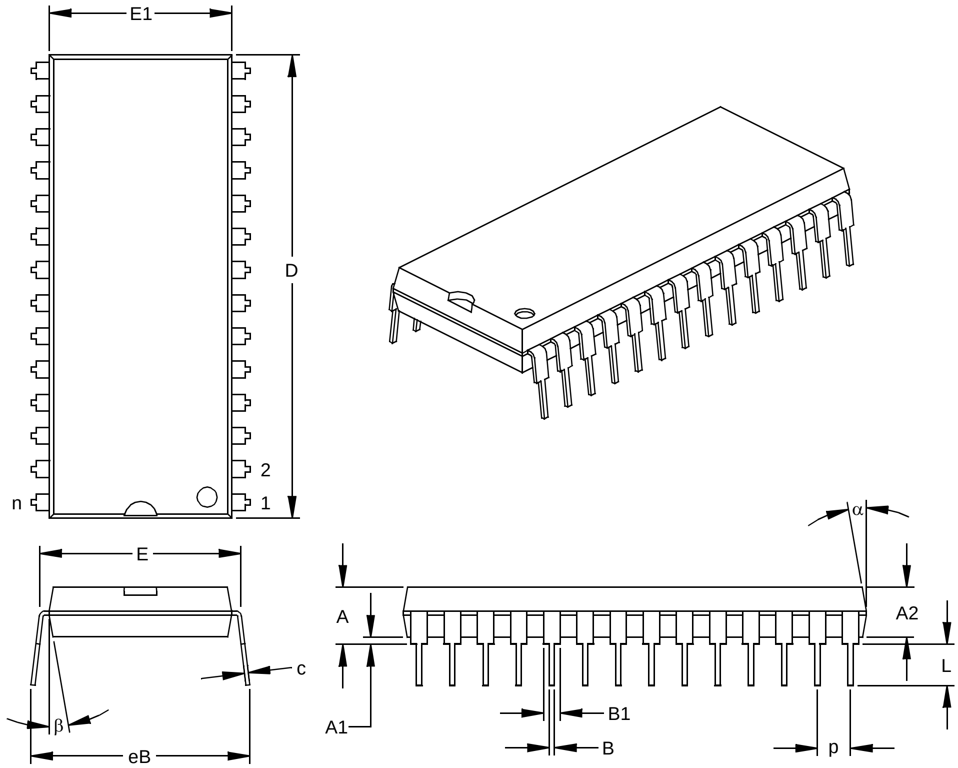

Example


28-Lead SSOP


Example

## 28-Lead Plastic Dual In-line (P) – 600 mil (PDIP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

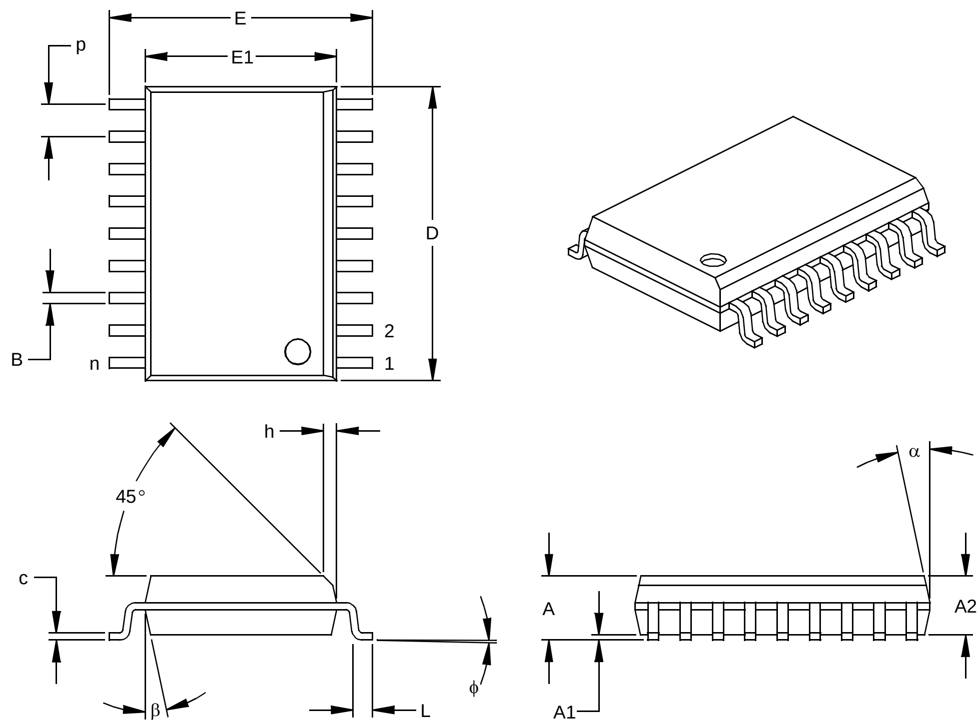



| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .160 | .175 | .190 | 4.06 | 4.45 | 4.83 |
| Molded Package Thickness | A2 | .140 | .150 | .160 | 3.56 | 3.81 | 4.06 |
| Base to Seating Plane | A1 | .015 | | | 0.38 | | |
| Shoulder to Shoulder Width | E | .595 | .600 | .625 | 15.11 | 15.24 | 15.88 |
| Molded Package Width | E1 | .505 | .545 | .560 | 12.83 | 13.84 | 14.22 |
| Overall Length | D | 1.395 | 1.430 | 1.465 | 35.43 | 36.32 | 37.21 |
| Tip to Seating Plane | L | .120 | .130 | .135 | 3.05 | 3.30 | 3.43 |
| Lead Thickness | c | .008 | .012 | .015 | 0.20 | 0.29 | 0.38 |
| Upper Lead Width | B1 | .030 | .050 | .070 | 0.76 | 1.27 | 1.78 |
| Lower Lead Width | B | .014 | .018 | .022 | 0.36 | 0.46 | 0.56 |
| Overall Row Spacing § | eB | .620 | .650 | .680 | 15.75 | 16.51 | 17.27 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-011
Drawing No. C04-079

## 18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 18 | | | 18 | |
| Pitch | p | | .050 | | | 1.27 | |
| Overall Height | A | .093 | .099 | .104 | 2.36 | 2.50 | 2.64 |
| Molded Package Thickness | A2 | .088 | .091 | .094 | 2.24 | 2.31 | 2.39 |
| Standoff § | A1 | .004 | .008 | .012 | 0.10 | 0.20 | 0.30 |
| Overall Width | E | .394 | .407 | .420 | 10.01 | 10.34 | 10.67 |
| Molded Package Width | E1 | .291 | .295 | .299 | 7.39 | 7.49 | 7.59 |
| Overall Length | D | .446 | .454 | .462 | 11.33 | 11.53 | 11.73 |
| Chamfer Distance | h | .010 | .020 | .029 | 0.25 | 0.50 | 0.74 |
| Foot Length | L | .016 | .033 | .050 | 0.41 | 0.84 | 1.27 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .009 | .011 | .012 | 0.23 | 0.27 | 0.30 |
| Lead Width | B | .014 | .017 | .020 | 0.36 | 0.42 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-051