Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc54at-04e-so

NOTES:

3.0   ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle except for program branches.

The PIC16C54/CR54 and PIC16C55 address 512 x 12 of program memory, the PIC16C56/CR56 address 1K x 12 of program memory, and the PIC16C57/CR57 and PIC16C58/CR58 address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 (for PIC16C54/56/58) and Table 3-2 (for PIC16C55/57).

5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the $\overline{MCLR}$/Vpp pin to Vdd. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is RESET. The DRT timer begins counting once it detects $\overline{MCLR}$ to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where $\overline{MCLR}$ is not tied to Vdd is shown in Figure 5-3. Vdd is allowed to rise and stabilize before bringing $\overline{MCLR}$ high. The chip will actually come out of reset Tdrt msec after $\overline{MCLR}$ goes high.

In Figure 5-4, the on-chip Power-On Reset feature is being used ($\overline{MCLR}$ and Vdd are tied together). The Vdd is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where Vdd rises too slowly. The time between when the DRT senses a high on the $\overline{MCLR}$/Vpp pin, and when the $\overline{MCLR}$/Vpp pin (and Vdd) actually reach their full value, is too long. In this situation, when the start-up timer times out, Vdd has not reached the Vdd (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

Note:	When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the Embedded Control Handbook.

The POR circuit does not produce an internal RESET when Vdd declines.

FIGURE 5-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)

- External Power-On Reset circuit is required only if Vdd power-up is too slow. The diode D helps discharge the capacitor quickly when Vdd powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$ pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

PIC16C5X

FIGURE 8-3: **TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALER**

	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4
PC (Program Counter)	PC-1	PC	PC+1	PC+2	PC+3	PC+4	PC+5	PC+6
Instruction Fetch		MOVWF TMR0	MOVF TMR0,W	MOVF TMR0,W	MOVF TMR0,W	MOVF TMR0,W	MOVF TMR0,W	
Timer0	T0	T0+1	T0+2	NT0	NT0	NT0	NT0+1	NT0+2
Instruction Executed			Write TMR0 executed	Read TMR0 reads NT0	Read TMR0 reads NT0	Read TMR0 reads NT0	Read TMR0 reads NT0 + 1	Read TMR0 reads NT0 + 2

FIGURE 8-4: **TIMER0 TIMING: INTERNAL CLOCK/PRESCALER 1:2**

	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4
PC (Program Counter)	PC-1	PC	PC+1	PC+2	PC+3	PC+4	PC+5	PC+6
Instruction Fetch		MOVWF TMR0	MOVF TMR0,W	MOVF TMR0,W	MOVF TMR0,W	MOVF TMR0,W	MOVF TMR0,W	
Timer0	T0	T0+1			NT0			NT0+1
Instruction Execute			Write TMR0 executed	Read TMR0 reads NT0	Read TMR0 reads NT0	Read TMR0 reads NT0	Read TMR0 reads NT0	Read TMR0 reads NT0 + 1

TABLE 8-1: **REGISTERS ASSOCIATED WITH TIMER0**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on MCLR and WDT Reset
01h	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells not used by Timer0.

Preliminary

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	$0 \leq f \leq 31$
Operation:	$(W) \rightarrow (f)$
Status Affected:	None
Encoding:	`0000` `001f` `ffff`
Description:	Move data from the W register to register 'f'.
Words:	1
Cycles:	1
Example:	MOVWF TEMP_REG

    Before Instruction
        TEMP_REG = 0xFF
        W = 0x4F
    After Instruction
        TEMP_REG = 0x4F
        W = 0x4F

NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Encoding:	`0000` `0000` `0000`
Description:	No operation.
Words:	1
Cycles:	1
Example:	NOP

OPTION	Load OPTION Register
Syntax:	[*label*] OPTION
Operands:	None
Operation:	$(W) \rightarrow OPTION$
Status Affected:	None
Encoding:	`0000` `0000` `0010`
Description:	The content of the W register is loaded into the OPTION register.
Words:	1
Cycles:	1
Example	OPTION

    Before Instruction
        W = 0x07
    After Instruction
        OPTION = 0x07

RETLW	Return with Literal in W
Syntax:	[*label*] RETLW k
Operands:	$0 \leq k \leq 255$
Operation:	$k \rightarrow (W)$; $TOS \rightarrow PC$
Status Affected:	None
Encoding:	`1000` `kkkk` `kkkk`
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Words:	1
Cycles:	2

Example:
```
        CALL TABLE ;W contains
                   ;table offset
                   ;value.
        •          ;W now has table
        •          ;value.
TABLE   •
        ADDWF PC  ;W = offset
        RETLW k1  ;Begin table
        RETLW k2  ;
        •
        •
        •
        RETLW kn  ; End of table
```

    Before Instruction
        W = 0x07
    After Instruction
        W = value of k8

SUBWF	Subtract W from f
Syntax:	[*label*] SUBWF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	$(f) - (W) \rightarrow (dest)$
Status Affected:	C, DC, Z
Encoding:	`0000` `10df` `ffff`
Description:	Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1

Example 1:   SUBWF   REG1, 1

    Before Instruction
      REG1   =   3
      W   =   2
      C   =   ?
    After Instruction
      REG1   =   1
      W   =   2
      C   =   1   ; result is positive

Example 2:
    Before Instruction
      REG1   =   2
      W   =   2
      C   =   ?
    After Instruction
      REG1   =   0
      W   =   2
      C   =   1   ; result is zero

Example 3:
    Before Instruction
      REG1   =   1
      W   =   2
      C   =   ?
    After Instruction
      REG1   =   0xFF
      W   =   2
      C   =   0   ; result is negative

SWAPF	Swap Nibbles in f
Syntax:	[*label*] SWAPF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	$(f<3:0>) \rightarrow (dest<7:4>)$; $(f<7:4>) \rightarrow (dest<3:0>)$
Status Affected:	None
Encoding:	`0011` `10df` `ffff`
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.
Words:	1
Cycles:	1

Example   SWAPF   REG1, 0

    Before Instruction
      REG1   =   0xA5
    After Instruction
      REG1   =   0xA5
      W   =   0x5A

TRIS	Load TRIS Register
Syntax:	[*label*] TRIS f
Operands:	f = 5, 6 or 7
Operation:	$(W) \rightarrow$ TRIS register f
Status Affected:	None
Encoding:	`0000` `0000` `0fff`
Description:	TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register.
Words:	1
Cycles:	1

Example   TRIS   PORTB

    Before Instruction
      W   =   0xA5
    After Instruction
      TRISB =   0xA5

FIGURE 12-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54/55/56/57

Note 1: Please refer to Figure 12-1 for load conditions.
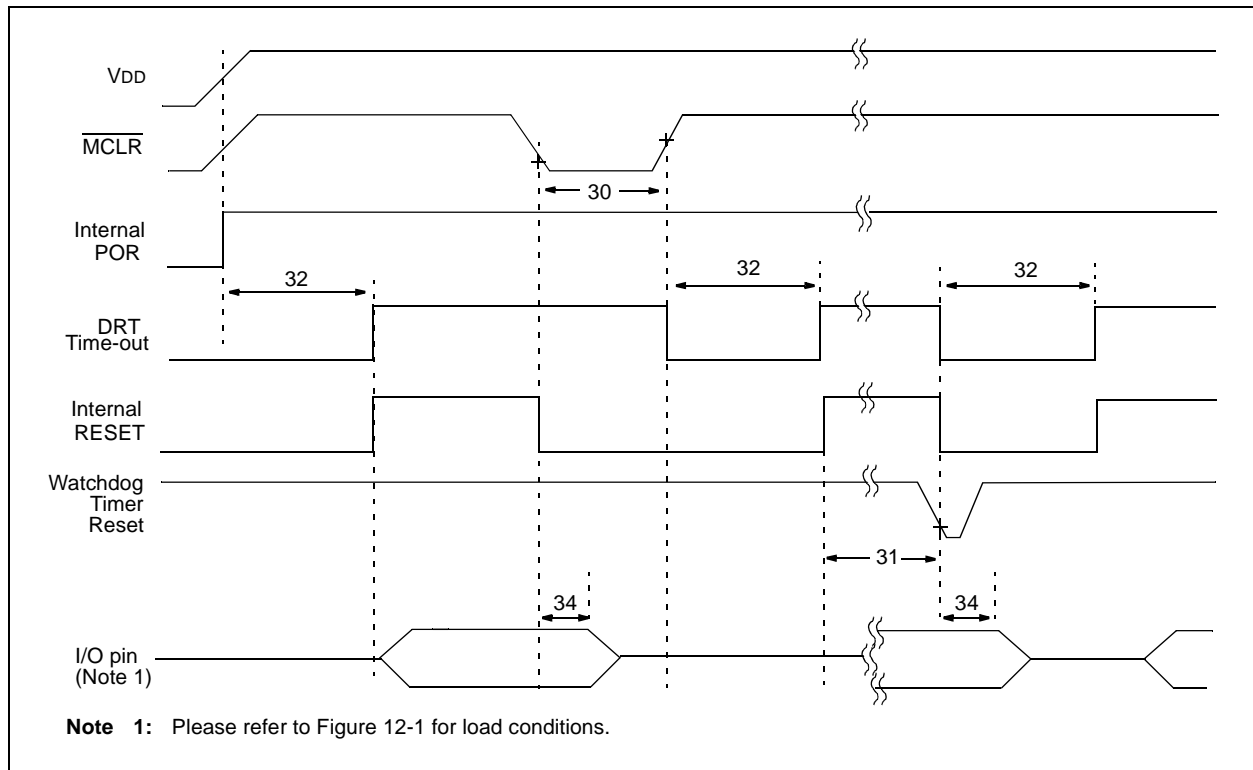
TABLE 12-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial −40°C ≤ TA ≤ +85°C for industrial −40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	100*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from $\overline{MCLR}$ Low	—	—	100*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 14-6: **MAXIMUM IPD vs. VDD, WATCHDOG DISABLED**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)
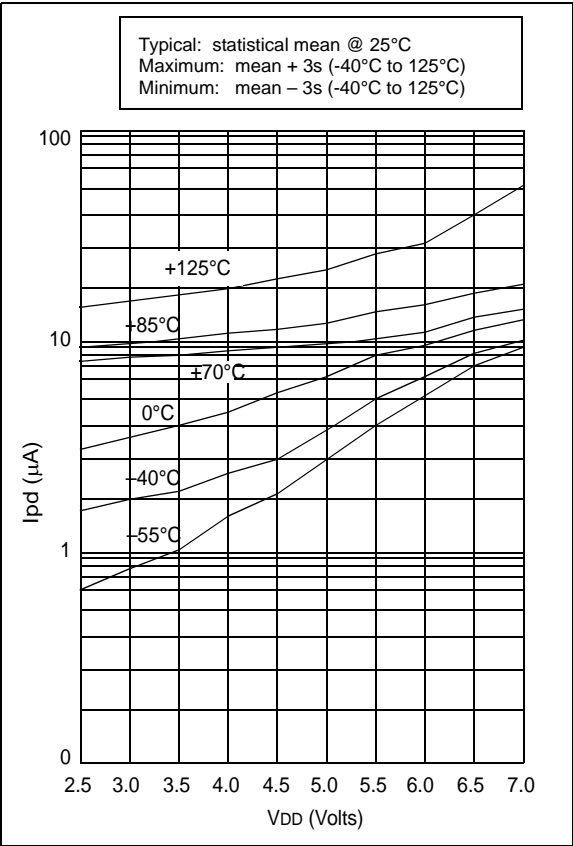
FIGURE 14-7: **TYPICAL IPD vs. VDD, WATCHDOG ENABLED**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)
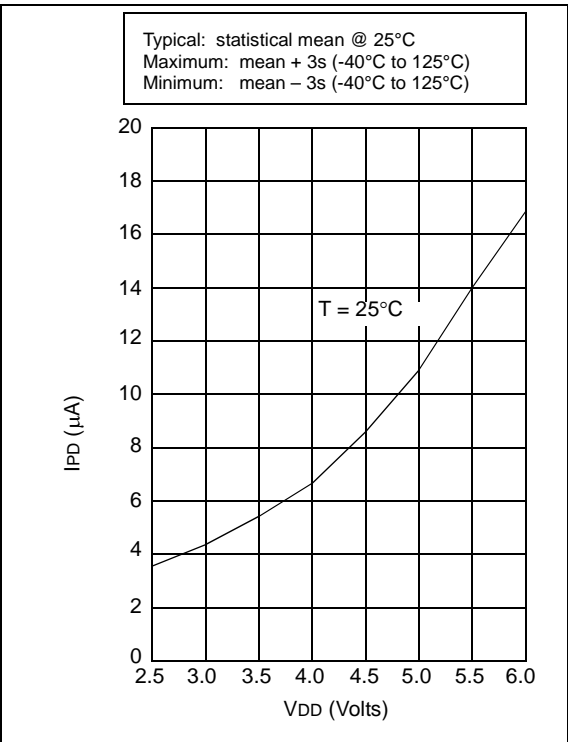
FIGURE 14-8: **MAXIMUM IPD vs. VDD, WATCHDOG ENABLED**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

IPD, with WDT enabled, has two components:
The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At –40°C, the latter dominates explaining the apparently anomalous behavior.

Preliminary
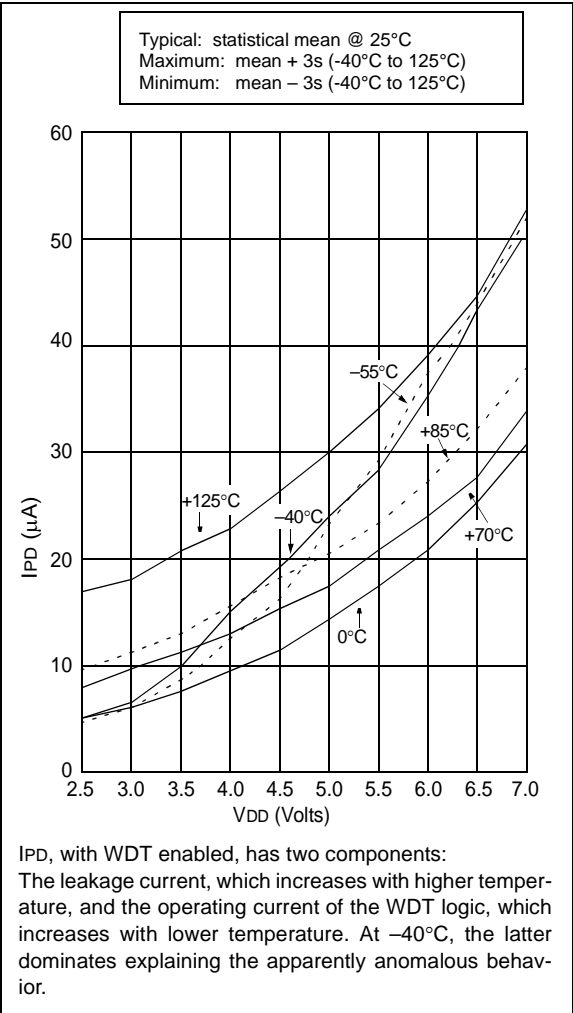
PIC16C5X

FIGURE 14-15: **WDT TIMER TIME-OUT PERIOD vs. VDD(1)**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Note 1: Prescaler set to 1:1.
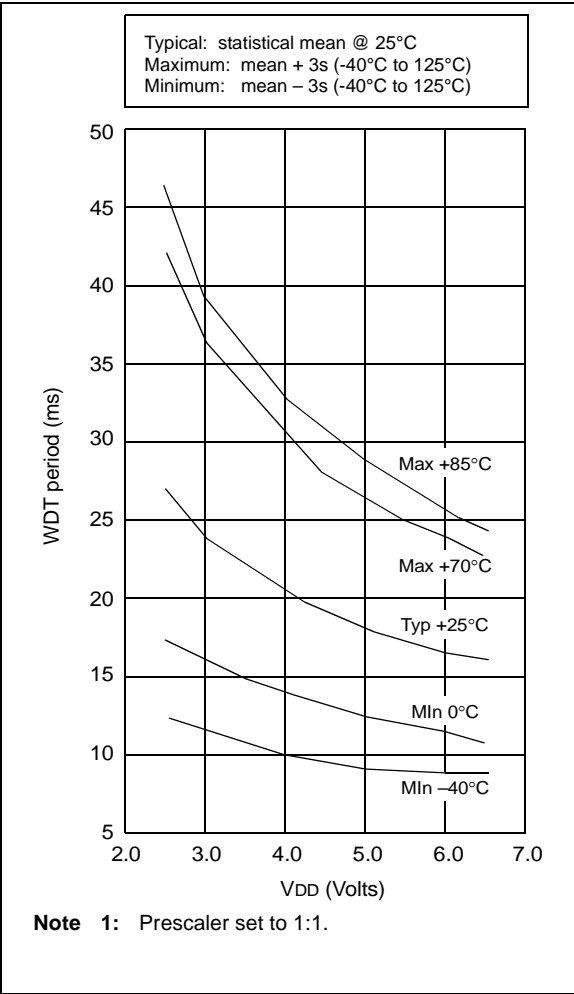
FIGURE 14-16: **TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Preliminary
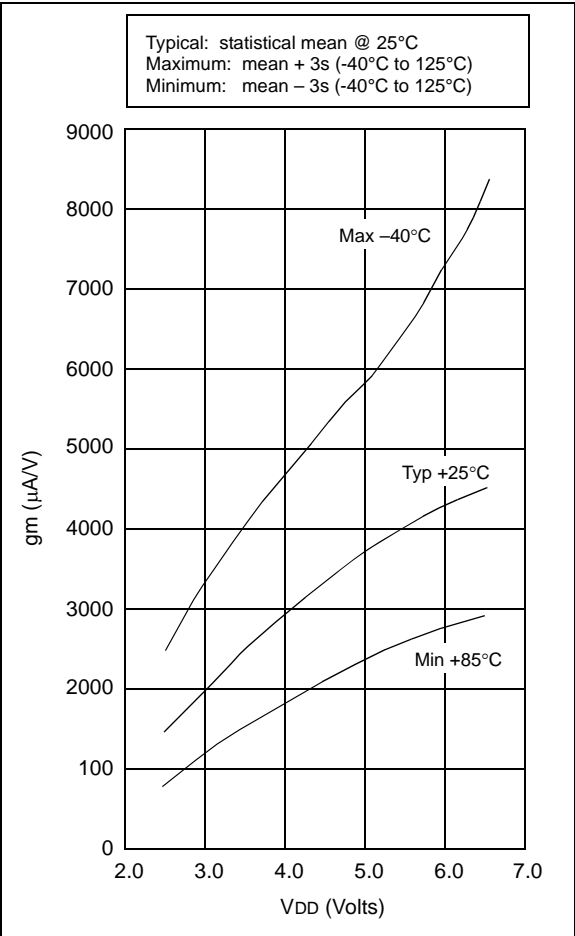
FIGURE 14-21: PORTA, B AND C IoL vs. VOL, VDD = 3 V

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean − 3s (-40°C to 125°C)
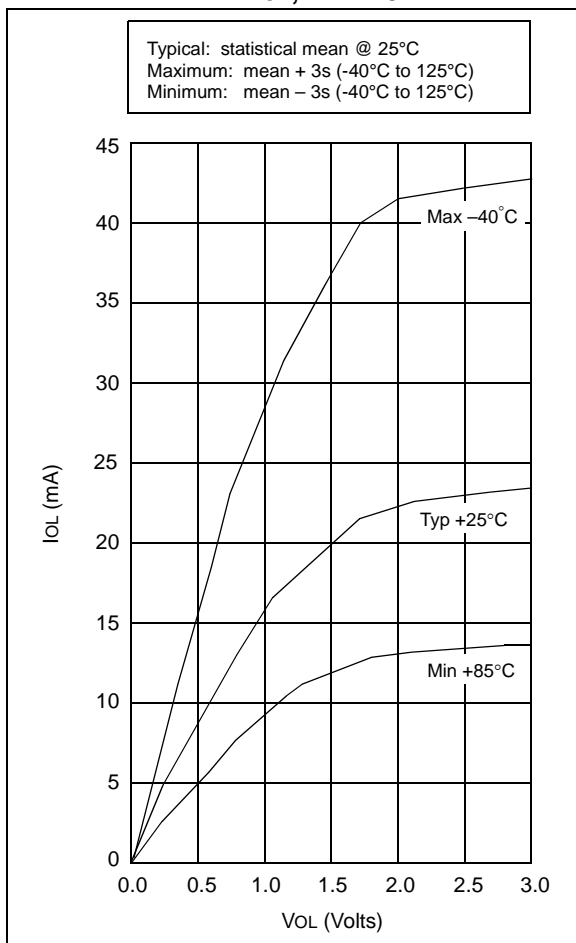
FIGURE 14-22: PORTA, B AND C IoL vs. VOL, VDD = 5 V

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean − 3s (-40°C to 125°C)
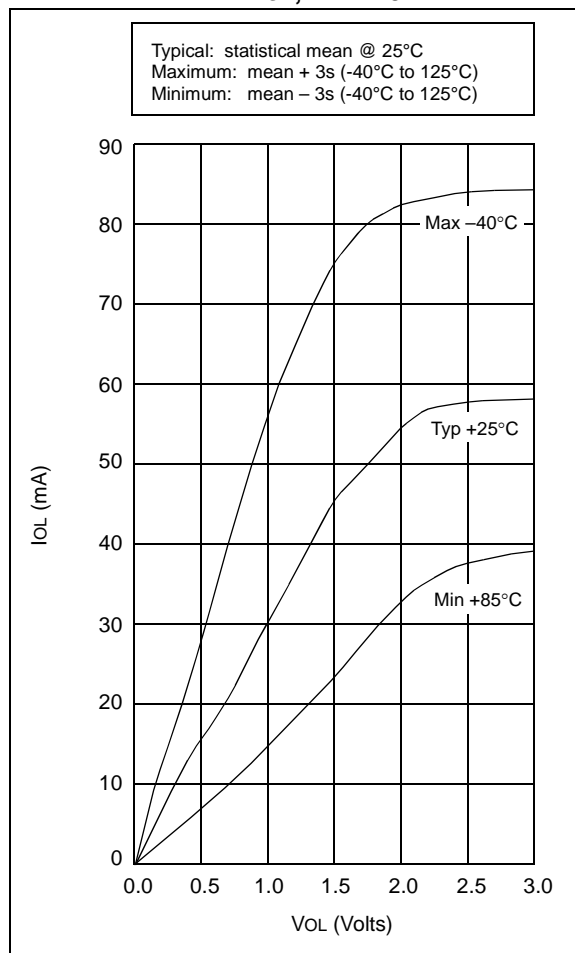
PIC16C5X

FIGURE 15-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A

Note 1: Please refer to Figure 15-1 for load conditions.
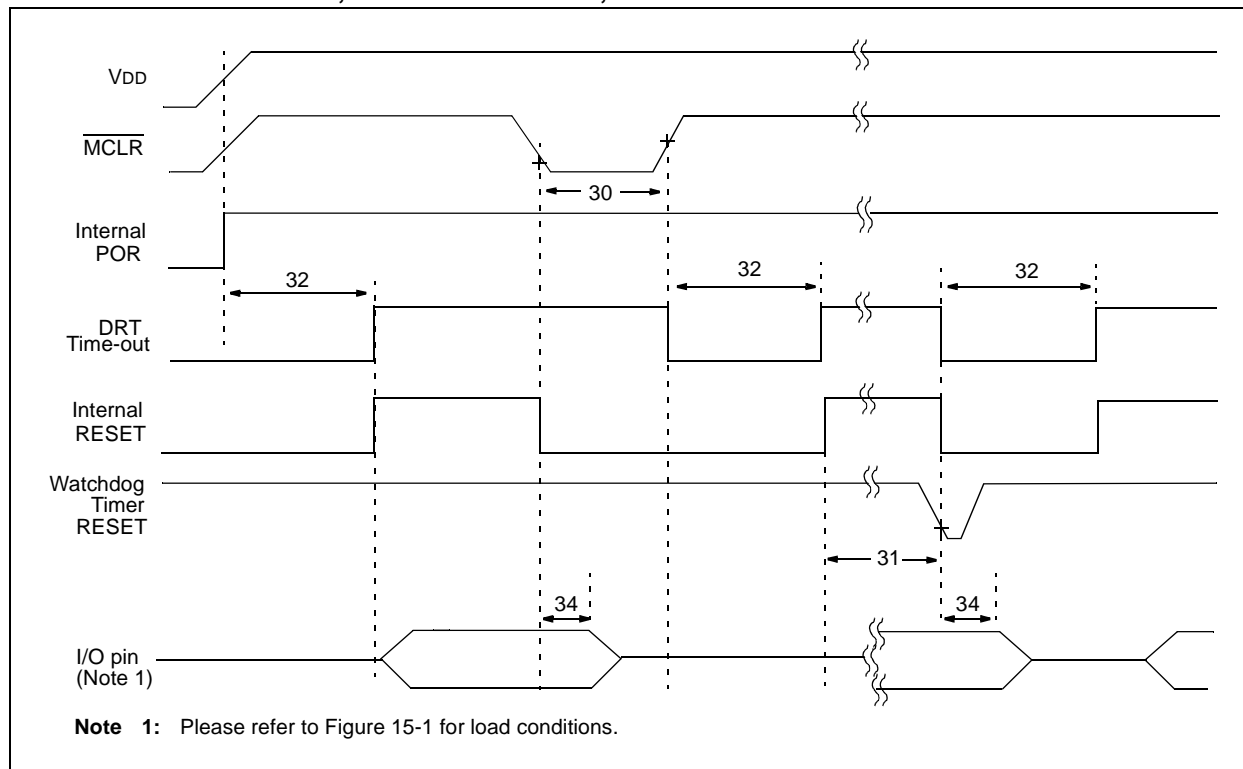
TABLE 15-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \leq T_A \leq +70°C$ for commercial $-40°C \leq T_A \leq +85°C$ for industrial $-20°C \leq T_A \leq +85°C$ for industrial - PIC16LV54A-02I $-40°C \leq T_A \leq +125°C$ for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	100* 1	— —	— —	ns µs	VDD = 5.0V VDD = 5.0V (PIC16LV54A only)
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	TioZ	I/O Hi-impedance from $\overline{MCLR}$ Low	— —	— —	100* 1µs	ns —	(PIC16LV54A only)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 16-22: PORTA, B AND C I$_{OL}$ vs. V$_{OL}$, V$_{DD}$ = 3V

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)
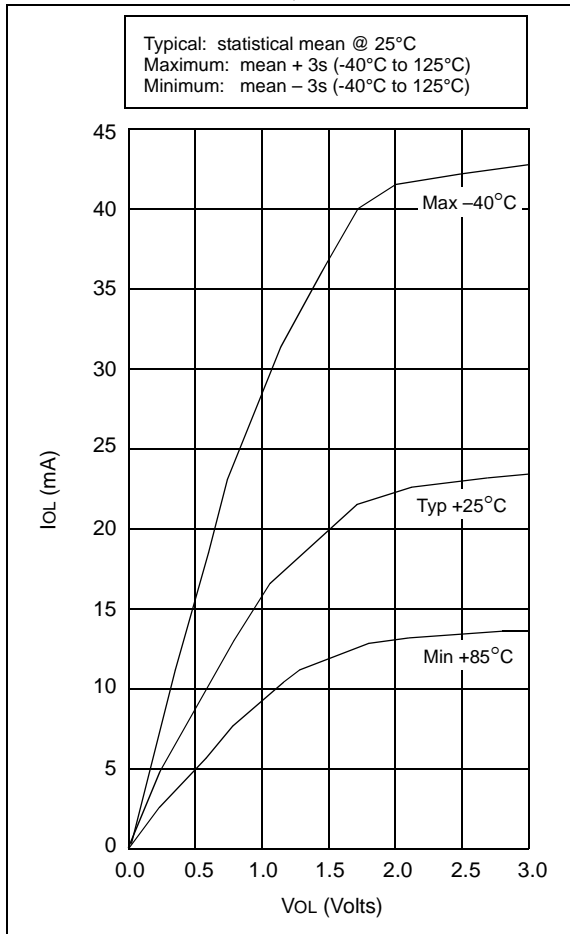
FIGURE 16-23: PORTA, B AND C I$_{OL}$ vs. V$_{OL}$, V$_{DD}$ = 5V

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)
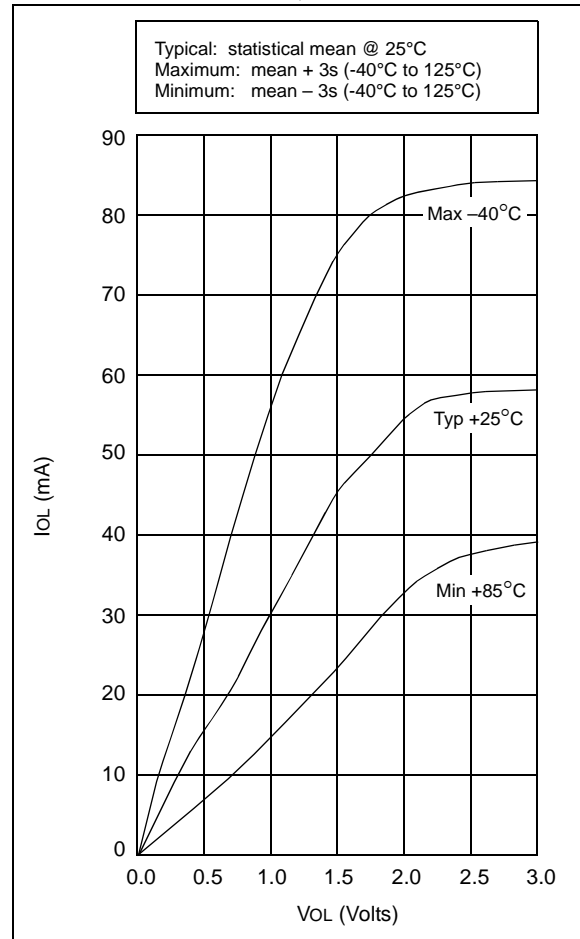
TABLE 16-2: INPUT CAPACITANCE FOR PIC16C54A/C58A

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{MCLR}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

17.0   ELECTRICAL CHARACTERISTICS - PIC16LC54A

Absolute Maximum Ratings[†]

Ambient temperature under bias .... −55°C to +125°C

Storage temperature .... −65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} .... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} .... 0 to +14V

Voltage on all other pins with respect to V_{SS} .... −0.6V to (V_{DD} + 0.6V)

Total power dissipation[1] .... 800 mW

Max. current out of V_{SS} pin .... 150 mA

Max. current into V_{DD} pin .... 100 mA

Max. current into an input pin (T0CKI only) .... ±500 µA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) .... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) .... ±20 mA

Max. output current sunk by any I/O pin .... 25 mA

Max. output current sourced by any I/O pin .... 20 mA

Max. output current sourced by a single I/O (Port A, B or C) .... 50 mA

Max. output current sunk by a single I/O (Port A, B or C) .... 50 mA

Note 1: Power dissipation is calculated as follows: $Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 17-3: **PIC16LC54C/55A/56A/57C/58B VOLTAGE-FREQUENCY GRAPH,**
0°C ≤ T$_A$ ≤ +85°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
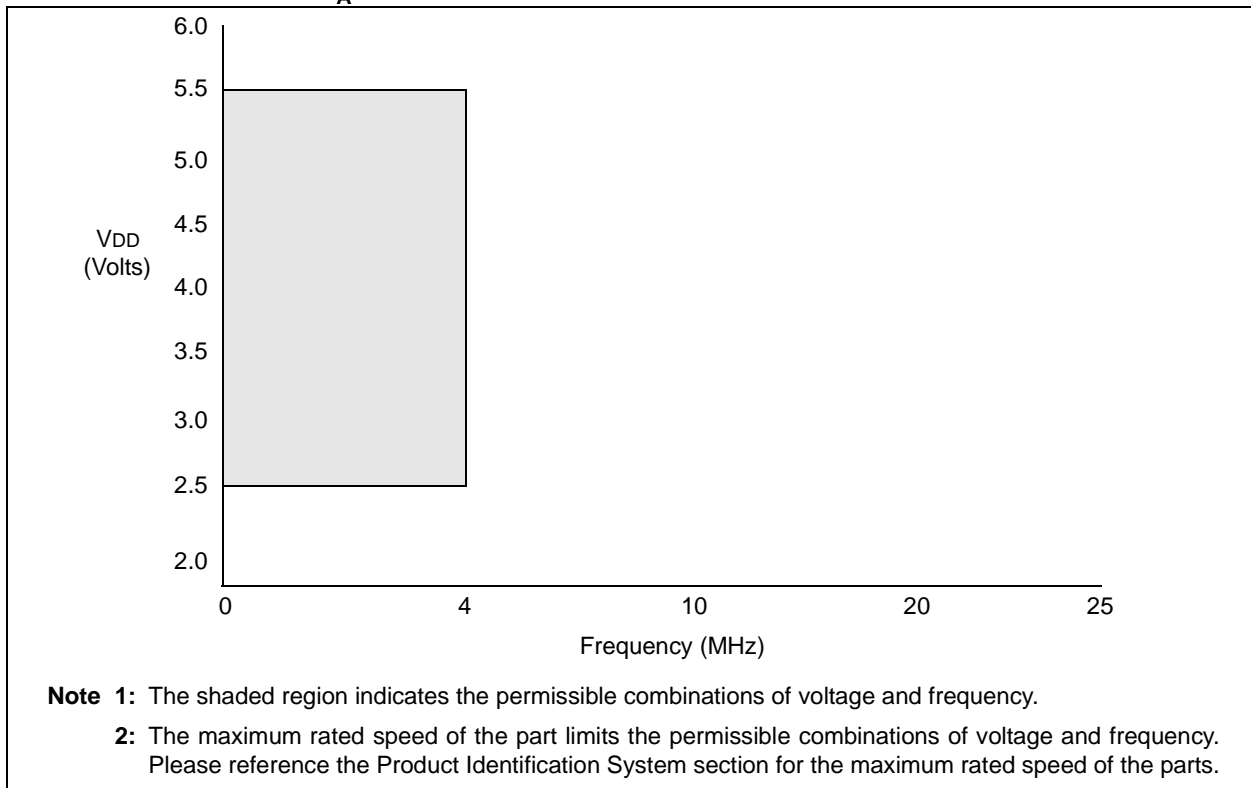
FIGURE 17-4: **PIC16LC54C/55A/56A/57C/58B VOLTAGE-FREQUENCY GRAPH,**
-40°C ≤ T$_A$ ≤ 0°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

PIC16C5X
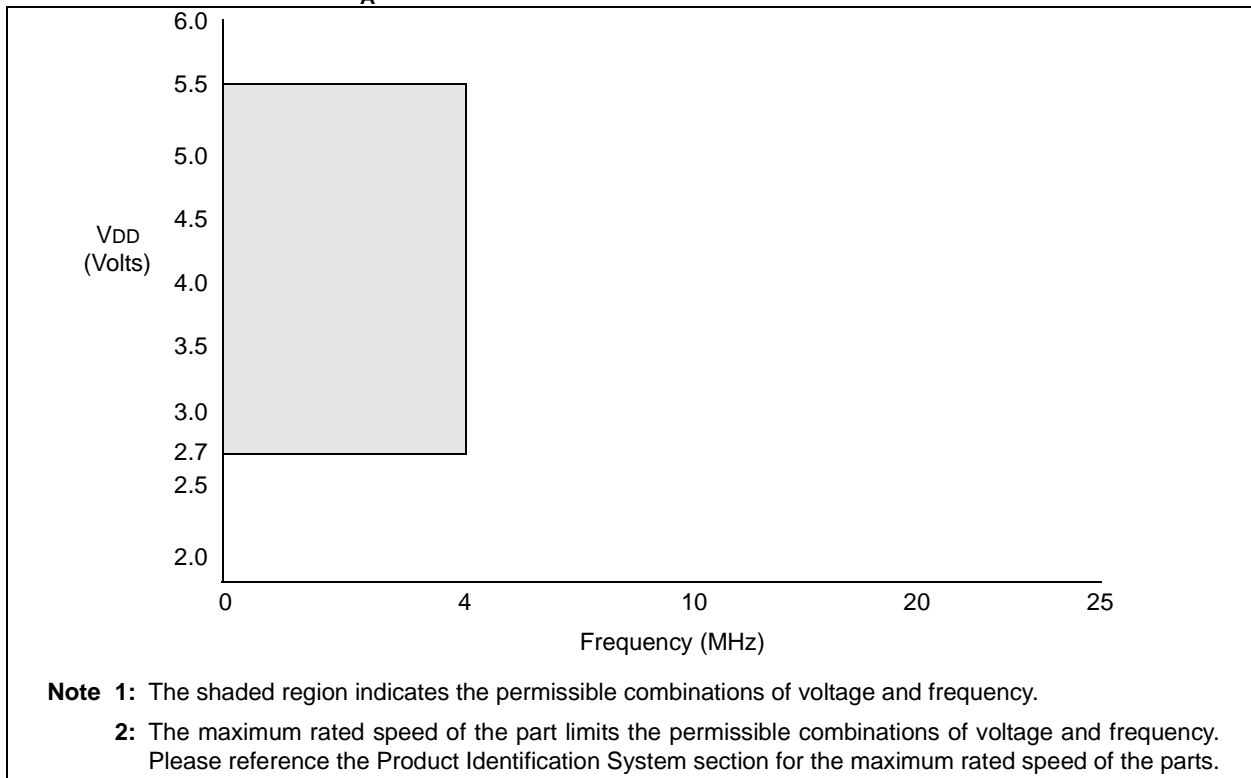
FIGURE 18-2: **TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 PF, 25°C**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

R=3.3K

R=5K

R=10K

R=100K

VDD (Volts)
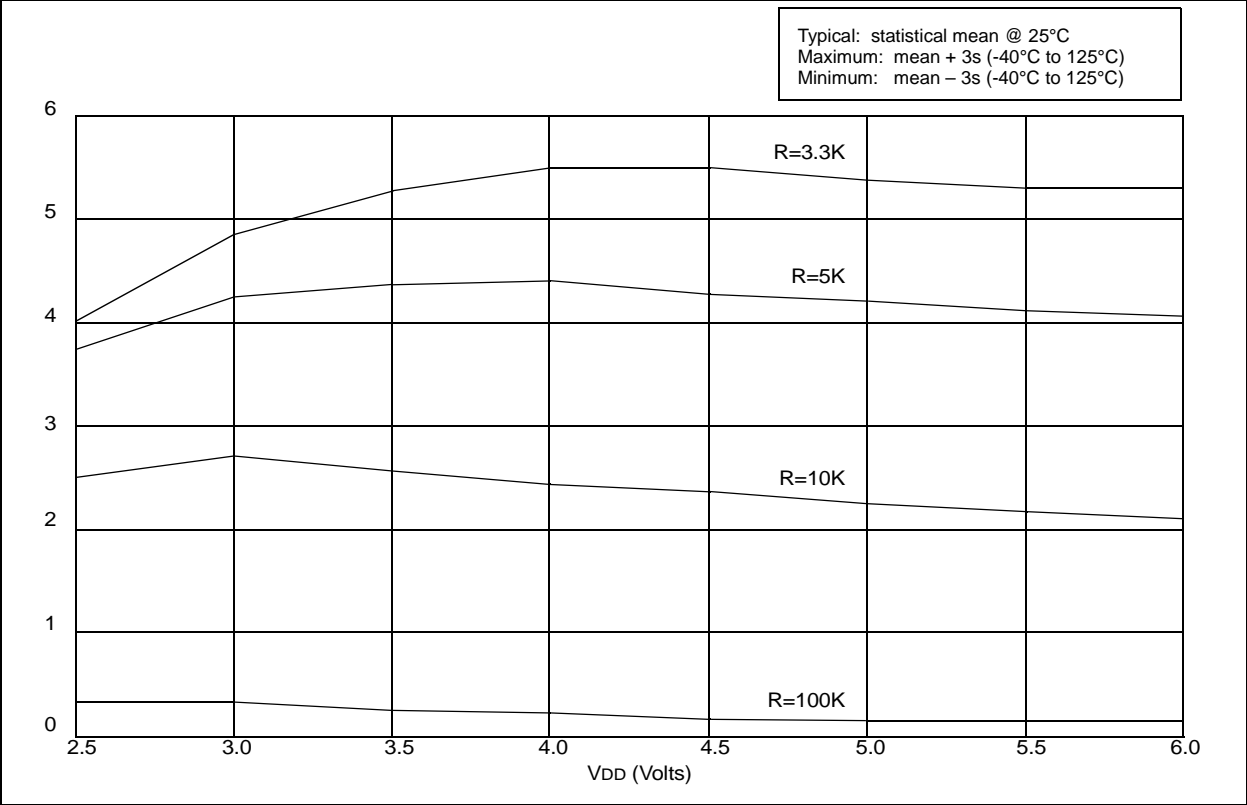
FIGURE 18-3: **TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 PF, 25°C**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

R=3.3K

R=5K

R=10K

R=100K

FOSC (MHz)

VDD (Volts)

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PIC16C5X
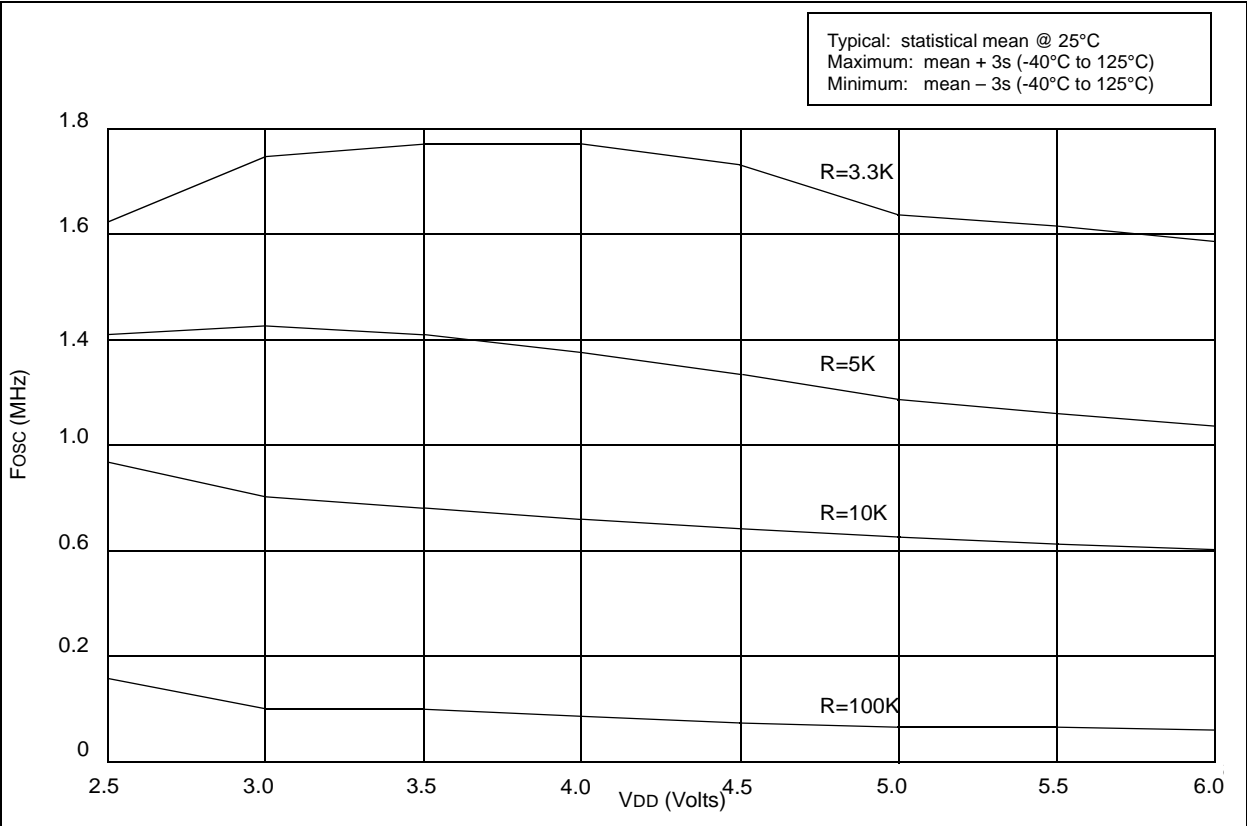
FIGURE 18-16: PORTA, B AND C I_{OH} vs. V_{OH}, V_{DD} = 5 V
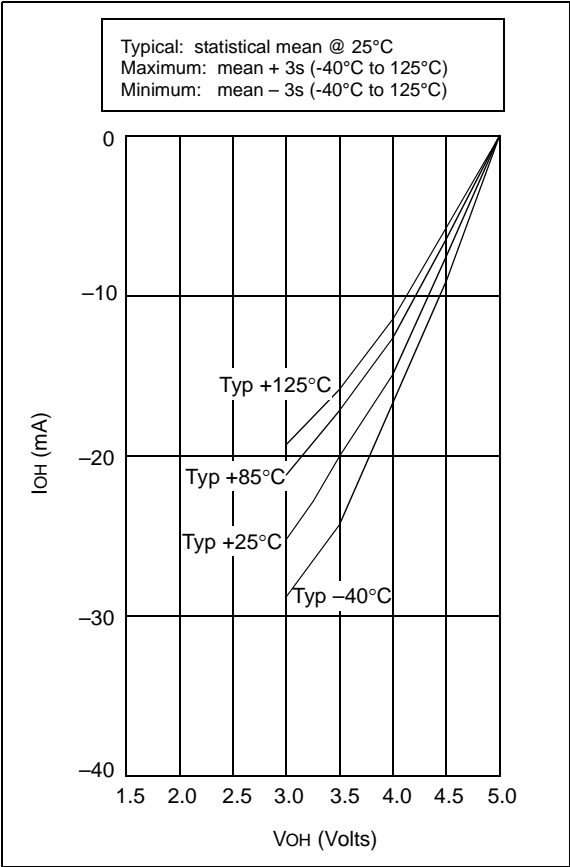
FIGURE 18-17: PORTA, B AND C I_{OL} vs. V_{OL}, V_{DD} = 3 V

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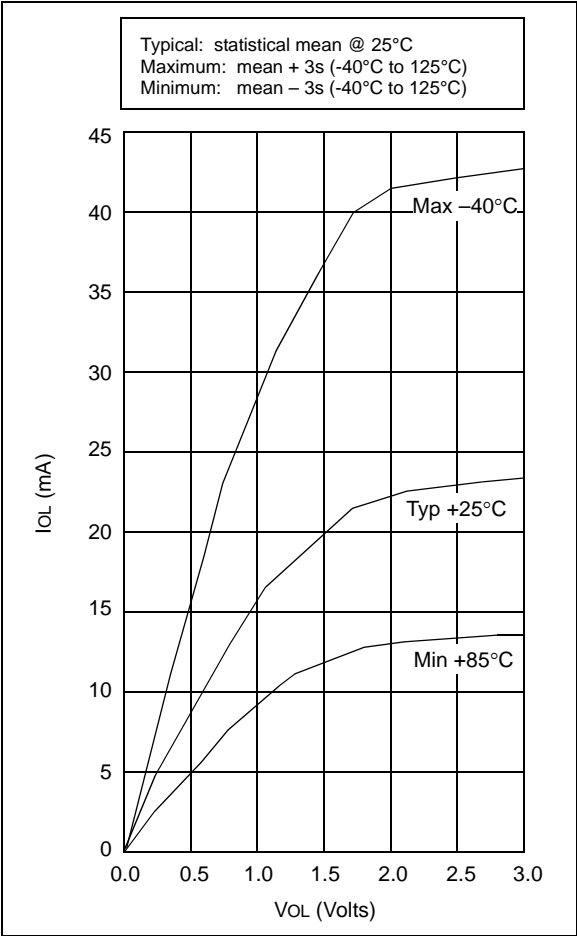
19.3   Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

**FIGURE 19-2:   LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS -
PIC16C54C/C55A/C56A/C57C/C58B-40**

C_L = 50 pF for all pins except OSC2
0 pF for OSC2 in HS mode for operation between 20 MHz to 40 MHz
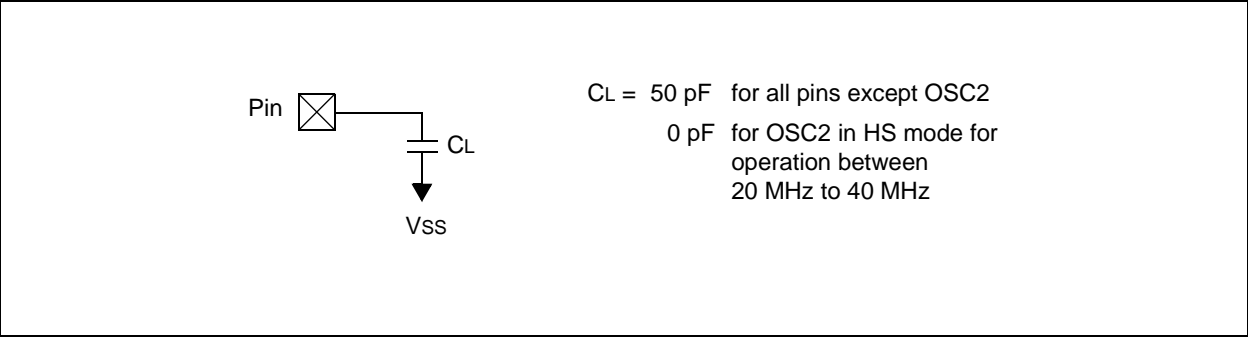
28-Lead Plastic Dual In-line (P) – 600 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
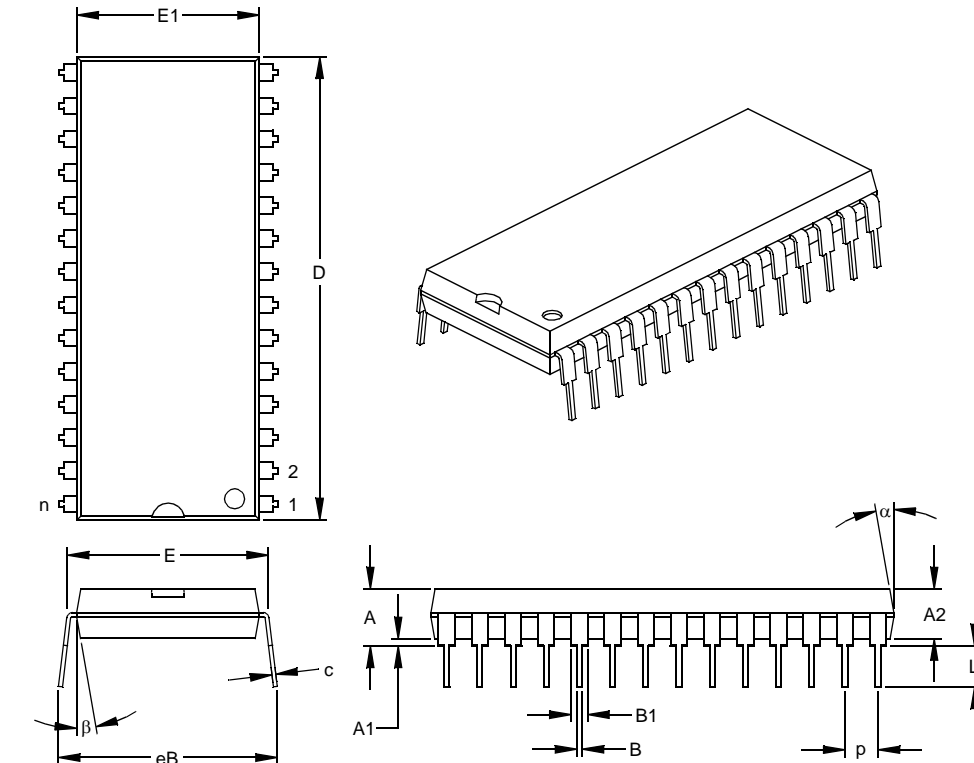
	Units		INCHES*			MILLIMETERS	
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.175	.190	4.06	4.45	4.83
Molded Package Thickness	A2	.140	.150	.160	3.56	3.81	4.06
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88
Molded Package Width	E1	.505	.545	.560	12.83	13.84	14.22
Overall Length	D	1.395	1.430	1.465	35.43	36.32	37.21
Tip to Seating Plane	L	.120	.130	.135	3.05	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.030	.050	.070	0.76	1.27	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.620	.650	.680	15.75	16.51	17.27
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MO-011
Drawing No. C04-079

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PIC16C5X

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