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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc55a-04-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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## FIGURE 8-4: TIMER0 TIMING: INTERNAL CLOCK/PRESCALER 1:2



#### TABLE 8-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	<u>Value</u> on MCLR and WDT Reset
01h	01h TMR0 Timer0 - 8-bit real-time clock/counter									xxxx xxxx	uuuu uuuu
N/A	OPTION	_		TOCS	TOSE	PSA	PS2	PS1	PS0	11 1111	11 1111

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells not used by Timer0.





# 9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of realtime applications. The PIC16C5X family of microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator Selection (Section 4.0)
- RESET (Section 5.0)
- Power-On Reset (Section 5.1)
- Device Reset Timer (Section 5.2)
- Watchdog Timer (WDT) (Section 9.2)
- SLEEP (Section 9.3)
- Code protection (Section 9.4)
- ID locations (Section 9.5)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in RESET until the crystal oscillator is stable. With this timer on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake up from SLEEP through external RESET or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

# PIC16C5X

XORLW	Exclusiv	e OR lite	eral with	w
Syntax:	[label]	XORLW	k	
Operands:	$0 \le k \le 2$	55		
Operation:	(W) .XOF	$R. k \to (W$	/)	
Status Affected:	Z			
Encoding:	1111	kkkk	kkkk	
Description:	XOR'ed	with the e	e W regis eight bit lit ed in the V	eral 'k'.
Words:	1			
Cycles:	1			
Example:	XORLW	0xAF		
Before Instru W = After Instruct W =				

Exclusive OR W with f	
[ label ] XORWF f,d	-
$\begin{array}{l} 0 \leq f \leq 31 \\ d  \in  [0,1] \end{array}$	
(W) .XOR. (f) $\rightarrow$ (dest)	
ted: Z	
0001 10df ffff	
W register with register 'f'. If 'd' is 0 the result is stored in the W regis- ter. If 'd' is 1 the result is stored back in register 'f'.	
1	
1	
XORWF REG,1	
Instruction G = 0xAF = 0xB5 struction G = 0x1A = 0xB5	
the result is stored in t ter. If 'd' is 1 the result back in register 'f'. 1 1 XORWF REG, 1 nstruction G = 0xAF = 0xB5 struction	er 'f'. If 'd' is 0 the W regis-

#### 11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for precompiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

## 11.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multiproject software development tool.

### 11.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft<sup>®</sup> Windows environment were chosen to best make these features available to you, the end user.

# 11.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

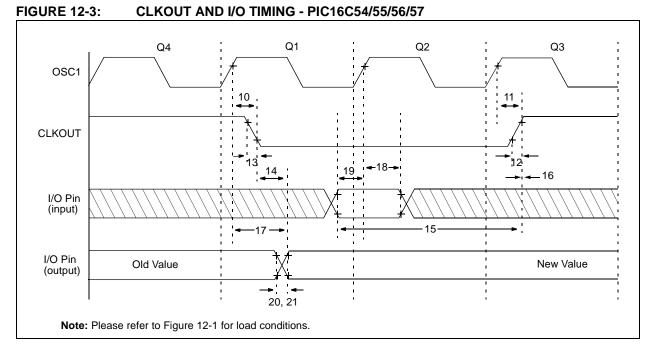
# 12.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

### Absolute Maximum Ratings<sup>(†)</sup>

Ambient Temperature under bias	–55°C to +125°C
Storage Temperature	65°C to +150°C
Voltage on VDD with respect to VSS	0V to +7.5V
Voltage on MCLR with respect to Vss <sup>(1)</sup>	0V to +14V
Voltage on all other pins with respect to Vss	0.6V to (VDD + 0.6V)
Total power dissipation <sup>(2)</sup>	800 mW
Max. current out of Vss pin	150 mA
Max. current into Vod pin	100 mA
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, Iк (Vi < 0 or Vi > VDD)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)	±20 mA
Max. output current sunk by any I/O pin	25 mA
Max. output current sourced by any I/O pin	20 mA
Max. output current sourced by a single I/O port (PORTA, B or C)	40 mA
Max. output current sunk by a single I/O port (PORTA, B or C)	50 mA

- **Note 1:** Voltage spikes below Vss at the  $\overline{\text{MCLR}}$  pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50 to 100  $\Omega$  should be used when applying a "low" level to the  $\overline{\text{MCLR}}$  pin rather than pulling this pin directly to Vss.
  - 2: Power Dissipation is calculated as follows: Pdis = VDD x {IDD  $\Sigma$  IOH} +  $\Sigma$  {(VDD VOH) x IOH} +  $\Sigma$ (VOL x IOL)

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



#### TABLE 12-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54/55/56/57

AC Char	acteristics	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for extended} \end{array}$							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units			
10	TosH2ckL	OSC1↑ to CLKOUT↓ <sup>(1)</sup>	_	15	30**	ns			
11	TosH2ckH	OSC1↑ to CLKOUT↑ <sup>(1)</sup>	_	15	30**	ns			
12	TckR	CLKOUT rise time <sup>(1)</sup>		5.0	15**	ns			
13	TckF	CLKOUT fall time <sup>(1)</sup>	—	5.0	15**	ns			
14	TckL2ioV	CLKOUT↓ to Port out valid <sup>(1)</sup>			40**	ns			
15	TioV2ckH	Port in valid before CLKOUT <sup>(1)</sup>	0.25 TCY+30*	_	_	ns			
16	TckH2iol	Port in hold after CLKOUT <sup>(1)</sup>	0*	_	_	ns			
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid <sup>(2)</sup>	_		100*	ns			
18	TosH2iol	OSC1 <sup>↑</sup> (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—		ns			
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns			
20	TioR	Port output rise time <sup>(2)</sup>	—	10	25**	ns			
21	TioF	Port output fall time <sup>(2)</sup>	—	10	25**	ns			

\* These parameters are characterized but not tested.

\*\* These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Please refer to Figure 12-1 for load conditions.

#### 13.2 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

			Standard Operating Conditions (unless otherwise specified Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
D001	Vdd	Supply Voltage RC, XT and LP modes HS mode	3.25 4.5		6.0 5.5	V V		
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	—	1.5*	—	V	Device in SLEEP mode	
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset	
D004	Svdd	VDD Rise Rate to ensure Power- on Reset	0.05*	_		V/ms	See Section 5.1 for details on Power-on Reset	
D010	IDD	Supply Current <sup>(2)</sup> RC <sup>(3)</sup> and XT modes HS mode HS mode		1.8 4.8 9.0	3.3 10 20	mA mA mA	Fosc = 4.0 MHz, Vdd = 5.5V Fosc = 10 MHz, Vdd = 5.5V Fosc = 16 MHz, Vdd = 5.5V	
D020	IPD	Power-down Current <sup>(2)</sup>		5.0 0.8	22 18	μΑ μΑ	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled	

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

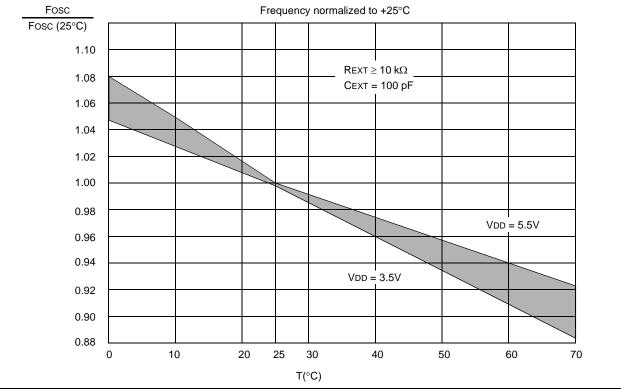
- 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
  - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
  - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

# 14.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean +  $3\sigma$ ) or (mean -  $3\sigma$ ) respectively, where  $\sigma$  is a standard deviation, over the whole temperature range.





#### TABLE 14-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Average Fosc @ 5 V, 25°C			
20 pF	3.3K	5 MHz	± 27%		
	5K	3.8 MHz	± 21%		
	10K	2.2 MHz	± 21%		
	100K	262 kHz	± 31%		
100 pF	3.3K	1.6 MHz	± 13%		
	5K	1.2 MHz	± 13%		
	10K	684 kHz	± 18%		
	100K	71 kHz	± 25%		
300 pF	3.3K	660 kHz	± 10%		
	5.0K	484 kHz	± 14%		
	10K	267 kHz	± 15%		
	100K	29 kHz	± 19%		

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is  $\pm 3$  standard deviations from the average value for VDD = 5V.

## 15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04 PIC16LC54A-04I (Commercial, Industrial)				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
PIC16C5	<b>54A-04, 10</b> 5 <b>4A-04I, 1</b> 0 ercial, Ind	01, 201	$\begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$				$0^{\circ}C \le TA \le +70^{\circ}C$ for commercial	
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions	
	IPD	Power-down Current <sup>(2)</sup>						
D006		PIC16LC5X		2.5 0.25 2.5 0.25	12 4.0 14 5.0	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT enabled, Commercial VDD = 2.5V, WDT disabled, Commercial VDD = 2.5V, WDT enabled, Industrial VDD = 2.5V, WDT disabled, Industrial	
D006A		PIC16C5X		4.0 0.25 5.0 0.3	12 4.0 14 5.0	μΑ μΑ μΑ μΑ	VDD = 3.0V, WDT enabled, Commercial VDD = 3.0V, WDT disabled, Commercial VDD = 3.0V, WDT enabled, Industrial VDD = 3.0V, WDT disabled, Industrial	

Legend: Rows with standard voltage device data only are shaded for improved readability.

\* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k $\Omega$ .

#### 15.3 DC Characteristics: PIC16LV54A-02 (Commercial) PIC16LV54A-02I (Industrial)

PIC16LV54A-02 PIC16LV54A-02I (Commercial, Industrial)				$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -20^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$					
Param No.	Symbol Characteristic		Min Typ†		Max	Units	Conditions		
D001	Vdd	Supply Voltage RC and XT modes	2.0	_	3.8	V			
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	—	1.5*	—	V	Device in SLEEP mode		
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*		—	V/ms	See Section 5.1 for details on Power-on Reset		
D010	IDD	<b>Supply Current<sup>(2)</sup></b> RC <sup>(3)</sup> and XT modes LP mode, Commercial LP mode, Industrial		0.5 11 14	 27 35	μA	Fosc = 2.0 MHz, VDD = 3.0V Fosc = 32 kHz, VDD = 2.5V WDT disabled Fosc = 32 kHz, VDD = 2.5V WDT disabled		
D020	IPD	<b>Power-down Current<sup>(2,4)</sup></b> Commercial Commercial Industrial Industrial		2.5 0.25 3.5 0.3	12 4.0 14 5.0	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled		

These parameters are characterized but not tested.

- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- **Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
  - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
    - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
    - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
  - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.
  - 4: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection on wake-up from SLEEP mode or during initial power-up.

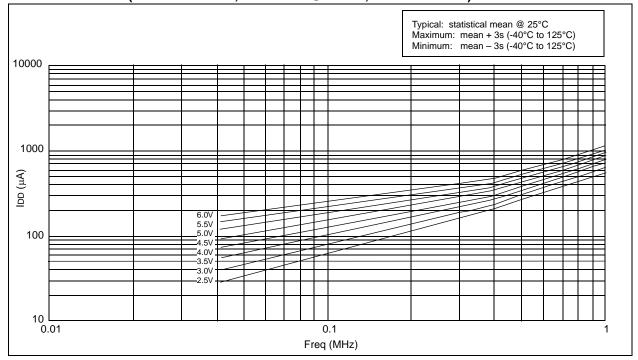
 Typical: statistical mean @ 25°C.

 Maximum: mean + 3s (-40°C to 125°C)

 Minimum: mean - 3s (-40°C to 125°C)
 </tr

FIGURE 16-14: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 PF, 25°C)

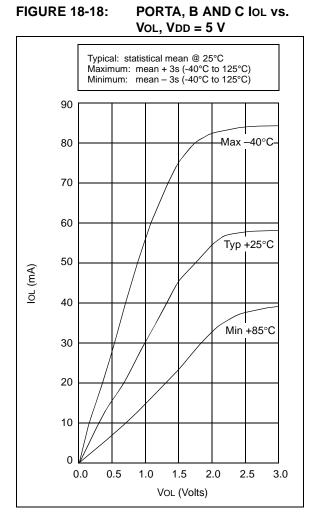
FIGURE 16-15: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 PF, -40°C to +85°C)





#### FIGURE 16-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD





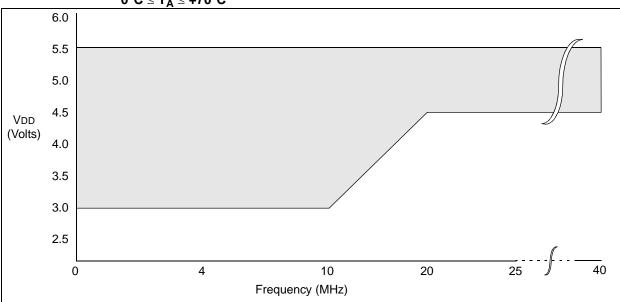
#### TABLE 18-2:INPUT CAPACITANCE

Pin	Typical Capacitance (pF)				
Pin	18L PDIP	18L SOIC			
RA port	5.0	4.3			
RB port	5.0	4.3			
MCLR	17.0	17.0			
OSC1	4.0	3.5			
OSC2/CLKOUT	4.3	3.5			
тоскі	3.2	2.8			

All capacitance values are typical at  $25^{\circ}$ C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

# PIC16C5X

FIGURE 19-1: PIC16C54C/C55A/C56A/C57C/C58B-40 VOLTAGE-FREQUENCY GRAPH,  $0^{\circ}C \le T_A \le +70^{\circ}C$ 





- **2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
- **3:** Operation between 20 to 40 MHz requires the following:
  - VDD between 4.5V. and 5.5V
  - OSC1 externally driven
  - OSC2 not connected
  - HS mode
  - Commercial temperatures

Devices qualified for 40 MHz operation have -40 designation (ex: PIC16C54C-40/P).

4: For operation between DC and 20 MHz, see Section 17.1.

# 19.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)<sup>(1)</sup>

PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)							itions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial	
Param No.	Symbol	Characteristic	Min	Min Typ† Max Units		Units	Conditions	
D001	Vdd	Supply Voltage	4.5	-	5.5	V	HS mode from 20 - 40 MHz	
D002	Vdr	RAM Data Retention Voltage <sup>(2)</sup>		1.5*	—	V	Device in SLEEP mode	
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset	
D004	SVDD	VDD Rise Rate to ensure Power- on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset	
D010	Idd	Supply Current <sup>(3)</sup>	_	5.2 6.8	12.3 16	mA mA	Fosc = 40 MHz, $VDD$ = 4.5V, HS mode Fosc = 40 MHz, $VDD$ = 5.5V, HS mode	
D020	IPD	Power-down Current <sup>(3)</sup>	_	1.8 9.8	7.0 27*	μΑ μΑ	VDD = 5.5V, WDT disabled, Commercial VDD = 5.5V, WDT enabled, Commercial	

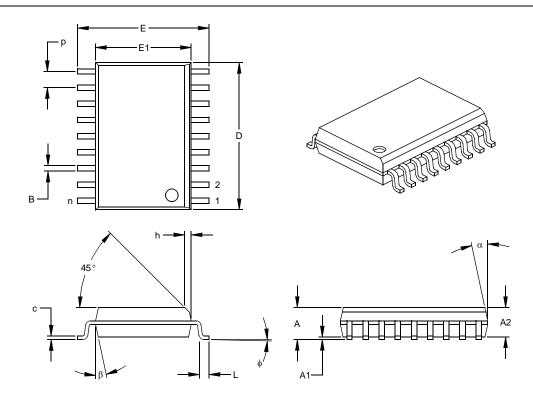
\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- **Note 1:** Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected, HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 19.1.
  - **2:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
  - **3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
    - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
    - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

#### 18-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging



	Units	INCHES*		MILLIMETERS		6	
Dimensi	on Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	р		.050			1.27	
Overall Height	А	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	ø	0	4	8	0	4	8
Lead Thickness	С	.009	.011	.012	0.23	0.27	0.30
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013 Drawing No. C04-051

# PIC16C5X

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# **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	- <u>xx</u>	Ť	<u>/xx</u>	<u>xxx</u>	Exa	nples	S:
Device	Frequency Range/OSC Type           PIC16C54           PIC16C54A           PIC16C54C           PIC16C55A           PIC16C55A           PIC16C55A           PIC16C56A           PIC16C57C           PIC16C57C           PIC16C58B           PIC16C58B	Temperature Range	(2) T(2)	Pattern	a) b) c) d) Note	PDIP QTP PIC10 packa PIC10 cial te dard PIC1 temp MHz, #123	C = normal voltage range LC = extended
Frequency Range/ Oscillator Type	04 200 KHz (LI 10 10 MHz (HS 20 20 MHz (HS 40 40 MHz (HS b <sup>(4)</sup> No oscillato *RC/LP/XT/HS a -02 is available for -04/10/20 options	Crystal ystal/Resonator Crystal P) or 2 MHz (XT an P) or 4 MHz (XT an conly) conly) conly) r type for JW packa re for 16C54/55/56	d RC) ages <sup>(3)</sup> /57 devices on all other device	s		3:	T = in tape and reel - SOIC and SSOP packages only JW Devices are UV erasable and can be programmed to any device configura- tion. JW Devices meet the electrical requirements of each oscillator type, including LC devices. b = Blank
Temperature Range	$b^{(4)} = 0^{\circ}C$ $I = -40^{\circ}C$ $E = -40^{\circ}C$	to +85°C					
Package	JW = 28-pin DIP <sup>(3)</sup> P = 28-pin SO = 300 m SS = 209 m SP = 28-pin	Waffle Pack 600 mil/18-pin 300 600 mil/18-pin 300 il SOIC il SSOP 300 mil Skinny PE for additional packa	) mil PDIP DIP				
Pattern		I code (factory spe lank for OTP and V					

#### Sales and Support

#### **Data Sheets**

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office

2. The Microchip Worldwide Site (www.microchip.com)